

'89.

GS LINEAR IC DATA BOOK

- TV/VCR/AUDIO
- TELECOMMUNICATION
- REMOTE CONTROL
- INDUSTRY



**ELECTRONIC
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GoldStar

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GoldStar

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PRELIMINARY data sheet is issued in advanced of the availability of samples and generally indicates that at the time of printing the device is not characterized. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed.

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6. **INDUSTRY APPLICATION**

GOLDSTAR SEMICONDUCTOR SALES NETWORK

QUALITY ASSURANCE MANUAL

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1. INTRODUCTION

In recent years, advances in integrated circuit have been rapid with increasing density and speed accompanied by decreasing cost. To meet these advances, there are three basic ingredients in the manufacture of reliable integrated circuits.

First, The device must be designed with the user's applications and reliability requirements in mind. Secondly, The device must be manufactured with the optimum technology for the application. Thirdly, Controls must be established to assure maintenance of the quality/reliability levels. Goldstar has a Quality Assurance System and conducts extensive reliability testing to supply its customer's needs.

This report presents Quality Assurance System and Reliability test results of Goldstar Company Products.

2. QUALITY ASSURANCE SYSTEM

To ensure that customers are satisfied with the products that are supplied, quality assurance programs are used at both the design and manufacturing phases, focusing on the following points:

- (1) In the development stage, reliability is designed into products. A thorough evaluation of reliability is performed to ascertain whether the design will lead to the desired quality and reliability.
- (2) Efforts are made at the manufacturing stage of quality control to assure that quality and reliability are built into products. Intermediate, final, and quality assurance inspection are used to verify that the desired quality and reliability have been achieved.
- (3) Information with regard to quality is fed back in a timely manner so that the required corrective action can be taken by quality assurance personnel.

2.1 Quality Assurance at the Development Stage

It is not an exaggeration to say that the fundamental quality and reliability of a discrete semiconductor device or an integrated circuit is determined at the design stage. Thus, to eliminate design problems and provide design improvements while attaining the desired quality and reliability, design reviews are performed on prototypes assure product quality. Particularly in the case of integrated circuits, bread-board models of the circuit using standard components can be an effective means of evaluating the required characteristic and quality. In addition CAD technology may be used to aid in the design of circuits and devices based on design standards.

Between the development stage, and mass production, there are two steps of prototype and pre-production (trial mass production).

At the prototype development stage, new theories, technologies and concepts are used by the development department to design and produce a new product. To determine whether the desired goals for characteristics, ratings, and reliability have been met, primary type test is performed at this stage. Based on these results, thorough investigations are made by both the engineering and quality assurance departments. Should product deficiencies arise, inspections and failure analysis are performed to enable improvements of the development prototype.

At the pre-production stage, the production department produces sufficient products having quality equal to or superior to the prototype. At this stage, secondary type test is used to verify quality. The required product specifications, operation instructions, drawings, etc., are produced at this stage in addition to the required manufacturing facilities.

2.2 Quality Assurance at the Mass Production Stage

At the mass production stage, the production department takes over production of product based on production planning. To maintain equal or better quality than that obtained in previous stages, careful control of materials purchasing, production processing, environment and facilities is performed. In addition, in process inspections and final inspections provide the required information with regard to partially completed and completed devices to assure overall quality.

2.2.1 Control of Materials Purchasing

While the responsibility for quality of individual materials purchased from vendors based on drawings and purchase specifications is the responsibility of the vendor, the corporation provides data from incoming inspection of sampled products as a means of monitoring quality and assuring materials quality.

Selection of vendors is made after an investigation of quality control, management, facilities and production capacity of the vendor, placing heavy emphasis on quality. Next, a meeting is held with the vendor concerning the purchase specifications, and prototypes or sample evaluations are used to verify quality at the beginning of a purchase cycle or after a change in manufacturing method or specifications.

2.2.2 Control of the Manufacturing Process

To prototype products of high quality in an economic manner, quality must be built-in at the manufacturing stage. To do this, work is carried out in accordance with operation instructions and check sheets are used to control those aspects of manufacturing that could affect quality. For example, such information as the purity of water, atmosphere, furnace temperature and gas flow are recorded. In addition, because of their great influence on diffusion, diffusion depth and surface density are recorded and used as control data for process conditions. Also, operations such as wire bonding which are affected by differences of individuals have been fully automated to contribute to product uniformity.

In-process inspections and final inspections are performed to evaluate product quality including outward appearance, dimensions, structure, as well as mechanical and electrical characteristics. The data obtained by such inspections is fed back to earlier processes to maintain and improve product quality as well as reduce variations in these areas.

Wafer processing and assembly inspections are part of the in-process inspection program, each contributing to the concept of building in quality at the manufacturing stage by providing self checks and the inspections performed by the quality control department. A final inspection of all products is performed to verify electrical characteristics as well as outward appearance of products. In addition, to improve product quality uniformity, debugging is used as a means of eliminating products which do not meet quality specifications. Again, data from these inspections are useful in quality control.

Products which have passed final inspection are then subjected to quality assurance inspections. This is a form of overall inspection from the standpoint of the end user and is used to accept or reject products on a lot basis, including tests of outward appearance, electrical characteristics, thermal and mechanical environment, and endurance. As an additional control test, samples are made periodically for evaluation of reliability. These tests include those of electrical characteristics, thermal and mechanical environment, and endurance for long periods of operation. The information on quality obtained by such quality assurance inspections is fed back in a timely fashion to the related departments, enabling the maintenance and improvement of quality as well as providing a means of predicting product quality in the market place.

QUALITY ASSURANCE MANUAL


STANDARD ASS'Y FLOW CHART OF GS

FLOW CHART	PROCESS TITLE	QC POINT
<pre> graph TD Start([Start]) --> Wafer[/Wafer/] Wafer --> FM((Foil Mount)) FM --> WS((Wafer Sawing)) WS --> QCM1[Q.C Monitor * DI Water * Visual] QCM1 --> DB((Die Bond)) DB --> QCM2[Q.C Monitor * Visual * Die Shear] QCM2 --> WB((Wire Bond)) WB --> QCM3[Q.C Monitor * Visual * Bond pull * Crater] QCM3 --> Insp3[3rd Optical Insp.] Insp3 --> QCM4[Q.C 3rd O/Gate * Visual] QCM4 --> Mold((Molding)) Mold --> QCM5[Q.C Monitor * Visual * X-Ray Monitor] QCM5 --> Deflash((Deflash/Trim/Form)) Deflash --> QCM6[Q.C Monitor * Visual/Dimension] QCM6 --> End([End]) </pre>	Wafer	
	Foil Mount	
	Wafer Sawing	
	Q.C Monitor * DI Water * Visual	RESISTIVITY VISUAL
	Die Bond	
	Q.C Monitor * Visual * Die Shear	APPEARANCE STRENGTH
	Wire Bond	
	Q.C Monitor * Visual * Bond pull * Crater	APPEARANCE APPEARANCE, STRENGTH CRATER
	3rd Optical Insp.	
	Q.C 3rd O/Gate * Visual	APPEARANCE
	Molding	SPIRAL FLOW
	Q.C Monitor * Visual * X-Ray Monitor	APPEARANCE X-RAY INSP.
	Deflash/Trim/Form	
	Q.C Monitor * Visual/Dimension	APPEARANCE/DIMENSION

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FLOW CHART	PROCESS TITLE	QC POINT
<pre> graph TD Start(()) --> S1[] S1 --> D1{ } D1 --> S2[] S2 --> D2{ } D2 --> S3[] S3 --> D3{ } D3 --> S4[] S4 --> D4{ } D4 --> S5[] S5 --> D5{ } D5 --> S6[] S6 --> End((())) </pre>	Solder-Dipping	
	Q.C Monitor * Temp of S/Bath * Sn in Solder * Solderability	TEMPERATURE. % OF Sn APPEARANCE
	4th Optical Insp	
	4th O/Gate * Visual	APPEARANCE
	Temp. cycle (Option)	
	Mark & Cure	
	Final Visual/Mech.	
	Initial Class	
	Burn-In (Option)	
	Final Test	
	Q.C Final Gate * Visual	APPEARANCE
	* Electrical	ELECTRICAL PARAMETERS * D.C & SPEED * FUNCTION
	RELIABILITY TEST * LIFE TEST LTPD: 5% * 85/85 TEST LTPD: 10% * PRESSURE POT LTPD: 10% * THERMAL SERIES LTPD: 10% * LEAD INTEGRITY LTPD: 20% * PHYSICAL DIMENSION LTPD: 15%	ENVIRONMENTAL TEST MECHANICAL TEST AND ENDURANCE TEST

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FLOW CHART	PROCESS TITLE	QC POINT
	<ul style="list-style-type: none">* RESISTANCE TO SOLVENTS LTPD: 15%* SOLDERABILITY LTPD: 10% <p>Packing</p> <p>Q.C Pack Gate</p> <p>Ship</p> <ul style="list-style-type: none">* ESD MONITOR (ALL PROCESS)	

2.2.3 Environmental Control

In the semiconductor industry, the environment plays a large role in influencing product quality and reliability. Control levels for dust, humidity, and temperature are set and rigidly maintained. The gases or water used in the production plant are carefully controlled to ensure high level of purity.

The control of dust is particularly important in reducing manufacturing defects and improving quality and reliability. For this reason the Corporation places heavy emphasis in this area, providing strict controls of working conditions and periodic checks to verify that these are being maintained.

2.2.4 Control of Production Equipment and Instrumentation.

The semiconductor industry is an equipment intensive industry having adopted a large variety of automatic equipment and high performance facilities to provide uniform high quality. The control of such equipment and instrumentation is extremely important in the manufacture of devices. For this reason, to eliminate loss of accuracy and equipment failures, periodic preventive maintenance and inspections are performed.

3. RELIABILITY TEST

3.1 Principle of Reliability

The fundamental principles of reliability engineering predict that the failure rate of any group of devices as a function of time will follow a curve similar to Figure 1. The curve is divided into three regions: Infant Mortality, Random Failures and Wearout Failures. These regions describe the principal classes of failure mechanisms encountered in that portion of the life of a device.

Infant Mortality represents the early life failures of a device. Failures in this region are usually associated with one or more manufacturing defects. After some period of time the failure rate reaches a low value or the Random failure portion of the curve that represents the useful portion of device life. Infant Mortal

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failures are eliminated prior to customer shipment by high voltage cell stress, HTRB and reliability screen testing. (Baking, Temp Cycle, Burn-In)

Wearout failures occur at the end of the device's useful life and are characterized by rapidly rising failure rate with time. This does not occur before hundreds of years for integrated circuits.

Associated with each portion of the curve are specific failure mechanisms. These failure mechanisms have been extensively discussed in the literature.

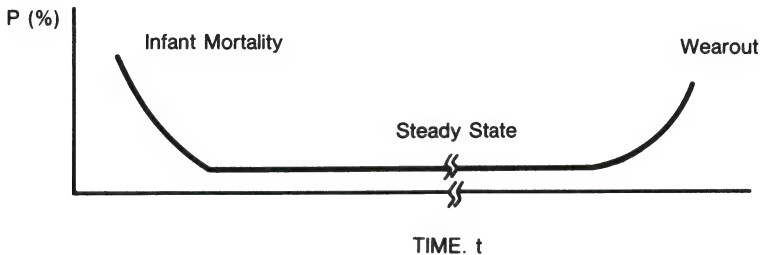


Figure 1. Reliability Life (Bach-Tub) Curve

3.2 Reliability Test Items and Conditions

I. Group A: ELECTRICAL TEST

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR
1. STATIC TEST (AT 25°C)		LTPD 2 : S/S = 266 C = 26	
2. STATIC TEST (AT MAX. OP. TEMP.)		LTPD 3 : S/S = 176 C = 2	AQL = 0.04% S/S = 315 C = 0
3. STATIC TEST (AT MIN. OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	
4. DYNAMIC TEST (AT 25°C)		LTPD 2 : S/S = 266 C = 2	
5. DYNAMIC TEST (AT MAX. OP. TEMP.)		LTPD 3 : S/S = 176 C = 2	
6. DYNAMIC TEST (AT MIN. OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	
7. FUNC. TEST (AT 25°C)		LTPD 2 : S/S = 266 C = 2	
8. FUNC. TEST (AT MAX. MIN OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	
9. SWITCHING (AT 25°C)		LTPD 2 : S/S = 266 C = 2	
10. SWITCHING (AT MAX. OP. TEMP.)		LTPD 3 : S/S = 176 C = 2	
11. SWITCHING (AT MIN. OP. TEMP.)		LTPD 5 : S/S = 105 C = 2	

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II. Group B : Per Lot

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR
Sub 1 PHYSICAL DIMENSION	2016	n = 2 : c = 0	n = 2 : c = 0
Sub 2 RESISTANCE TO SOLVENTS	2015	n = 4 : c = 0	LTPD 15% S/S = 15 C = 0
Sub 3 SOLDERABILITY TEST	2022 2003	LTPD 15% S/S = 15 C = 0	LTPD 10% S/S = 22 C = 0
Sub 4 INTERNAL VISUAL & MECHANICAL	2014	n = 1 : c = 0	n = 1 : c = 0
Sub 5 BOND STRENGTH	2011	LTPD 15% S/S = 15 C = 0	LTPD 15% S/S = 15 C = 0
Sub 6 INTERNAL WATER VAPOR CONTENT	1018	n = 3 : c = 0 or n = 5 : c = 1	NOT BEING
Sub 7 SEAL			
FINE LEAK	1014	LTPD 5% S/S = 45	LTPD 5% S/S = 45
GROSS LEAK		C = 0	C = 0
Sub 8			
A) ELECTRICAL PARAMETERS	Gr A	n = 15 : c = 0	LTPD 10% S/S = 22
B) E. S. D CLASSIFICATION	3015		C = 0
C) ELECTRICAL PARAMETERS	Gr A		

III. Group C : PERIODIC : DIE-RELATED TESTS

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR
Sub 1			
A) STEADY STATE LIFE TEST	1005	AT 125°C : 1000 HRS	AT 125°C : 1000 HRS
B) END POINT ELECTRICAL.		LTPD 5% S/S = 77 C = 1	LTPD 5% S/S = 77 C = 1
Sub 2			
A) TEMPERATURE CYCLE	1010	TEST COND. C	TEST COND. C : 100 CYCLE
B) CONSTANT ACCELERATION	2001	LTPD 15% S/S = 25, C = 1	LTPD 15% S/S = 25, C = 1
C) SEAL	1014	TEST COND. E Y1 ORIENTATION ONLY	TEST COND. E Y1 ORIENTATION ONLY
FINE LEAK		TEST COND. B	TEST COND. B
GROSS LEAK		TEST COND. C	TEST COND. C
D) VISUAL EXAMINATION	1010		
E) END POINT ELECTRICAL.	1011		

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IV. Group D : PACKAGE RELATED TESTS

TEST ITEMS.	METHOD.	MIL-STD-883C		GOLDSTAR	
Sub 1 PHYSICAL DIMENSION	2016	LTPD 15%	S/S = 15 C = 0	LTPD 15%	S/S = 15 C = 0
Sub 2 A) LEAD INTEGRITY	2004	LTPD 15%	S/S = 15 C = 0	LTPD 15%	S/S = 15 C = 0
B) SEAL	1014	TEST COND. B TEST COND. C		TEST COND. B TEST COND. C	
Sub 3 A) THERMAL SHOCK	1011	COND. B : 15 CYCLES LTPD 15%	S/S = 15 C = 0	NOT BEING	
B) TEMPERATURE CYCLE	1010	TEST COND. C : 100 CYCLE		TEST COND. C : 100 CYCLE	
C) MOISTURE RESISTANCE	1004				
D) SEAL	1004	TEST COND. B TEST COND. C		TEST COND. B TEST COND. C	
FINE LEAK GROSS LEAK					
E) VISUAL EXAMINATION	1010 & 1004				
F) END POINT ELECTRICAL.					
Sub 4 A) MECHANICAL SHOCK	2002	LTPD 15%	S/S = 15 C = 0	LTPD 15%	S/S = 15 C = 0
B) VIBRATION, VARIABLE FREQUENCY	2007	COND. B TEST COND. A		COND. B TEST COND. A	
C) CONSTANT ACCELERATION	2001	TEST COND. E Y1 ORIENTATION ONLY		TEST COND. E Y1 ORIENTATION ONLY	
D) SEAL	1014	TEST COND. B TEST COND. C		TEST COND. B TEST COND. C	
FINE LEAK GROSS LEAK					
E) VISUAL EXAMINATION	1010 & 1011				
F) END POINT ELECTRICAL.					
Sub 5 A) SALT ATMOSPHERE	1009	LTPD 15%	S/S = 15 C = 0	NOT BEING	
B) VISUAL EXAMINATION	1009	COND. A			
C) END POINT ELECTRICAL.					
Sub 6 INTERNAL WATER VAPOR CONTENT (5000 PPM)	1018	n = 3 : c = 0 or n = 5 : c = 1		NOT BEING	
Sub 7 ADHESION OF LEAD FINISH	2025	LTPD 15%	S/S = 15 C = 0	LTPD 15%	S/S = 15 C = 0
Sub 8 LID TORQUE	2024	n = 5 : c = 0		n = 5 : c = 0	

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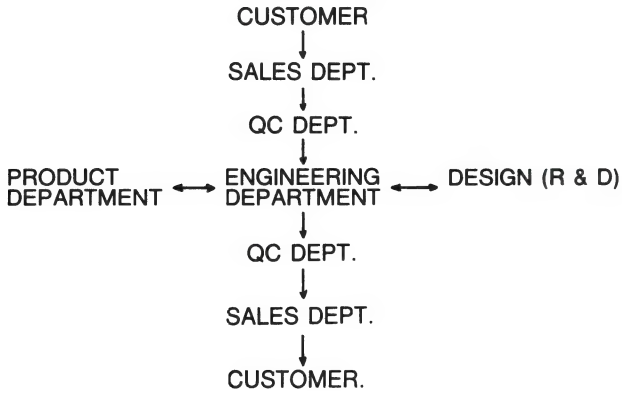
V. Group E : RADIATION HARDNESS ASSURANCE TESTS

TEST ITEMS.	METHOD.	MIL-STD-883C	GOLDSTAR
Sub 1 NEUTRON IRRADIATION A) QUALIFICATION B) QCI	1017	at 25°C n = 15 : c = 0 n = 11 : c = 0	NOT BEING
Sub 2 STEADY-STATE TOTAL DOSE IRRADIATION A) QUALIFICATION B) QCI	1019	at 25°C n = 15 : c = 0 n = 11 : c = 0	NOT BEING

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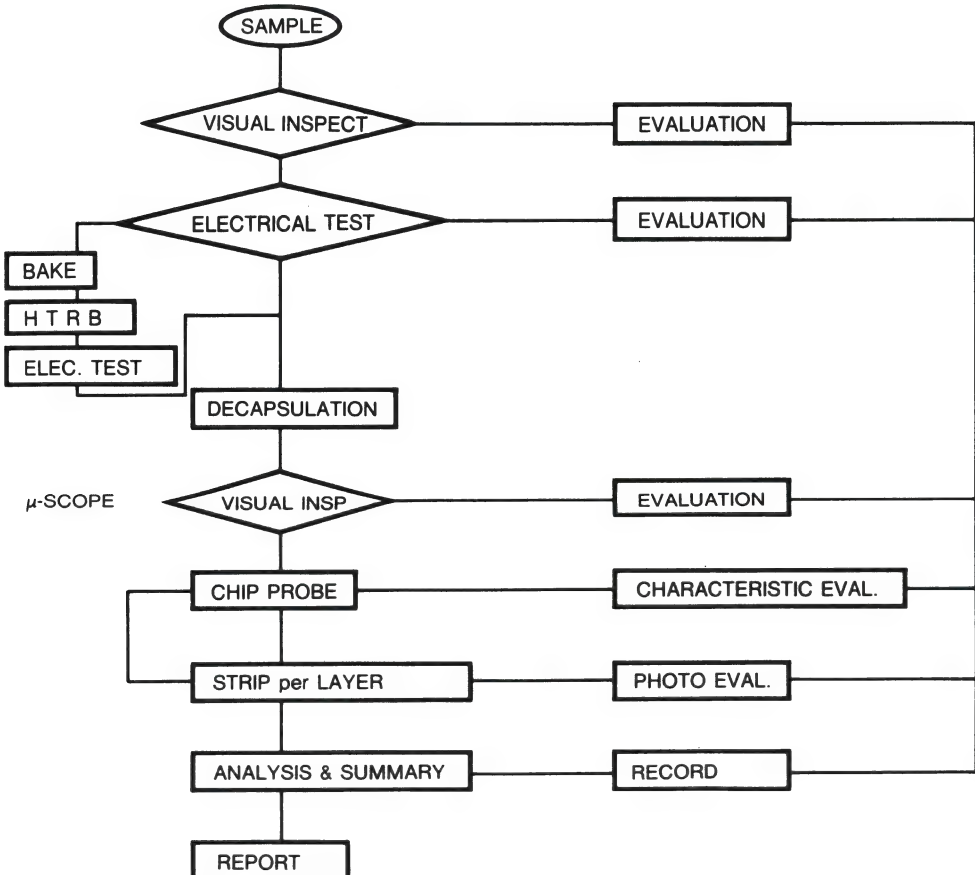
FMA FLOW CHART

PROCEDURE OF FAILURE ANALYSIS



- CLAIM, COMPLAINT
- IF REQUIRED, SEND DEVICE FAILED TO QC DEPT.
- * FAILURE ANALYSIS
- DETAILED INVESTIGATION.
- CORRECTIVE ACTION
- PREVENTION OF REOCCURENCE
- REPORT THE RESULT
- ANSWER TO THE CLAIM.

* FAILURE ANALYSIS



RELIABILITY TEST ITEMS of GOLDSTAR

PLASTIC-DIP ONLY

ITEM NO	TEST ITEM	TEST CONDITION	QUALITY APPROVAL				QUALITY CONFORMANCE			
			TEST FREQ	S/S	LTPD	# of ACC.	TEST FREQ	S/S	LTPD	# of ACC.
1	Visual Inspection	Outgoing Visual Specification		—	—	—	Every Lot		AQL 0.065%	0
2	Electrical Test (DC/AC)	Outgoing Test Specification		—	—	—	Every Lot		AQL 0.04%	0
3	Dimension	Lead Thickness	Every Lot	5	—	0	Every Lot	1	—	0
4	Dimension	All Dimension	Every Week	5	—	0	Every Week	1	—	0
5	Packaging Inspection	Outgoing Packaging Specification		—	—	—	Every Lot	All	—	0
6	High Temperature Operating Life Test	Ta=125°C, t=1000 HRS Vcc=5V	Every 3 Months	77	5	1	Every Week	38	10	1
7	High Temperature Storage Test	Ta=150°C, t=1000 HRS	Every 3 Months	38	10	1		—	—	—
8	Biased Humidity Test	Ta=85°C, 35% RH Vcc=5V, t=1000HRS	Every 3 Months	38	10	1	Every Week	38	10	1
9	Pressure Pot	Ta=121°C, 30 PSIG 100% RH, 100 HRS	Every 3 Months	38	10	1	Every Week	25	15	0
10	Temperature Cycle Test	-65°C, 25°C, 150°C 10 Min, 5 Min, 10 Min 200 Cycle	Every 3 Months	38	10	1	Every Week	22	10	0
11	Lead Integrity	3 X, 90 Arcs 5 Units	Every 3 Months	15	15	0		—	—	—
12	Solderability	Solder Temp 240~5°C, Steam Aging 1 HRS Flux 6 sec, Solder 5 sec	2 Times / Week	22	10	0	2 Times / Week	22	10	0
13	Resistance to Solvents		Every Lot	15	15	0	Every Lot	15	15	0
14	Electro Static Discharge	MIL-STD-883C METHOD 3015	Every Lot	22	10	0	Every Lot	15	15	0

4. SUMMARY

This report has presented quality assurance system and reliability test on GoldStar devices. According to the reliability test results and actual experimental data of operating life test, it is concluded that GoldStar devices are high quality devices and the incoming failure rate is expected to be less than 0.04%.

5. HANDLING AND STORAGE INSTRUCTION

5.1 HANDLING PRECAUTIONS

For all devices, the following practices should be observed for protection against high electro static discharges.

5.1.1 Device leads should be in contact with a conductive material except when being tested or in actual operation.

5.1.2 Conductive parts tools, fixtures, soldering irons and handling equipment should be grounded to handle the devices.

5.1.3 Devices should not be inserted into or removed from test stations unless the power is off.

5.1.4 Neither should signals be applied to the input while the device power supply is in an off condition.

5.1.5 Operators should use grounded wrist straps and work conductive surfaces should be also grounded.

5.2 STORAGING PRECAUTIONS

There are several basic requirements in case of long term storage for semiconductor devices.

5.2.1 Store the devices in a covered or sealed antistatic container.

5.2.2 Store the devices in an environment of no more than 60% relative humidity.

5.2.3 Store the devices in a inert atmosphere not exceeding +125°C or no more than -55°C.

5.2.4 Physical force is not permitted on any leads or plastic body when the devices are stored for prevention damage of device.

	DATA SHEET INDEX	
	QUALITY ASSURANCE MANUAL	
1.	TV APPLICATION	
2.	VCR APPLICATION	
3.	AUDIO APPLICATION	
4.	TELECOM APPLICATION	
5.	REMOTE CONTROL APPLICATION	
6.	INDUSTRY APPLICATION	
	GOLDSTAR SEMICONDUCTOR SALES NETWORK	

GL1130

VERTICAL DEFLECTION OUTPUT CIRCUIT FOR COLOR TV SETS

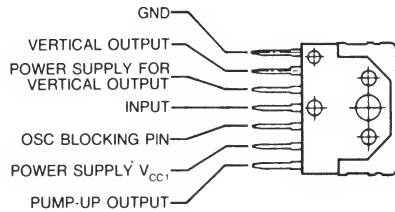
Description

The GL1130 is monolithic linear IC designed for small aperture color TV vertical deflection output and has such features as greatly reduced number of external parts and low power dissipation. The GL1130/1131 can be used in conjunction with the GL3320 for video chroma deflection use and the GL1150/GL1151 for display use to form a stable and compact vertical output deflection circuit.

Features

- High output
- On-chip pump-up circuit and low power dissipation
- Minimum number of external parts required
- High ESD Characteristic (about 20 kV)

Pin Configuration



Maximum Ratings at $T_A = 25^\circ\text{C}$

Maximum Supply Voltage	$V_{6\text{max}}$	30	V
	$V_{3\text{max}}$	60	V
Deflection Output Current	$I_{2\text{max}}$	± 1.3	Ap-0
Allowable Power Dissipation	$P_{d\text{max}}$	4.5	W
Operating Temperature	T_{OPR}	-20 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 to +125	$^\circ\text{C}$

Operating Conditions at $T_A = 25^\circ\text{C}$

Recommended Supply Voltage	V_6	24	V
Operating Voltage Range	V_6	18 to 27	V
Deflection Output Current	$I_{2\text{p-p}}$	up to 1.5	Ap-p

Operating Characteristics at $T_A = 25^\circ\text{C}$, $V_{\text{CC}} = 24.0\text{V}$

PARAMETER	MIN	TYP	MAX	UNIT
Output Transistor Saturation Voltage (1)		0.5	1.0	V
Output Transistor Saturation Voltage (2)		1.8	2.6	V
Pin 7 Saturation Voltage (1)			1.5	V
Pin 7 Saturation Voltage (2)		0.8	1.6	V
Quiescent Current	8.0	11.5	24.0	mA
Middle-Point Voltage		11		V

GL1150 / 1151

SYNC. DEFLECTION CIRCUIT FOR CRT DISPLAY

Description

The GL1150/1151 are sync. deflection circuit IC dedicated to CRT display use. They can be connected to the GL1130/1131(for vertical output use) to form a sync. deflection circuit that meets every requirement for CRT display use. So far, IC's for color TV use have been applied to the sync. deflection circuit for CRT display use and general-purpose IC's such as one-shot multivibrator, inverter and a lot of transistors have been used to form the peripherals such as sync input interface, horizontal phase shifter.

The GL1150/1151 contain these peripherals on chip and adopt a stable circuit for horizontal oscillation from 15kHz to 100kHz aiming at improving the characteristics required for CRT display use.

Features

- The Horizontal Oscillation Frequency can be Adjusted Stably from 15kHz to 100kHz.
- The Horizontal Display can be Shifted Right/Left.
- The Horizontal/Vertical Sync Input can be Used Intact Regardless of the Difference in Pulse Polarity and Pulse Width
- The AFC Feedback Sawtooth Wave can be Obtained by Simply Applying a Flyback Pulse to the IC as a Trigger Pulse.
- Any Duty of the Horizontal Pulse can be Set.
- Good Linearity Because DC Bias at Vertical Output Stage is Subjected to Sampling Control Within Retrace Time.
- Vertical Pull-In Range 20 Hz Permits Non-Adjusting at Vertical Sync 50Hz/60Hz in GL1151.

On-chip Functions

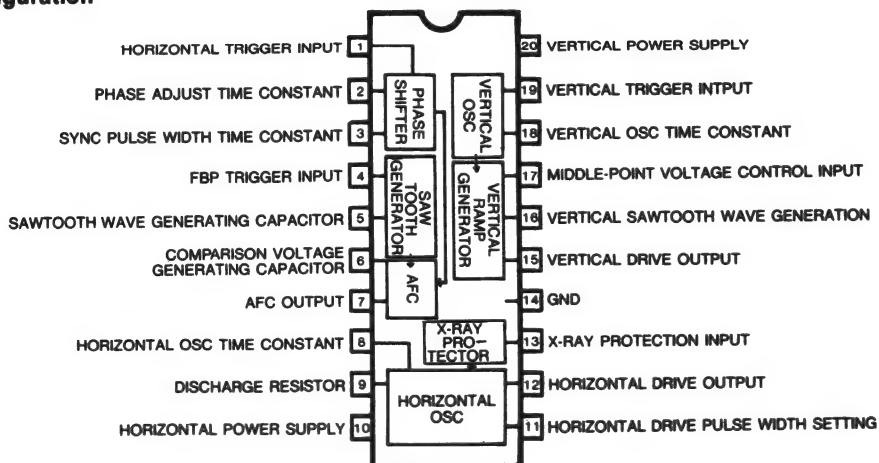
[Horizontal Block]

- AFC
- Horizontal OSC
- X-ray Protector
- Horizontal Phase Shifter
- AFC Sawtooth Wave Generator
- Horizontal Pulse Duty Setting

[Vertical Block]

- Vertical OSC
- Vertical Sawtooth Wave Generator
- Sampling Type DC Voltage Control

Pin Configuration



Absolute Maximum Ratings at $T_A=25^{\circ}\text{C}$

			unit
Maximum Supply Voltage	$V_{10,20\text{max}}$	14	V
Allowable Power Dissipation	$P_{D\text{max}}$ $T_A \leq 65^{\circ}\text{C}$	780	mW
Operating Temperature	T_{opg}	-20 to +85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}\text{C}$

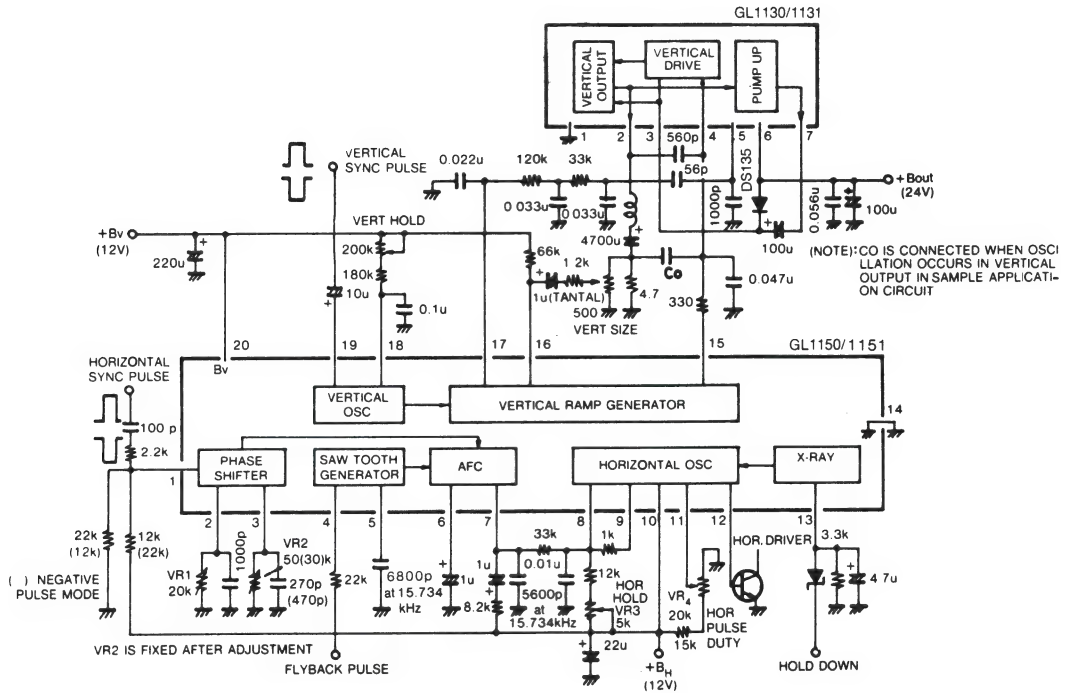
Operating Conditions at $T_A=25^{\circ}\text{C}$

			unit
Operating Voltage Range	$V_{10,20\text{-opg}}$	9.0 to 13.5	V
Recommended Supply Voltage	$V_{10,20}$	12.0	V

Operating Characteristics at $T_A=25^{\circ}\text{C}$, $V_{CC10}=V_{CC20}=12\text{V}$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{10}	V_{CC10} Current Dissipation		12		30	mA
I_{20}	V_{CC20} Current Dissipation		5		12	mA
V_{P-in}	Vertical Frequency Pull-in Range	Vertical Sync				
		60Hz				
		GL150	10.0		12.0	Hz
		GL1151	19.0		23.0	Hz
f_V	Vertical Free-Running Frequency	f_V center 55Hz	50		60	Hz
Δf_{VV}	Increased/Reduced Voltage Characteristic of Vertical Frequency	$V_{20}=12 \pm 1\text{V}$ 55Hz at 12V	-0.5		0.5	Hz
V_{MC}	Middle-point Voltage Control Threshold Level		3.8		4.4	V
V_{OUS}	Vertical OSC Start Voltage			4		V
G_V	Vertical Driver Amplification Factor		12		18	dB
I_{AFC}	Horizontal AFC DC Loop Current		± 1.0		± 1.9	mA
f_H	Horizontal Free-Running Frequency	f_H center 15.734kHz	-750		750	Hz
V_{OSH}	Horizontal OSC Start Voltage			4		V
Δf_{HV}	Increased/Reduced Voltage Characteristic of Horizontal Frequency	$V_{10}=12 \pm 1\text{V}$ 15.734kHz at 12V	-50		50	Hz
V4	Comparison Wave Generation Input Operating Voltage		0.6		0.9	V
V13	Holddown Operation Start Voltage		0.5		0.8	V
I12	Horizontal Drive Current		6.0		12.0	mA

Sample Application Circuit: 14" Color Monitor/ $f_V=60\text{Hz}$, $f_H=15.734\text{kHz}$



GL3101A

CTV VIDEO IF SYSTEM

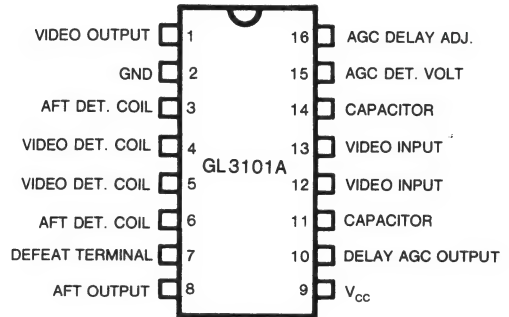
Description

The GL3101A is a bipolar monolithic integrated circuit designed for color television receivers. This IC has all function including video IF amplifier, quasi-synchronous detector, AFT with defeat terminal, video amplifier, delay IF AGC amplifier, RF AGC, and noise canceller.

Feature

- 920 KHz Beats and Cross-Color Reduced
- Improved DG and DP
- Minimized External Components
- Minimum Level of Forward AGC Output
Voltage is Changeable by External Resistors.

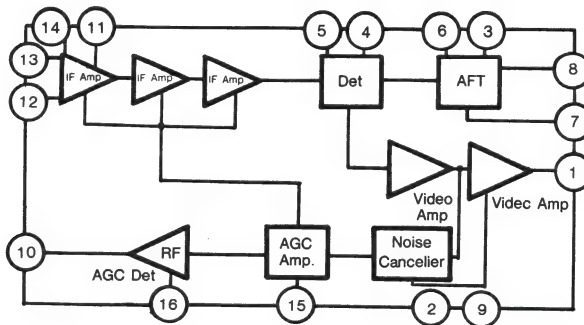
Pin Configuration



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Power Supply	V_{CC}	15	V
Power Dissipation	P_d	745	mW
Operating Temperature	T_{OPR}	$-20 \sim +65$	$^\circ\text{C}$
Storage Temperature	T_{STG}	$-55 \sim +125$	$^\circ\text{C}$
Mean Level of Maximum Output Current at Pin-1	I_O	4.2	mA

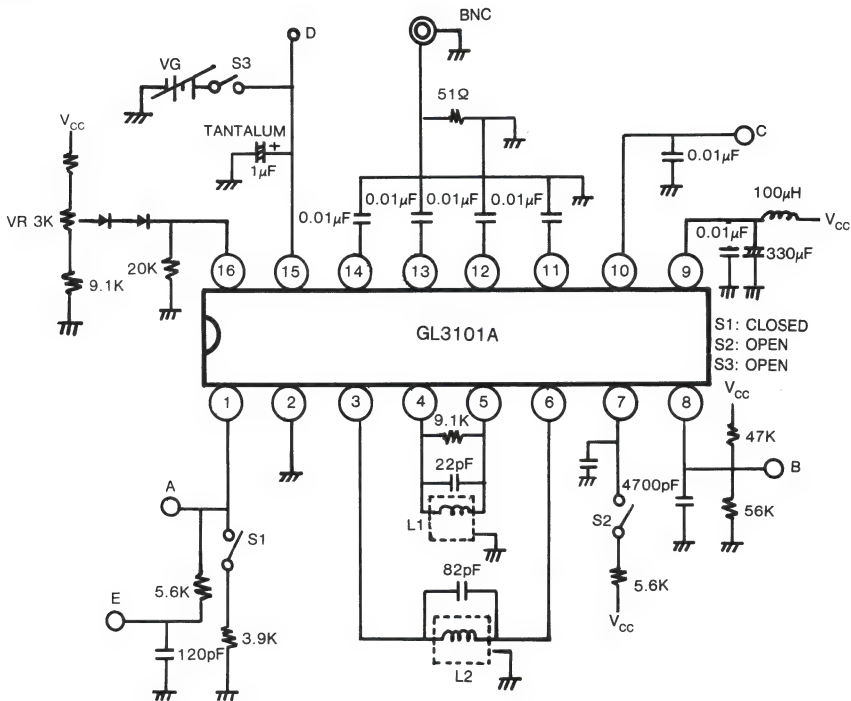
Block Diagram



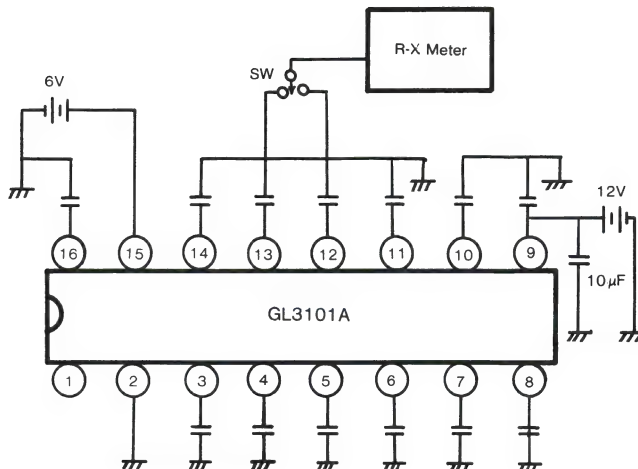
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
SUPPLY CURRENT 1	I_1	VIF=0	27.0	39.0	51.3	mA
SUPPLY CURRENT 2	I_2	VIF=80 dB μ	27.0	40.0	51.3	mA
INPUT SENSITIVITY	V_{in}	The Input Voltage at Which the Video Output Voltage Reduced 1dB	35	40	45	dB μ
Video Bandwidth	f_c	The Frequency at Which the Video Output Voltage Reduced 3dB	6.0	7.5	—	MHz
Maximum Input Voltage	$V_{in(max)}$	The Input Voltage at Which the Video Output Voltage Varies Within 5%	93	98	—	V
Video Output Level	V_{out}	$m=0.875$	1.98	2.32	2.65	V _{p-p}
Sync. Tip Voltage	$V_{sync.}$		5.20	5.60	5.90	V
Noise Canceller Starting Voltage	V_{nc}		1.20	1.50	1.80	V
Differential Gain	DG	$m=0.876$; 5% Chroma Added; DSB Signal Input	—	8	12	%
Differential Phase	DP	$m=0.875$; 5% Chroma Added: DSB Signal Input	—	2.5	6	Deg.
AGC Charging time Constant	T_C	Input Signal Modulated with Square Wave	—	350	500	μs
AGC Discharging Time Constant	T_O	Input Signal Modulated with Square Wave	—	14	28	mS
Vertical Internal Distortion	V_{ver}		—	50	100	mV _{p-p}
Minimum RF AGC Voltage	$V_{tr(min)}$	$V_{1F}=85$ dB μ	—	—	1.0	V
Maximum RF AGC Voltage	$V_{tr(max)}$	$V_{2F}=65$ dB μ	11.0	11.70	11.95	V
Signal-to-Noise Ratio	SNR	VIF=80 dB μ ; CW Input Signal	49	52	—	dB
Noise Limited Sensitivity	V_{SN}		—	48	52	dB
PIF Input Resistance at Pin-12	R_{i12}	Test Circuit 2	—	1.80	—	K Ω
PIF Input Resistance at Pin-13	R_{i13}	Test Circuit 2	—	1.80	—	K Ω
PIF Input Capacitance at Pin-12	C_{i12}		—	3.0	—	pF
PIF Output Capacitance at Pin-13	C_{i13}		—	3.0	—	pF
Video Output Resistance	R_{out}		—	3.0	—	Ω
AFT Quiescent Voltage	V_{M1}	No Input Signal	5.25	6.52	7.55	V
DC Output Voltage at AFT	V_{M2}	Defeat On	6.45	6.52	6.59	V
AFT Detection Sensitivity		IF Sweep Signal Input	—	180	230	MHz
AFT Hold Range (High)	F_{AH}	IF Sweep Signal Input	1.0	1.8	3.5	MHz
AFT Hold Range (Low)	F_{AL}	IF Sweep Signal Input	-3.5	-1.8	-1.0	MHz
Maximum AFT Voltage	$V_{A(max)}$	IF Sweep Signal Input	11.0	11.6	11.95	V
Minimum AFT Voltage	$V_{A(min)}$	IF Sweep Signal Input	0.05	0.30	1.0	V
Time Constant at AGC Lock Prevention	L		110	220	440	μSec
Gain Attenuation	V_{AT}	RF Stage Gain of Tuner Attenuated	0	2	5	dB
Thermal Deviation of Delay Point	DD_{LT}	$T_A = -20^\circ\text{C}$ to $+65^\circ\text{C}$	-6	0	6	dB
Thermal Deviation of Video output	DV_{OT}	$T_A = -20^\circ\text{C}$ to $+65^\circ\text{C}$	-5	0	5	%

Test Circuit 1



Test Circuit 2



GL3120

VIF+SIF CIRCUIT for TV Sets, VTR's

Description

The GL3120 is an IC containing the VIF section and SIF section on a single chip in the DIP30S package of shrink type. Since the GL3120 is capable of performing video detection and sound detection independently or simultaneously, it can be applied to various sets from popular type to high-grade type according to the designer's policy.

Function

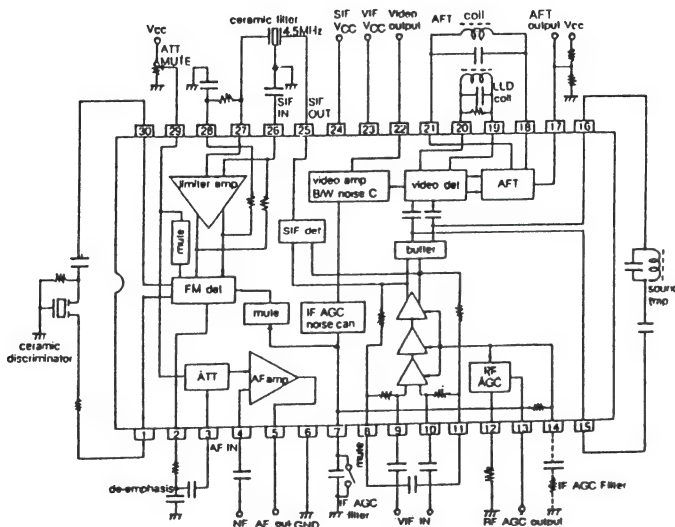
VIF section: VIF amp, video detector, peak IF AGC, B/W noise canceler, RF AGC, AFT, SIF detector

SIF section: SIF limiter amp, FM detector, DC attenuator, AF driver

Feature

- High Gain VIF Amp Requiring No Preamp
- High AGC Speed
- Provides Wide-Band Detection Characteristics and Meets Sound MPX Demodulation Requirements Because of FM Detection Being quadrature Detection.
- Possible to Use Sound REC Pin (Pin 2), Aux Pin (Pin 3)
- Possible to Mute Video, Sound for VTR:
Pin 7 GND: Muting of Both Video and Sound
Pin 29 GND: Muting of Sound Only

Block Diagram

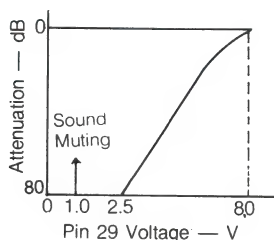


Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, $f_p = 58.75\text{MHz}$, $f_s = 54.25\text{MHz}$ (VIF), $f_o = 4.5\text{MHz}$ (SIF)

(VIF Section)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Total circuit current	$I_{23} + I_{24}$	dc	59	74	98	mA
Maximum RF AGC voltage	V_{13H}	dc	8.5	8.9	9.2	V
Minimum RF AGC voltage	V_{13L}	dc		0	0.5	V
Quiescent video output voltage	V_{22}	dc	5.6	6.1	6.6	V
Quiescent AFT output voltage	V_{17}	dc	4.5	6.5	7.5	V
Input sensitivity	v_i	$f_m = 400\text{Hz} \text{ --- } 40\%\text{AM}$, $v_o = 0.8\text{Vpp}$	30	36	42	$\text{dB}\mu$
AGC voltage	GR	$f_m = 15\text{kHz} \text{ --- } 78\%\text{AM}$, $v_o = \pm 1\text{dB}$	60	74	100	dB
Maximum allowable input voltage	$v_i \text{ max}$	$f_m = 15\text{kHz} \text{ --- } 78\%\text{AM}$, $v_o = \pm 1\text{dB}$	100	500	900	mVrms
Video output amplitude	v_{o22}	$v_i = 10^*$, $f_m = 15\text{kHz} \text{ --- } 78\%\text{AM}$	1.9	2.2	2.5	Vpp
Output S/N	S/N	$v_i = 10^*$, CW	48	54		dB
Carrier leak	CL	$v_i = 100^*$, $f_m = 15\text{kHz} \text{ --- } 78\%\text{AM}$	50	57		dB
Maximum AFT voltage	V_{17H}	$v_i = 10^*$, SWEEP	11.0	11.5	12.0	V
Minimum AFT voltage	V_{17L}	$v_i = 10^*$, SWEEP	0	0.4	1.0	V
AFT Detection sensitivity	sf	$v_i = 10^*$, SWEEP	70	100	140	mV/kHz
White noise threshold voltage	V_{WTH}	$v_i = 10^*$, SWEEP	6.4	6.8	7.2	V
White noise clamp level	V_{WCL}	$v_i = 1^*$, SWEEP	4.2	4.6	5.0	V
Black noise threshold voltage	V_{BTH}	$v_i = 10^*$, SWEEP	2.1	2.4	2.7	V
Black noise clamp level	V_{BCL}	$v_i = 10^*$, SWEEP	3.8	4.2	4.6	V
SIF output signal voltage	V_{o25}	P/S = 20dB	40	60	100	mVrms
Frequency characteristic	f_c	—3dB	6	8	15	MHz
Differential gain	DG	$v_i = 10^*$, —87.5%, video-mode	0	4	10	%
Differential phase	DP	$v_i = 10^*$, —87.5%, video-mode	0	3	6	deg
Input resistance	r_i		1.0	1.5	2.0	$\text{k}\Omega$
Input capacitance	c_i			3.5	7.0	pF

Electronic volume control characteristic



(SIF Section)

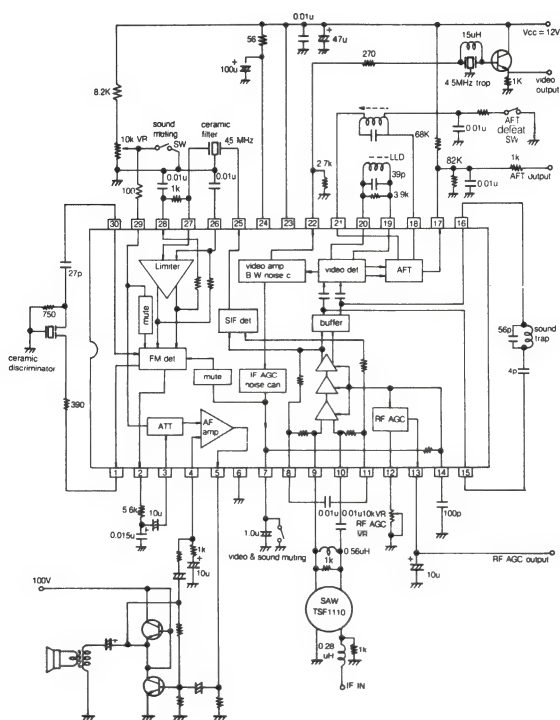
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SIF limiting sensitivity	ViLim	—3dB	0	200	400	μVrms
Detection output voltage	Vo2	$v_i = 100^*$, $f_m = 400\text{Hz}$, $\Delta f = \pm 25\text{kHz}$	450	680	850	mVrms
Total harmonic distortion	THD	$v_i = 100^*$, $f_m = 400\text{Hz}$, $\Delta f = \pm 25\text{kHz}$		0.5	1.0	%
AM rejection	AMR	$v_i = 100^*$, $f_m = 400\text{Hz}$, $\Delta f = \pm 25\text{kHz}$, —30%AM	50	60	100	dB
DCVR maximum attenuation	ATT	$v_i = 200^*$, $f = 400\text{Hz}$	70	80		dB
AF amp gain	$V_{G_{AF}}$	$v_i = 100^*$, $f = 400\text{Hz}$	18	20	22	dB
AF amp output voltage	vo5	THD = 10%, $f = 400\text{Hz}$	3	4		Vrms

(Note)

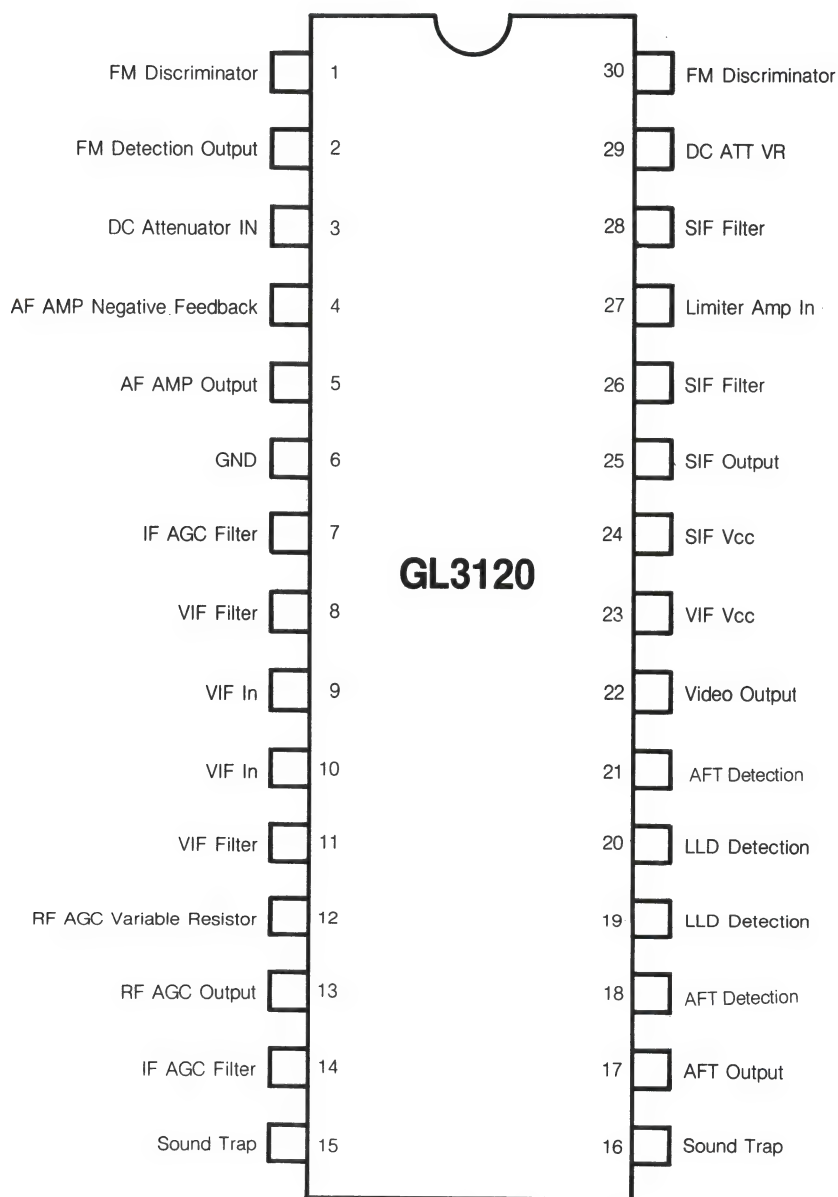
- FM detector input impedance (pin 30): $2k\ \Omega$ (typ.)

*: mVrms

Typical Application



Pin Configuration



GL3201A/GL3202

TV SOUND IF SYSTEM

Features

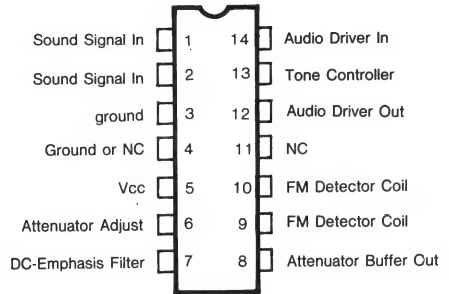
- Electronic attenuator replaces conventional volume control...range>60 dB
- Differential peak detector requires one single tuned coil
- Internal Zener diode regulated supply
- Inherent high stability
- Excellent AM rejection at 4.5MHz
- Low harmonic distortion
- High sensitivity 180 μ V limiting at 4.5MHz
- Audio drive capability...6.0mA p-p
- Undistorted audio output voltage...7V p-p
- Minimum undersirable output signal at Maximum attenuation

Description

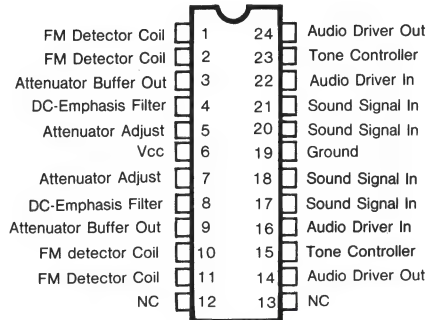
...a versatile monolithic integrated circuit incorporating a multi stage IF amplifier limiter, an FM, an electronic attenuator, a zener diode regulated power supply and an audio amplifier driver.

...designed for television sound system applications. The GL3202 is dual of GL3201A. Because Vcc and Ground is common, all the parameter of GL3202 is same as GL3201A except Icc, which is 2 times higher than that of GL3201A.

Pin Configuration

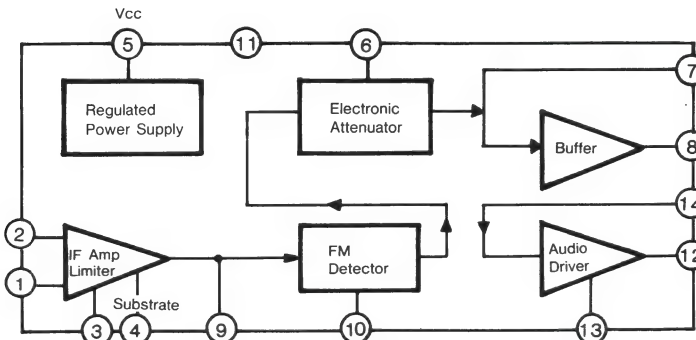


1) GL3201A



2) GL3202

Block Diagram



Maximum Ratings (T_A = 25°C)

• Input Signal Voltage (Pins 1&2)	V _{in}	±3	V
• Power Supply Current (Pin 5)	I _S	50	mA
• Power Dissipation	P _D	625	mW
• Storage Temperature	T _{STG}	-65~+150	°C
• Operating Temperature	T _{OPR}	-20~+85	°C

Dynamic Characteristics (V_{CC} = 24Vdc, T_A = 25°C)

If Amplifier

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Limiting Voltage (at-3dB Point)		V _{i(lim)}	f _o = 4.5MHz, f _m = 400Hz Deviation = ±25KHz	—	180	400	μV
AM Rejection		AMR	f _o = 4.5MHz, Amplitude Modulation = 30%	40	55	—	dB
Input Impedance	Input Resistance	R _i (IF)	Measured between Pin No. 1&2 f = 4.5MHz	—	17	—	KΩ
	Input Capacitance	C _i (IF)		—	4	—	pF
Output Impedance	Output Resistance	R _o (IF)	Measured between Pin No. 9 & GND f = 4.5MHz	—	3.25	—	KΩ
	Output Capacitance	C _o (IF)		—	7.5	—	pF

Detector

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Recovered Audio Output Voltage		V _o (AF)	f _o = 4.5MHz, V _{in} = 0.1V	0.5	0.8	—	V _(rms)
Total Harmonic Distortion		THD	f = ±25KHz, f _m = 400Hz	—	0.9	2	%
Output Resistance	Pin 7	R _o		—	7.5	—	KΩ
	Pin 8			—	250	—	Ω

Attenuator

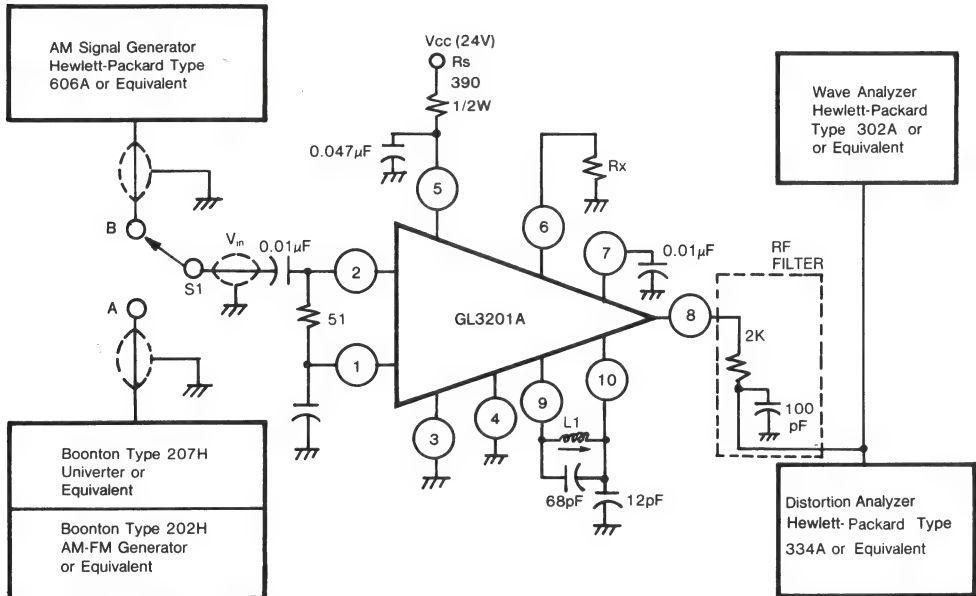
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
MAX. Attenuation	—	DC Volume Control = ∞	60	—	—	dB
MAX. "Play-through" Voltage	—	DC Volume Control = ∞	—	0.03	1	mV

Audio Amplifier

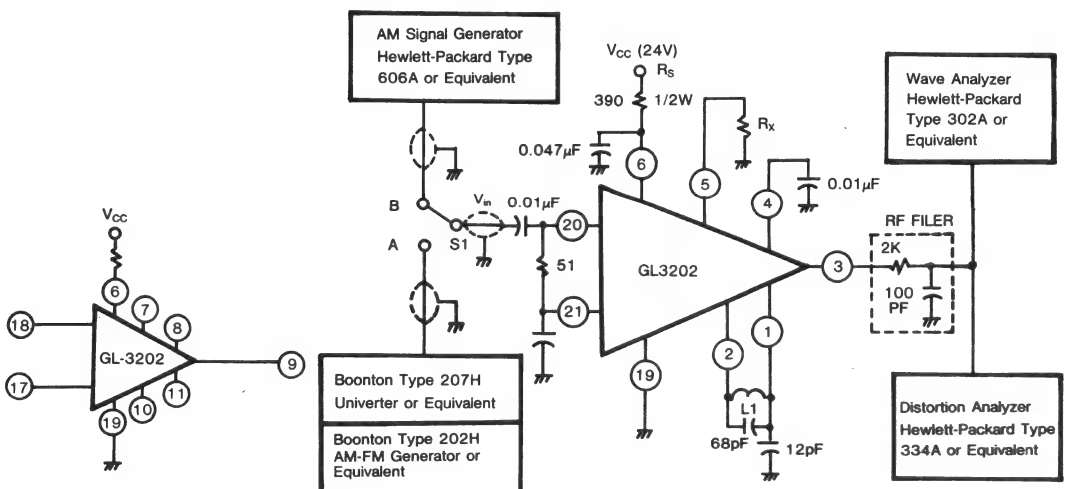
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage Gain	A(AF)	V _{in} = 0.1V _(mm) , f = 400Hz	17.5	20.5	—	dB
Total Harmonic Distortion	THD(AF)	V _o = 2V _(mm) , f = 400Hz	—	1.5	—	%
Output Voltage		THD = 5%, f = 400Hz	2	3.5	—	V _(rms)
Input Resistance	R _i (AF)	f = 400Hz	—	70	—	KΩ
Output Resistance	R _o (AF)	f = 400Hz	—	270	—	Ω

* Test Circuit For $V_i(lim)$, AMR, VO(AF), THD, ATTENUATION

1) GL3201A

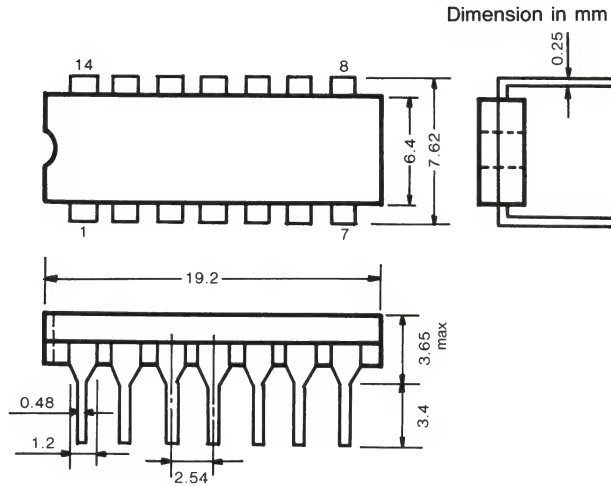


2) GL3202

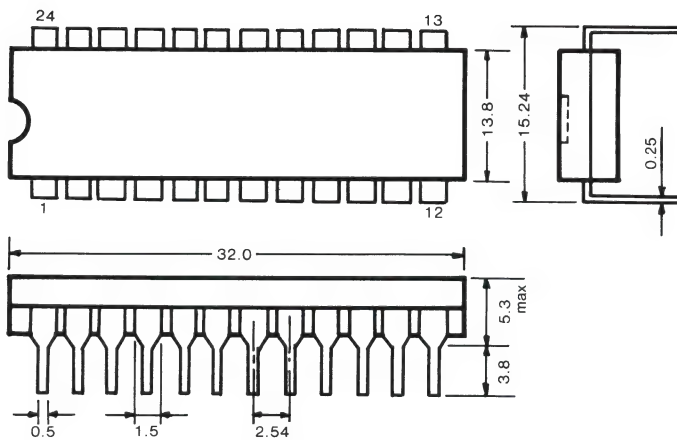


Package Dimentionns

1) GL3201A



2) GL3202



GL 3301

CTV VIDEO CHROMA SYSTEM

Description

GL3301 is a bipolar monolithic integrated circuit designed for C-TV Luminance-Chroma system with auto flesh. This IC has all functions including auto flesh control, color average, chroma amp, color sync, color demodulation, sharpness emitter peaking, contrast control, pedestal clamp, brightness control, blanking video output circuit and over saturation preventer.

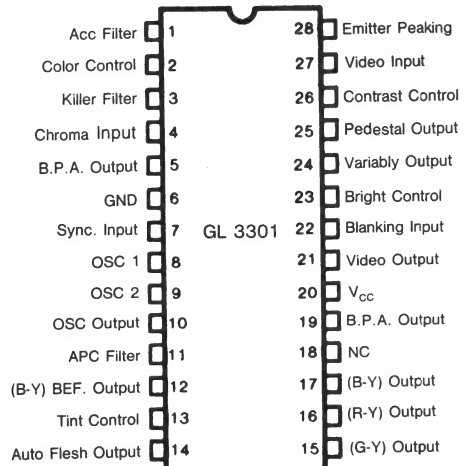
Feature

- **Low Cost and Excellent Characteristics for VTR Monitors**
- **Demodulation Phase is Adjustable by One External Capacitor (90° Demond., Without the Capacitor).**
- **VCO's Output Frequency is Adjustable by a Variable Resistor**
- **Voltage Gain of Auto Flesh Control is Adjustable Externally.**

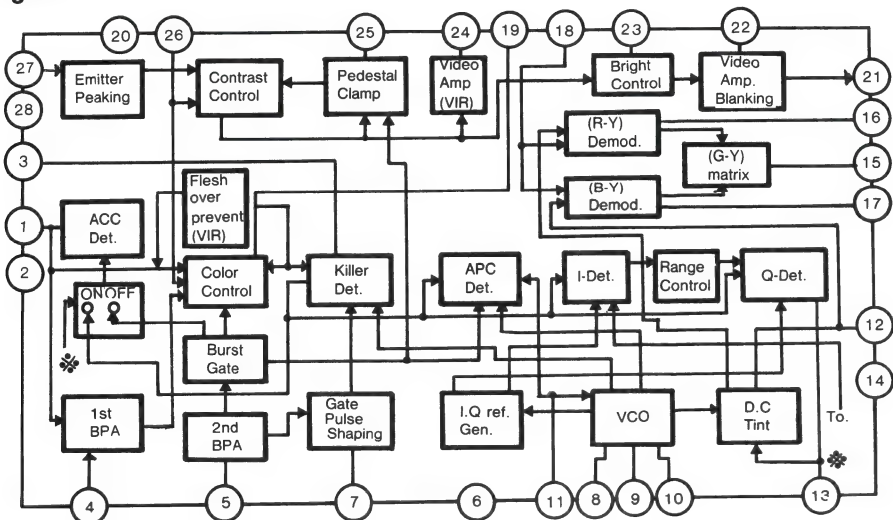
Absolute Maximum Ratings

Supply Voltage	V_{CC}	15	V
Power Dissipation ($T_A=70^\circ\text{C}$)	P_d	850	mW
Operating Temperature	T_{OPR}	$-20\sim+70$	$^\circ\text{C}$
Storage Temperature	T_{STG}	$-55\sim+125$	$^\circ\text{C}$

Pin Configuration



Block Diagram



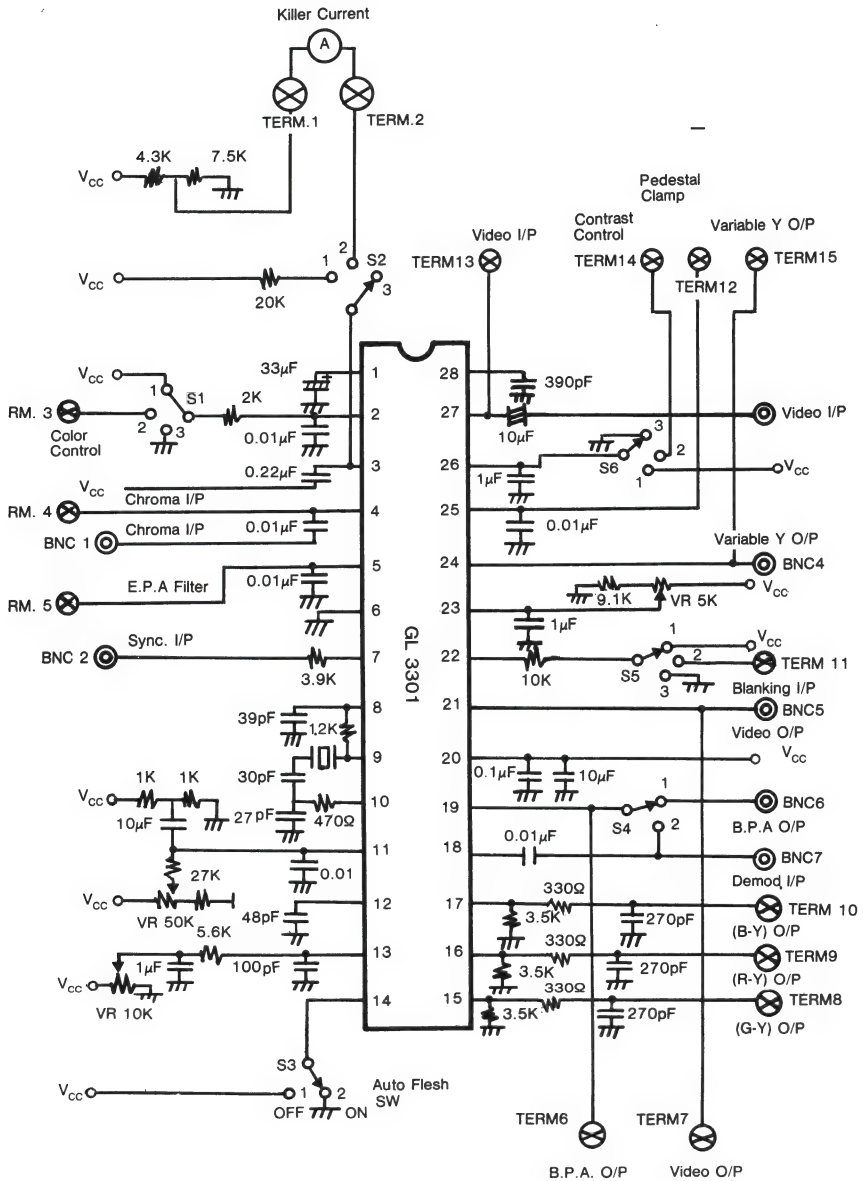
Electrical Characteristics; ($T_A=25^{\circ}\text{C}$, $V_{CC}=12\text{V}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
D.C Voltage Difference Between any demod. output	E17 – E16	Voltage at Pin 17 –Voltage at Pin 16	–0.3	0	0.3	V
D.C Voltage Difference Between any demod. output	E16 – E15	Voltage at Pin 16 –Voltage at Pin 15	–0.3	0	0.3	V
D.C Voltage Difference Between any demod. output	E15 – E17	Voltage at Pin 15 –Voltage at Pin 17	–0.3	0	0.3	V
Blanked Output Voltage	V_{BO}	S1=1,S2=3,S3=2,S4=2,S5=1, S6=1,V23=8.9V	10.1	11.1	—	V
Blanking Input Level	V_{BI}	S1=1,S2=3,S3=2,S4=2,S5=2, S6=1	0.6	0.7	0.8	V
Total Consumption Current	I_{CC}	S1=2,S2=3,S3=2,S4=2,S5=3, S6=2 Sync. in, No Input	35	50	62	mA
Tint Center Voltage	V_{TI}	S1=2,S2=3,S3=1,S4=2,S5=3,S6=1 Sync. in, Chroma Input: Burst=100mV _{p-p} /100mV _{p-p} , Pin12 Open	3.6	4.0	4.4	V
Pedestal Clamp Voltage	V_{25}	S1=1,S2=3,S3=2,S4=2,S5=3,S6=1	9.2	9.9	10.3	V
Max. Chroma output	$E_{C\max}$	S1=1,S2=3,S3=1,S4=1,S5=3,S6=1 Sync. in, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	0.50	0.65	0.80	V _{p-p}
ACC Range (1)	E_{A1}	S1=1,S2=3,S3=1,S4=1,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=10mV _{p-p} /10mV _{p-p}	0.4	0.53	0.67	V _{p-p}
ACC Range (2)	E_{A2}	S1=1,S2=3,S3=1,S4=1,S5=3,S6=1 Sync. Inc, Chroma Input: Burst/Chroma=200mV _{p-p} /200mV _{p-p}	0.5	0.66	0.85	V _{p-p}
Killer Current (Color)	I_{KC}	S1=1,S2=2,S3=1,S4=1,S5=3,S6=1 Sync. In, Chroma Output: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	60	150	200	μA
Killer Current (B/W)	I_{KB}	S1=1,S2=2,S3=1,S4=1,S5=3,S6=1 Sync. In, No I/P	–46	–25	–4	μA
Killed chroma output voltage	E_{KL}	S1=1,S2=1,S3=1,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	—	—	30	mV _(rms)
Min Gain Chroma O/P Voltage	E_{CL}	S1=3,S2=3,S3=1,S4=1,S5=3,S6=1 Sync. In, Chroma Input: V2=4V Burst/Chroma=100mV _{p-p} /100mV _{p-p}	—	—	30	mV _(rms)
Killer Sensitivity	E_K	S1=1,S2=3,S3=1,S4=1,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	–55	–40	–30	dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Min. Chroma Output	$E_{C \min}$	S1=1,S2=3,S3=1,S4=1,S5=3,S6=3 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	—	0.19	—	V _{p-p}
Contrast Range of Chroma Output	R_C	20 log ($E_{C \min}/E_{C \max}$)	-13.6	-11.1	-10.1	dB
A.P.C Pull-In Range (+)	f_{p+}	S1=1,S2=S3=1,S4=1,S5=3,S6=3 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	-300	—	—	Hz
A.P.C Pull-In Range (-)	f_{p-}	S1=1,S2=S3=1,S4=1,S5=3,S6=3 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	—	—	300	Hz
OSC Output Level	V_{osc}	S1=1,S2=3,S3=1,S4=1,S5=3,S6=1 No Input:	1.2	1.8	2.4	V _{p-p}
OSC. Free Run Frequency	f_{osc}	S1=1,S2=3,S3=1,S4=1,S5=3,S6=1 No Input:	—	—	±250	Hz
Detection Sensitivity of APC Det.	U	$U = \frac{f_p}{\sqrt{2m} \times \frac{180}{\pi} \times \beta}$ m=0.042	—	24	—	mV/Deg.
VCO. Controlling Sensitivity	β	S1=1,S2=3,S3=1,S4=1,S5=3,S6=1	—	1.53	—	Hz/mV
Stability of VCO. Freq. vs Supply Voltage	f_{ov}	S1=1,S2=3,S3=1,S4=1,S5=3,S6=1 V _{CC} =12V±1V	0	10	20	Hz
Tint Control Range (1)	R_{T1}	S1=1,S2=3,S3=1,S4=2,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p} V13=1V, Pin 12 Open	-69	-55	-41	Deg.
Tint Control Range (2)	R_{T2}	S1=1,S2=3,S3=1,S4=2,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p} V13=7V, Pin 12 Open	41	60	74	Deg.
Max. (B-Y) Output	$E_{B \max}$	S1=1,S2=3,S3=1,S4=1,S5=3,S6=1 Demo. I/P (BNC 7): Sine Wave with Amplitude=1.2V _{p-p} & Freq.=3578545±5Hz	4.5	6.2	—	V _{p-p}
Demod. Conversion Gain	E_{R-Y}	S1=1,S2=3,S3=1,S4=2,S5=3,S6=1 Demod. I/P (BNC 7): Sine Wave with Amplitude=0.2V _{p-p} & Freq.=3578545 ± 5Hz	6.5	7.8	—	
Matrix Ratio (1)	$\frac{E_{R-Y}}{E_{B-Y}}$	S1=1,S2=3,S3=1,S4=2,S5=3,S6=1 Demod. I/P (BNC 7): Sine Wave with Amplitude=0.2V _{p-p} & Freq.=3578545±5Hz	0.7	0.8	0.95	

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Matrix Ratio (2)	$\frac{E_{G-Y}}{E_{B-Y}}$	S1=1,S2=3,S3=1,S4=2,S5=3,S6=1 Demod. I/P (BNC 7): Sine Wave with Amplitude=0.2V _{p-p} & Freq.=3578545±5Hz	0.22	0.30	0.38	
Relative Demod. output Phase of R-Y to B-Y	$\frac{\angle(R-Y)}{\angle(B-Y)}$	S1=3,S2=3,S3=1,S4=2,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p} Connect 33pF from Pin 12 to GND	100	115	130	Deg.
Relative Demod. output Phase of G-Y to B-Y	$\frac{\angle(G-Y)}{\angle(B-Y)}$	S1=3,S2=3,S3=1,S4=2,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p} Connect 33pF from Pin 12 to GND	240	255	270	Deg.
Residual carrier Voltage at Demod. output	θ_{car}	S1=1,S2=3,S3=1,S4=2,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	—	—	0.2	V _{p-p}
Supply Voltage Coefficient of Demod. D.C. of Voltage	$\frac{\partial V_O}{\partial V_{CC}}$	S1=1,S2=3,S3=1,S4=2,S5=3,S6=1 [Demod. O/P (V _{CC} =13.8V) – Demod. O/P (V _{CC} =10.2V)] 13.8–10.2V	—	0.5	—	V/V
Auto Flesh Control Center	P _C	S1=1,S2=3,S3=2,S4=2,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	285	295	305	Deg.
Auto Flesh Control Range	P _R	S1=1,S2=3,S3=2,S4=2,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	±30	±40	±50	Deg.
Auto Flesh Control Gain	P _G	S1=1,S2=3,S3=2,S4=2,S5=3,S6=1 Sync. In, Chroma Input: Burst/Chroma=100mV _{p-p} /100mV _{p-p}	±20	±30	±40	Deg.
Video Amp. Voltage Gain(1)	V _G	S1=1,S2=3,S3=2,S4=2,S5=3,S6=1 V23=8.9V , V26=12V Video Input: Sine Wave with Amplitude= 0.3V _{p-p} & Freq.=0.1MHz	9.2	11	12.8	
Contrast Range of Video Amp. Voltage Gain (1)	R _V	S1=1,S2=3,S3=2,S4=2,S5=3,S6=1 V23=8.9V, Video Input: Sine Wave with Amplitude=0.3V _{p-p} & Freq.=0.1MHz	–14.2	–13.2	–12.2	dB
Video Amp. freq. Response	f _C	S1=1,S2=3,S3=2,S4=2,S5=3,S6=1 V23=8.9V, Pin 23 Open	5	—	—	MHz
Peaking Ratio	R _P	S1=1,S2=3,S3=2,S4=2,S5=3,S6=1 Video O/P at f=6MHz Video O/P at f=0.1MHz	2.2	2.8	3.4	
Video Amp. Voltage Gain(2)	G _{VIR}	S1=1,S2=3,S3=2,S4=2,S5=3,S6=1 V23=8.9V Video Input: Sine Wave with Amplitude =0.3V _{p-p} & freq.=0.1MHz	3.5	4.5	5.2	

Test Circuit



GL3320

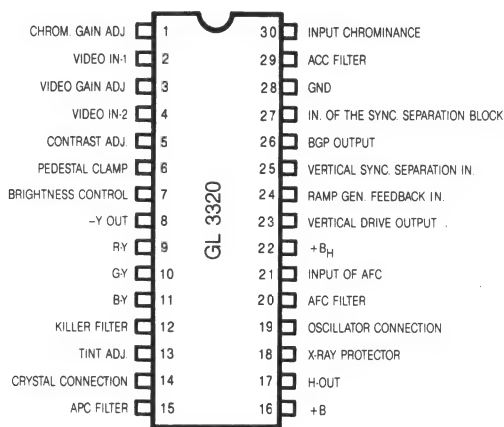
VIDEO CHROMA DEFLECTION CIRCUIT for Color TV Sets

Description

The GL 3320 are small-sized multifunctional IC's containing the "video, chroma, deflection" circuit of NTSC color TV in the DIP-30S of shrink type. Besides being small-sized, they have such features as greatly reduced number of parts and fewer adjustments required. The GL 3320 can be used in conjunction with the GL 3120 for "VIF + SIF" use to perform all color TV signal processings.

The GL 3320 containing a peak clip circuit in the video circuit is well suited for use in small-sized sets.

Pin Configuration



Features

- **Small-Size Package.**
- **Minimum Number of Parts Required.**
- **Fewer Adjustment Required (Non-adjusting of Functions Shown Below).**
 - **Chroma VCO (APC)**
 - **Horizontal OSC (H-Hold)**
 - **Vertical OSC (V-Hold).**

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Supply Voltage	V_{16}	14.0	V
Supply Current	I_{22}	15.0	mA
Power Dissipation	P_d	$T_A \leq 65^\circ\text{C}$ 1100	mW
Operating Temperature	T_{OPR}	-20 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Operating Conditions $T_A = 25^\circ\text{C}$

Supply Voltage	V_{16}	12.0	V
Supply Current	I_{22}	10.0	mA
Operating Voltage Range		9.0 to 14.0	V
Operating Current Range		8.5 to 15.0	mA

Electrical Characteristics: $T_A = 25^\circ\text{C}$, $V_{16} = 12\text{V}$, $I_{22} = 10\text{mA}$ (unless otherwise specified)

(DEFLECTION BLOCK)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supple Current of Pin 16	I_{16}		40	53	75	mA
Horizontal Supply Voltage	V_{Z22}		8.2	8.7	9.2	V
Sync. Signal Separation Input DC Level	V_{SS}		9.0	9.3	9.6	V
Vertical Free Run Frequency 1	f_{V1}			$1H/296.5$		Hz
Vert. Blanking Pulse Width	$PWVB$			$19.25/f_H$		sec
Vert. Output Pulse Width	$PWVO$			$10.25/f_H$		sec
Vert. Drive Part Voltage Gain	G_V		13	16.2	19	dB
Vert. Output Pulse Starting Voltage	V_{CDS}				4.0	V
Vert. Pull-In Operation Starting Voltage	V_{VPS}				4.0	V
Vert. Blanking Pulse Peak Value	V_{VBLK}				10.0	V
AFC DC Loop Gain	I_{AFC}		± 300	± 400	± 500	μA
Hori. Free Run Frequency	f_H	Hori. Output freq. -15,734	-70	0	130	Hz
Hori. OSC Frequency Power Supply Voltage Change	Δf_{HV}	$f_H(8V) - f_H(7V)$	-10	0	10	Hz
Hori. OSC Frequency Ambient Temperature Variation Dependence	$\Delta f/\Delta T$	$T_A = -10 \sim 60^\circ\text{C}$	-1.5		1.5	Hz/ $^\circ\text{C}$
Hori. Output Pulse Width	$PWHO$		23.5	24.5	25.5	μs
Hori. Sync Pull-In Range	f_H Pull	Deviation from 15,734Hz	+400 -500			Hz
Hori. Output Pulse Starting Voltage	V_{HPOS}				5.5	V
Hori. Free Run Frequency Aging Drift	Δf_{HT}	from 5 sec to 30 min.	-50	-10	30	Hz
Hori. Blanking Threshold Level	V_{HBLK}		11			V
Hori. Output Drive Current	$I_{H,D}$		2.0		4.5	mA
Hori. OSC Control Sensitivity	βf_H	Reference Level		236		Hz/ μA
Hold Down Operation Starting Input Voltage	$V_{H,D}$		0.55	0.65	0.75	V
Hold Down No Return Supply Voltage	$V_{H,DNR}$				4.0	V

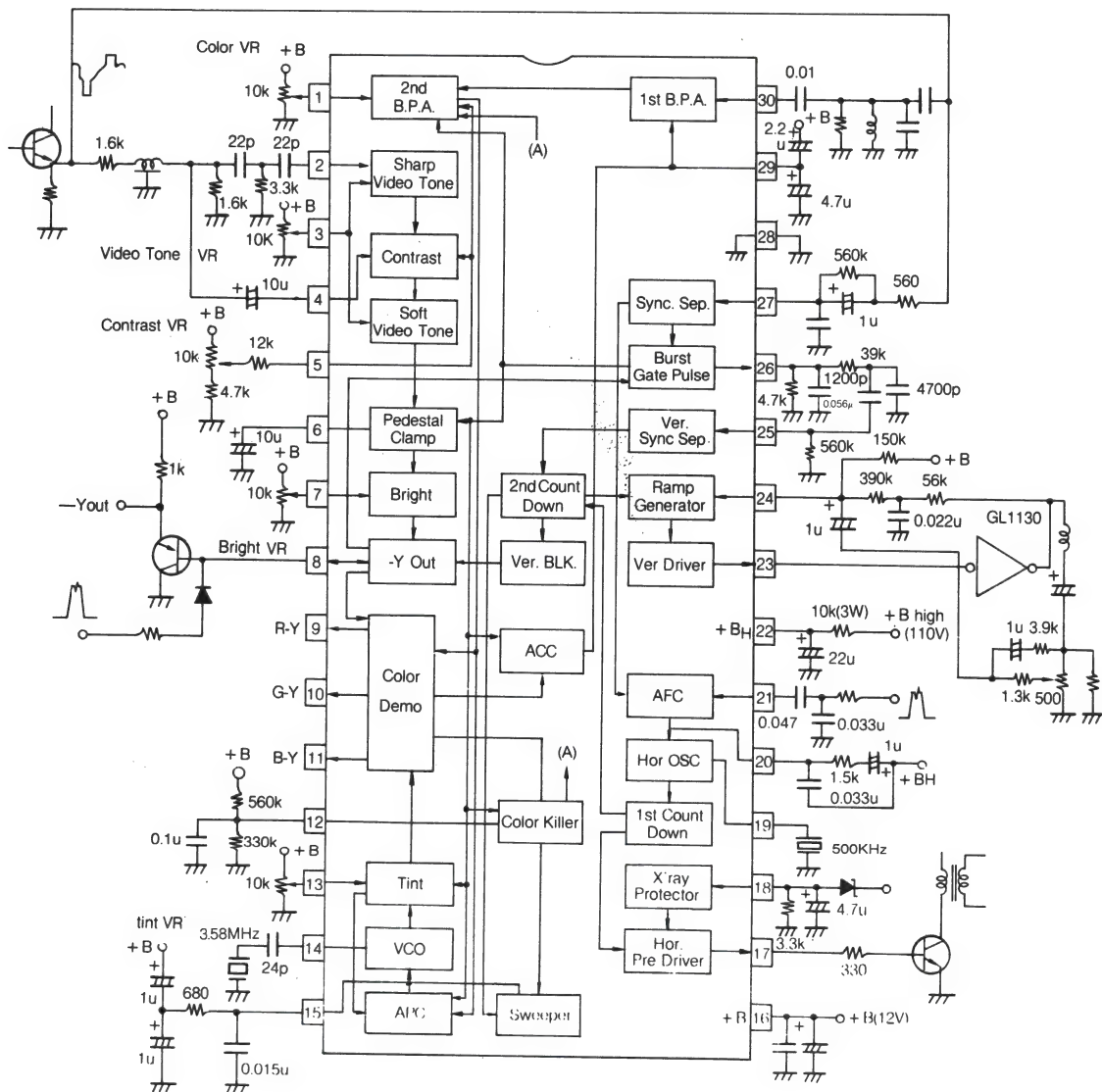
(VIDEO BLOCK)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video Tone Control Characteristic(1)	RE1	$f = 2\text{MHz}$, Video Tone VR: 0V	-5	-3	-1	dB
Video Tone Control Characteristic(2)	RE2	$f = 2\text{MHz}$, Video Tone VR: 12V	12	15	18	dB
Vido Tone Turning Point	V_{3TH}	Reference Value		5.5		V
Video Voltage Gain	A_v	$f = 100\text{ KHz}$	12	15	18	dB
Contrast Control Characteristic	eo	$f = 100\text{KHz}$, $V_i = 100\text{mVpp}$	0.2	0.3	0.4	Vpp
Contrast Control Range	Δeo	$f = 100\text{KHz}$	16	18	20	dB
Bright Control Characteristic(1)	BR1	No Signal, Bright VR: 3V	8			V
Bright Control Characteristic(2)	BR2	No Signal, Bright VR: 6V	5.8	6.3	6.8	V
Bright Control Characteristic(3)	BR3	No Signal, Bright VR: 9V			4.5	V
Frequency Characteristic	f_v	$f = 5\text{MHz}/f = 100\text{KHz}$	-5			dB
Video Output Voltage Change By Contrast	ΔE_o		-50		50	mV
Dependence of Video Output Voltage on Supply Voltage	$\Delta eo(V_{cc})$	$V_{cc} = 12\text{V} \pm 1\text{V}$, $f = 100\text{KHz}$	-10		10	%
Dependence of Video Output Voltage on Temperature	$\Delta eo(T_A)$	$T_A = 25^\circ\text{C} \pm 35^\circ\text{C}$, $f = 100\text{KHz}$	-10		10	%
Dependence of Video Output Voltage on Temperature	$\Delta E_{OY}/\Delta T$	No Signal, $T_A = 25^\circ\text{C} \pm 35^\circ\text{C}$	0	+2	+4	mV/°C

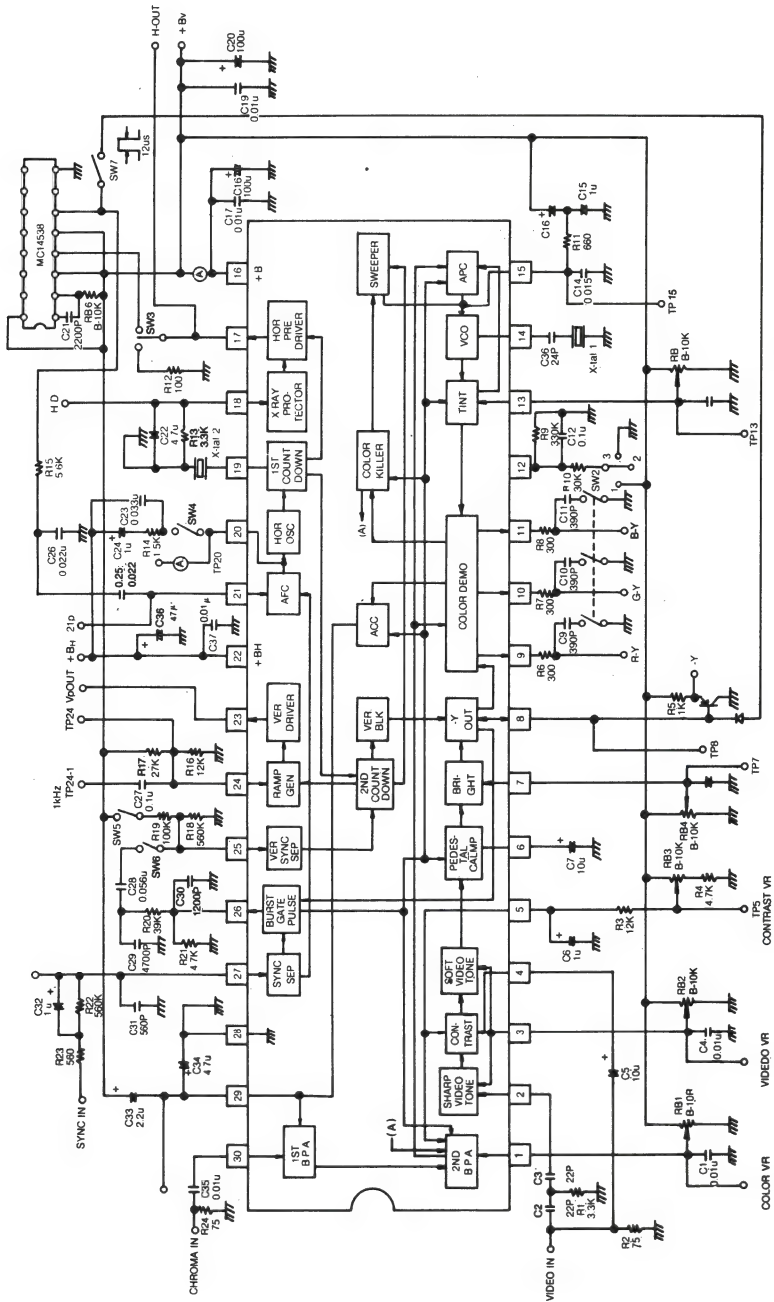
(CHROMA BLOCK)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ACC Amplitude Characteristic(1)	ACC 1	Input: +6dB	-3		3	dB
ACC Amplitude Characteristic(2)	ACC 2	-7	-7		2	dB
ACC Phase Characteristic(1)	ACC 01	Input: +6dB	-3		3	dB
ACC Phase Characteristic(2)	ACC 02	Input: -20dB	-7		7	dB
Killer Operating Point	E_K		-55	-46	-40	dB
Killer Color Residual	E_{KOUT}	Input: E_K (dB)			50	mVpp
Residual Color	E_{CMIN}	Color VR: 0V, Contrast VR: 12V			50	mVpp
Color Difference Output Center	B-Y(CEN)	Output B-Y	2.9	4.3	5.5	Vpp
Maximum Demodulation Output	B-Y(MAX)	Output B-Y	5.5	6.5		Vpp
Color Control Phase Characteristic	$\Delta\phi_c$	Output B-Y	-5		5	deg
Contrast Color Amplitude Characteristic	ΔG	Output B-Y	15.5	17	18.5	dB
Contrast Color Phase Characteristic	$\Delta\phi$	Output B-Y	-5		5	deg
Tint Center	Tcen	Output B-Y	-17	-5	7	deg
Tint Control Range	ΔT	Tint VR: 0V, 6V, 12V	+45 -35			deg
APC Pull-In Range	Δf_{APC}		± 300			Hz
Demodulation Output Ratio(1)	R-Y/B-Y		0.81	0.90	0.98	
Demodulation Output Ratio(2)	G-Y/B-Y		0.24	0.30	0.38	
Demodulation Phase Ratio(1)	$\angle R-Y/B-Y$		96	104	112	deg
Demodulation Phase Ratio(1)	$\angle GY/B-Y$		-132	-122	-112	deg
Color Difference Output Residual Carrier Level	Ecar	No Signal			1.0	Vpp
Color Difference Output Residual Harmonics Level	Ehar				3.0	Vpp
Color Difference Output Voltage	$V_{9,10,11}$		6.7	7.2	7.7	V
Color Difference Output Voltage Difference	$\Delta V_{9,10,11}$		-200		200	mV
Dependence of B-Y Demodulation Output on Supply Voltage	$\Delta B-Y(V_{CC})$	$V_{CC} = 12V \pm 1V$	-20		20	%
Dependence of B-Y Demodulation Phase on Supply Voltage	$\Delta LB-Y(V_{CC})$	$V_{CC} = 12V \pm 1V$	-5		5	deg
Dependence of Color Difference Output Voltage Difference on Supply Voltage	$\Delta \Delta V_{9,10,11}$	$V_{CC} = 12V \pm 1V$			50	mV
Dependence of B-Y Demodulation Output on Temp	$\Delta LB-Y(T_A)$	$T_A = 25^\circ C \pm 35^\circ C$	-15		15	%
Dependence of B-Y Demodulation Phase on Temp	$\Delta LB-Y(T_A)$	$T_A = 25^\circ C \pm 35^\circ C$	-7		7	deg
Dependence of Color Difference Output Voltage on Temp	$\Delta V_{9,10,11}(T_A)$	$T_A = 25^\circ C \pm 35^\circ C$	-2		2	mV/°C
Dependence of Color Difference Output Voltage Difference on Temp	$\Delta \Delta V_{9,10,11}(T_A)$	$T_A = 25^\circ C \pm 35^\circ C$	-1		1	mV/°C

Block diagram and Application Circuit



Test Circuit



GL 3401

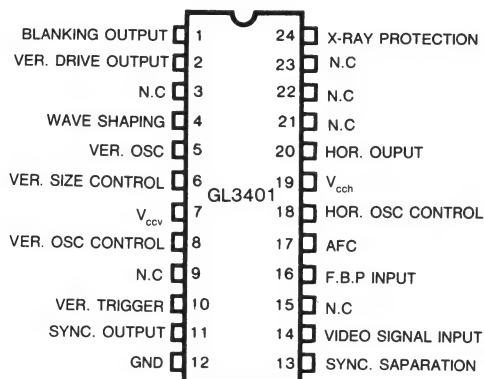
TV DEFLECTION SYSTEM

Description

GL3401 is a bipolar monolithic integrated circuit designed TV deflection system. This IC has all functions including sync.separator, horizontal AFC, horizontal oscillator, X-radiation protector, vertical oscillator and vertical blanking pulse generator.

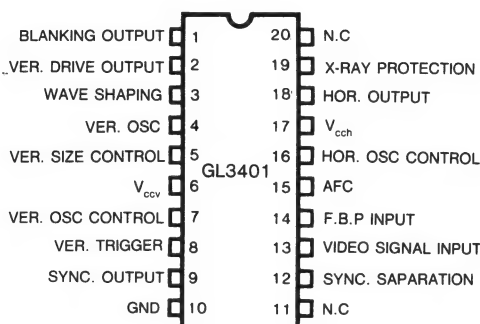
Feature

- Output Circuit Designing Simplified
- No Linearity Adjusting of Vertical Output
- Horizontal OSC. Frequency Limiter: No Malfunction of X-Ray Protector
- Hold-type Operation of X-Ray Protector
- Fewer Influence of Frost between Pins on Impedance Declining

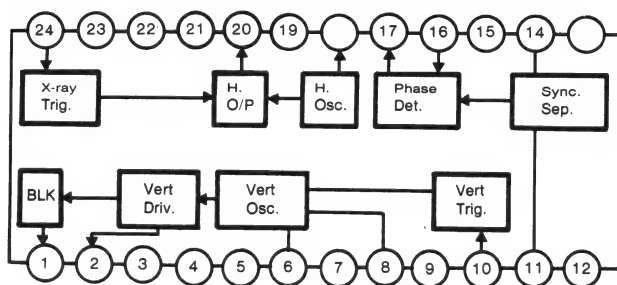


Absolute Maximum Ratings

Vertical Supply Voltage	V_{CCV}	16	V
Horizontal Supply Current	I_{CCH}	25	mA
Vertical Output Current	I_{OV}	15	mA
Horizontal Output Current	I_{OH}	15	mA
Operating Temperature	T_{OPR}	-20~+75	°C
Storage Temperature	T_{STG}	-55~+125	°C
Power Dissipation	P_D	500	mW



Block Diagram



Electrical Characteristics ($T_A = 25^\circ\text{C}$)

	PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
D	Vertical Quiescent Current	I_{CCV}	$V_{CCV} = 12\text{V(DC)}$	6.5	9.4	12.2	mA
C	Horizontal Supply Voltage	V_{CCH}	$I_{CCH} = 15\text{mA}$	11.8	12.8	13.8	V
	H. OSC. Frequency	f_{OH}	$I_{CCH} = 15\text{mA}$	14.734	15.734	16.734	kHz
A	H. OSC. Starting Voltage	V_{OHS}		—	2	6	V
	H. Output Pulse Width	t_{HW}	$f_{OH} = 15.734\text{ kHz}$	22.5	25.0	27.5	μs
C	V_{CCH} Stability of H-OSC.	Δf_{OV}	$V_{CC} \text{ MOD. } -10\%$	-100	+20	100	Hz
	H. Output Saturation Voltage	$V_{CE(sat)}$		—	—	0.3	V
	V. OSC. Frequency	f_{OV}	$V_{CCV} = 12\text{V}$	50	55	60	Hz
	V_{CCV} Stability of V. OSC.	Δf_{OV}	$f_{OV} = (14.4\text{V}) - f_{OV} (9.6\text{V})$	-2	0.7	2	Hz
	V. OSC. Starting Voltage	V_{OVS}	$V_{CCV} = 12\text{V}$	—	4	8	V
	Output Voltage at Pin 11	V_{SY}	Standard Circuit	8.0	10	—	V_{p-p}
	Pulse Width at Pin 11	t_{SV}	APL 50% 1.0 V_{p-p}	4.5	5.0	5.5	μs
	Trigger Gate Voltage	V_{GT}	$I_{CCH} = 15\text{mA}$	0.65	0.72	0.79	V
	V. BlockingPulse Rising Time	$t_{B(up)}$		-5	0	5	μs
	V. Blocking Pulse Falling Time	$t_{B(DOWN)}$		-10	60	180	μs
	Blocking Output Voltage	V_{BL}	Pin 17 (5.6 k ohm)	8.0	10	—	V
	AFC Capture Range	CR		± 450	± 650	—	Hz

GL3711

TV TUNER CONTROLLER

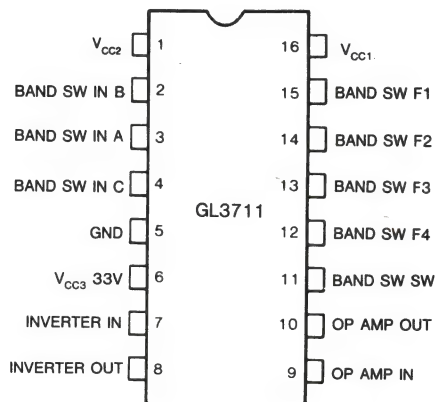
Description

The GL3711 is a tuner controller IC having such functions as band switch, inverter, low pass filter, 33V zener. It can be used for frequency synthesizer or voltage synthesizer according to external application.

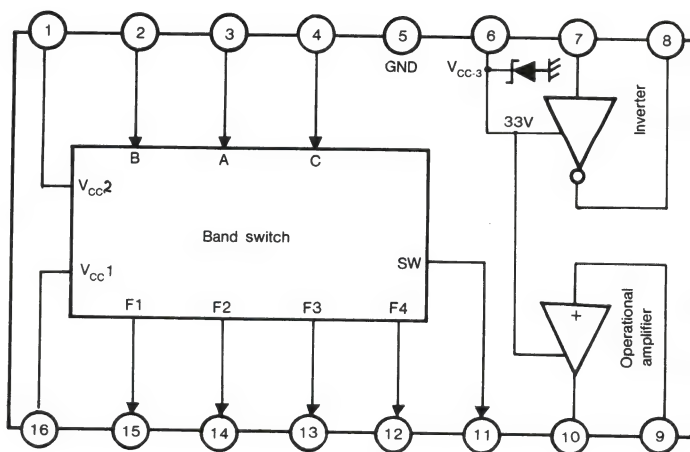
Features

- 2-Input 5-Output Band Switch
- Band Switches of 2 Types Available by Changing Over C Pin
- Large Maximum Output Current and Small Saturation Voltage
- Meets CATV Tuner Requirements
- Usable for Frequency Synthesizer or Voltage Synthesizer by Changing Connection of Inverter and Operational Amplifier

Pin Configuration



Block Diagram



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

BAND SWITCH

V_{CC1} Supply Voltage	V_{16}	18V
V_{CC2} Supply Current	I_1	10mA
Load Current	I_{12} $I_1=6\text{mA}$	-60mA
Load Current	I_{12}, I_{13} $I_1=6\text{mA}$	-60mA
	I_{14}, I_{15} $V_{CC1}=12\text{V}$	
B Input Current	I_2	2mA
A Input Current	I_3	2mA
Applied Voltage (SW)	V_{11}	35V
Applied Voltage	V_{12}	-18V
Applied Voltage	V_{14}	-18V

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

COMMON

Power Dissipation	P_D	600mW
Operating Temperature	T_{OPR}	-20~+65°C
Storage Temperature	T_{STG}	-55~+125°C

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

INVERTER, OPERATIONAL AMPLIFIER

V_{CC3} Supply Current	I_6	8mA
Applied Voltage	V_8	35V
Load Current	I_8	5mA
Input Voltage	V_7	8V
Input Current	I_7	1mA
Input Voltage	V_9	$V_{CC}-1\text{V}$

Electrical Characteristics: $T_A=25^\circ\text{C}$

BAND SWITCH

Parameter	Symbol	CONDITIONS	Min	Typ	Max	Unit
Quiescent Current	I_{CC}	$V_{CC}=12\text{V}$ (V_1, V_{16})	—	—	9	mA
Output Saturation Voltage	$F_{(sat)}$	$V_{CC}=12\text{V}$ (V_{16}) $I_1=6\text{mA}$ $I_{F1\sim F4}=-60\text{mA}$	—	—	0.7	V
Output Saturation Voltage	$SW_{(sat)}$	$V_{CC}=12\text{V}$ (V_{16}) $I_1=6\text{mA}$ $I_7=25\text{mA}$	—	—	0.7	V
Input Threshold Voltage	V_{TH}	$V_{CC}=18\text{V}$ (V_{16}) $I_1=6\text{mA}$, $I_7=25\text{mA}$ $I_{F1\sim F4}=-60\text{mA}$	0.8	1.5	3	V
Output Leak Current	I_L	$V_{CC}=18\text{V}$ (V_{16}) $I_1=6\text{mA}$, $I_{11}=25\text{mA}$	—	—	-50	μA

Electrical Characteristics: $T_A = 25^\circ\text{C}$

INVERTER, OPERATIONAL AMPLIFIER, ZENER

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Zener Voltage	V_Z	$I_6 = 6\text{mA}$	31	33	35	V
Output Saturation Voltage	$V_{8(\text{sat})}$	$I_6 = 6\text{mA}$ $I_8 = 5\text{mA}$			0.3	V
Input Threshold Voltage	V_{TH}	$I_6 = 6\text{mA}$ $I_8 = 5\text{mA}$	2.5		4.5	V
Input Offset Voltage(1)	V_{10-1}	$I_6 = 6\text{mA}$	-100		+100	mV
Input Offset Voltage(2)	V_{10-2}	$I_6 = 6\text{mA}$	-100		+100	mV
Input Bias Current	I_B	$I_6 = 6\text{mA}$			-190	nA

Band Switch Truth Table

Input			Output				
A	B	C	F1	F2	F3	F4	SW
L	L	Open	H	Z	Z	Z	Z
H	L	Open	Z	H	Z	Z	L
L	H	Open	Z	Z	H	Z	L
H	H	Open	Z	Z	Z	H	L
L	L	GND	H	Z	Z	H	Z
H	L	GND	Z	H	Z	H	L
L	H	GND	Z	Z	H	Z	L
H	H	GND	Z	Z	H	H	L

*Z: High Impedance State

GL3812

AUDIO/VIDEO SWITCH FOR TV, VCR

Functions

- Audio Signal Switching
- Video Signal Switching
- Input Signal Selecting Logic

Features

- Possible to Switch 4 Channel Video Signals
- Possible to Switch 4 Channel L & R Audio Signals

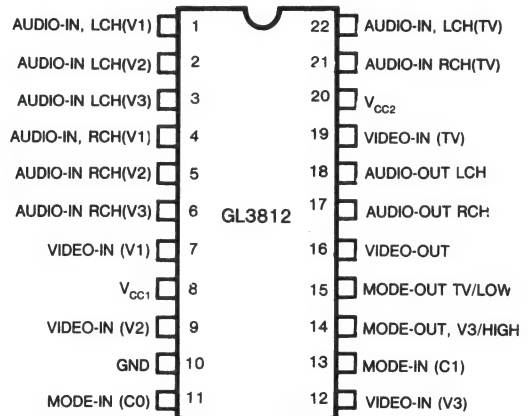
Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage	V_{CC1}	15V
	V_{CC2}	
Power Dissipation	P_D	310mW
Operating Temperature	T_{OPR}	-20 to +70°C
Storage Temperature	T_{STG}	-55 to +125°C

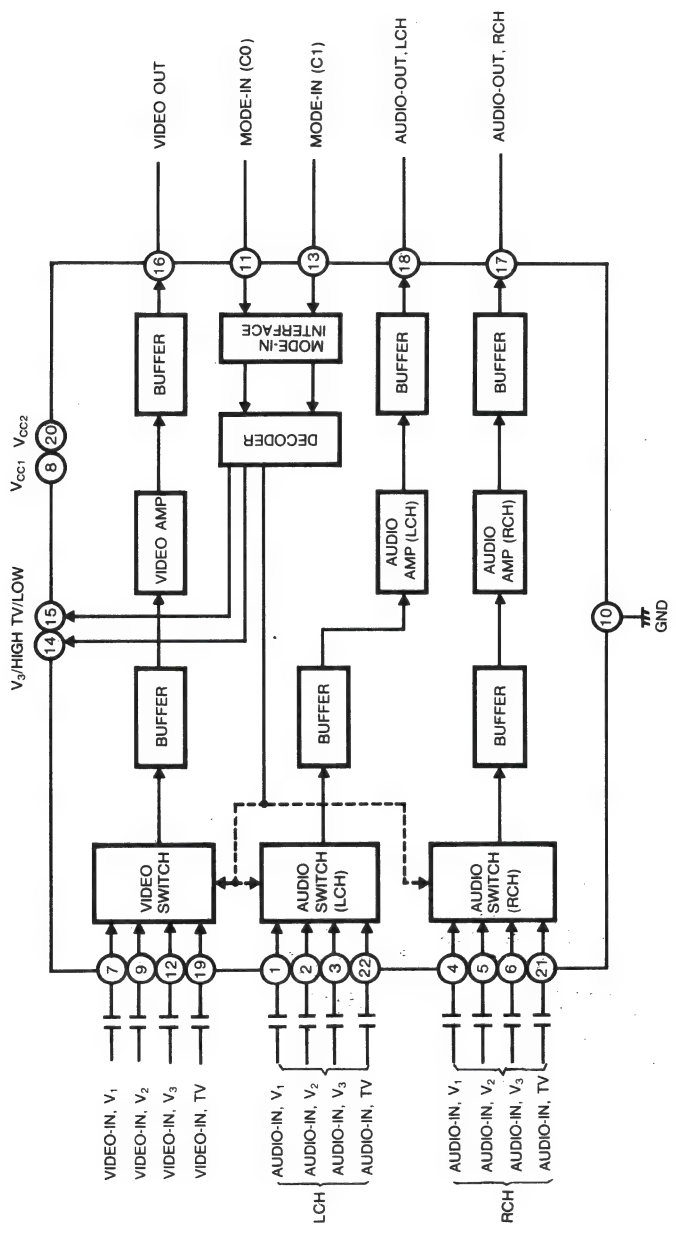
Mode Selection Logic/Output Signal

C1	C0	PIN 14	PIN 15	PIN 16	PIN 17	PIN 18
L	L	L	L	VIDEO (TV)	AUDIO RCH(TV)	AUDIO LCH(TV)
L	H	L	H	VIDEO (V_1)	AUDIO RCH(V_1)	AUDIO LCH(V_1)
H	L	L	H	VIDEO (V_2)	AUDIO RCH(V_2)	AUDIO LCH(V_2)
H	H	H	H	VIDEO (V_3)	AUDIO RCH(V_3)	AUDIO LCH(V_2)

Pin Configuration



Block Diagram



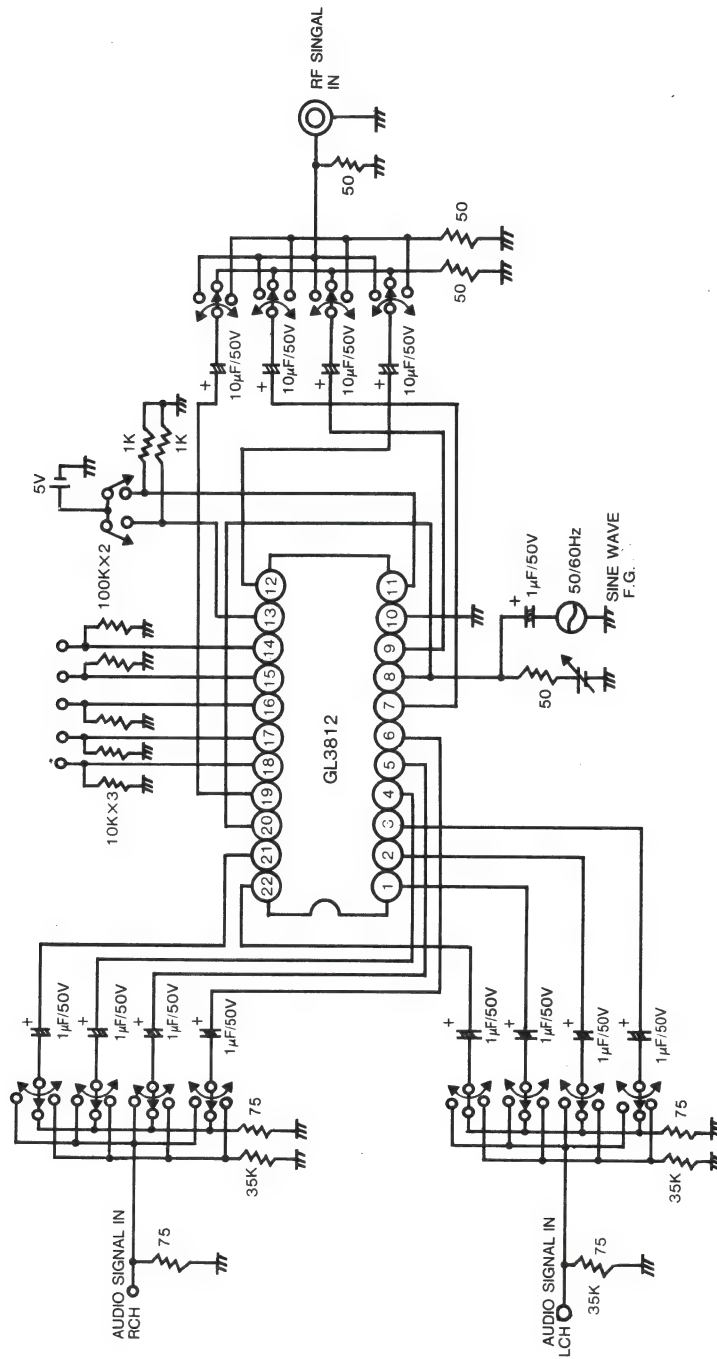
Electrical Characteristics: $T_A=25^{\circ}\text{C}$, $V_{CC}=12\text{V}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Current Dissipation	$I_{CC1,2}$	$V_{CC1}=V_{CC2}=12\text{V}$	10	15	20	mA
Video Channel Bandwidth	F_V	-3dB Frequency	5	10	—	MHz
Video Signal Voltage Gain	A_V	$f=500\text{ kHz}$, $V_{IN}=1V_{p-p}$	5.0	6.0	7.0	dB
Video Signal Input Dynamic Range	D_V	$f=500\text{ kHz}$, THD<1%	1.7	2.0	—	V_{p-p}
Video Channel PSRR	PS_V	$V_{CC1}=12\text{V}+1V_{p-p}$ Sine wave (50Hz/60Hz)	15	20	—	dB
Video Channel Input Impedance	R_{IV}		10	15	20	K Ω
Video Channel Output Impedance	R_{OV}		—	200	—	Ω
Video Channel Crosstalk	CT_V	$f=3.58\text{ MHz}$, $V_{IN}=1V_{p-p}$	40	50	—	dB
Video Channel S/N	SN_V	$V_{out}=2V_{p-p}$	50	60	—	dB
Audio Channel Bandwidth	F_A	-3dB frequency	100	—	—	kHz
Audio Signal Voltage Gain	A_a	$f=1\text{ kHz}$, $V_{IN}=0.5V_{p-p}$	10	12	14	dB
Audio Signal Input Dynamic Range	D_a	$f=1\text{ kHz}$ THD < 1%	0.7	1.0	—	V_{p-p}
Audio Channel PSRR	PS_a	$V_{CC2}=12\text{V}+1V_{p-p}$ Sine wave (50Hz/60Hz)	15	20	—	dB
Audio Channel Input Impedance	R_{ia}		10	15	20	K Ω
Audio Channel Output Impedance	R_{oa}		—	200	—	Ω
Audio Channel Crosstalk	CT_a	$f=1\text{ kHz}$	50	60	—	dB
Audio Channel S/N	SN_a	$V_{OUT}=2V_{p-p}$	60	70	—	dB
Audio Signal THD	THD_a	$f=1\text{ kHz}$, $V_{OUT}=2V_{p-p}$	—	0.5	1.5	%
Input Mode Selection Threshold Voltage	V_{MTH}		2.0	2.3	2.6	V
PIN14 (V_3/H) Low Level Voltage	$V_{L, V3}$	TV or V_1 or V_2 1 mode selection	—	—	0.5	V
PIN 14 (V_3/H) High Level Voltage	$V_{H, V3}$	V_3 mode selection	10	—	—	V
PIN 15 (TV/L) Low Level Voltage	$V_{L, TV}$	TV mode selection	—	—	0.5	V
PIN 15 (TV/L) High Level Voltage	$V_{H, TV}$	V_1 or V_2 or V_3 1 mode selection	10	—	—	V

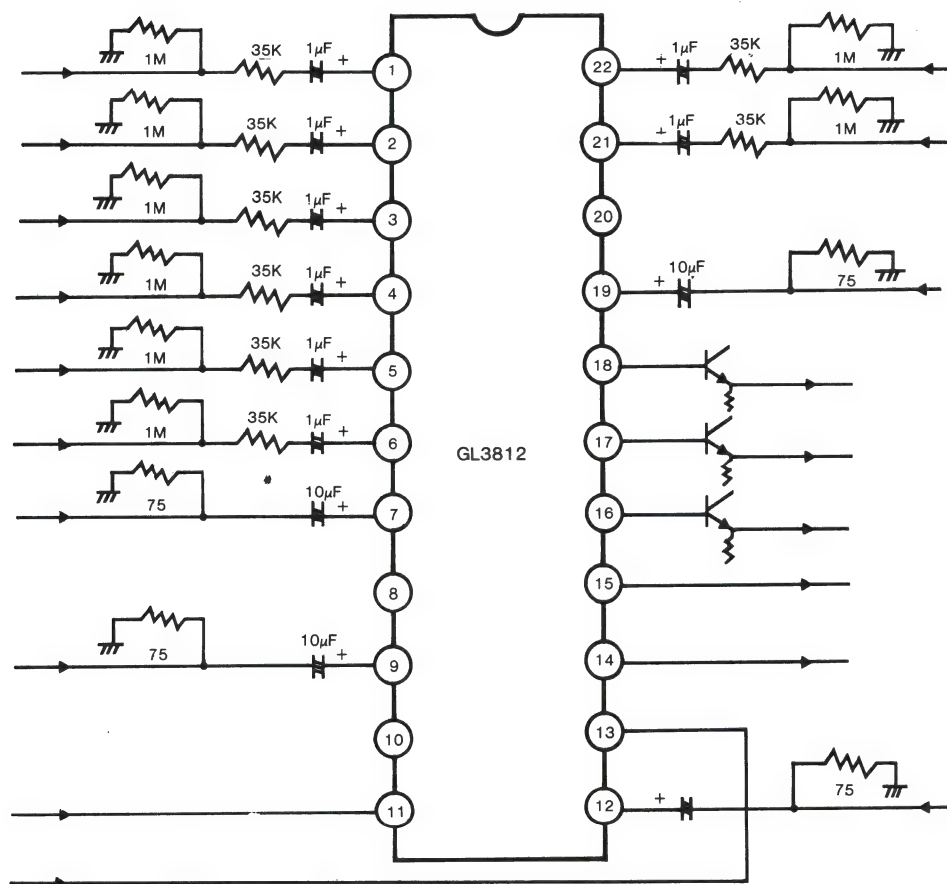
Pin Description

No.	Name	Explanation	No.	Name	Explanation
1	AUDIO-IN (L ₁)	Input of L-Ch Audio Signal for Video (V ₁).	13	MODE-IN (C1)	Input for Mode Selection.
2	AUDIO-IN (L ₂)	Input of L-Ch Audio Signal for Video (V ₂).	14	MODE-OUT (V ₃ /H)	Output Voltage of this Pin Becomes High State, Only when V ₃ is Selected. Else Low State.
3	AUDIO-IN (L ₃)	Input of L-Ch Audio Signal for Video (V ₃).	15	MODE-OUT (TV/L)	Output Voltage of this Pin Becomes Low State, Only when TV is Selected. Else High State.
4	AUDIO-IN (R ₁)	Input of R-Ch Audio Signal for Video (V ₁).	16	VIDEO-OUT	Output of Selected Video Signal.
5	AUDIO-IN (R ₂)	Input of R-Ch Audio Signal for Video (V ₂).	17	AUDIO - OUT (R)	Output of Selected R-CH Audio Signal.
6	AUDIO-IN (R ₃)	Input of R-Ch Audio Signal for Video (V ₃).	18	AUDIO-OUT (L)	Output of Selected L-CH Audio Signal.
7	VIDEO-IN (V ₁)	Input of V Video Signal.	19	VIDEO-IN (TV)	Input of TV Video Signal.
8	V _{CC1}	Power Supply for Video and Logic Block.	20	V _{CC2}	Power Supply for Audio Block.
9	VIDEO-IN (V ₂)	Input of V Video Signal.	21	AUDIO-IN (R-TV)	Input of R-CH Audio Signal for Video (TV).
10	GND		22	AUDIO-IN (L-TV)	Input of L-CH Audio Signal for Video (TV).
11	MODE-IN (C0)	Input for Mode Selection.			
12	VIDEO-IN (V ₃)	Input of V Video Signal.			

Test Circuit



Application Circuit



- * In case of not using Pin 14 or 15, Connect to Ground.
- In case of not using pin 11, Connect to V_{CC} .
- In case of not using pin 13, Connect to Ground.

GL3813

BILINGUAL SIGNAL PROCESSOR (KOREAN TWO-CARRIER TV SYSTEM)

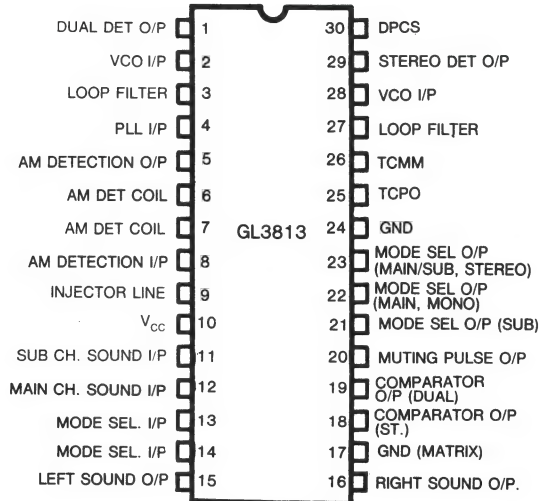
Description

GL3813 is an Integrated Circuit for processing the signals related with a multivoice system in TV sets, and incorporates all the functions required for processing multivoice signals.

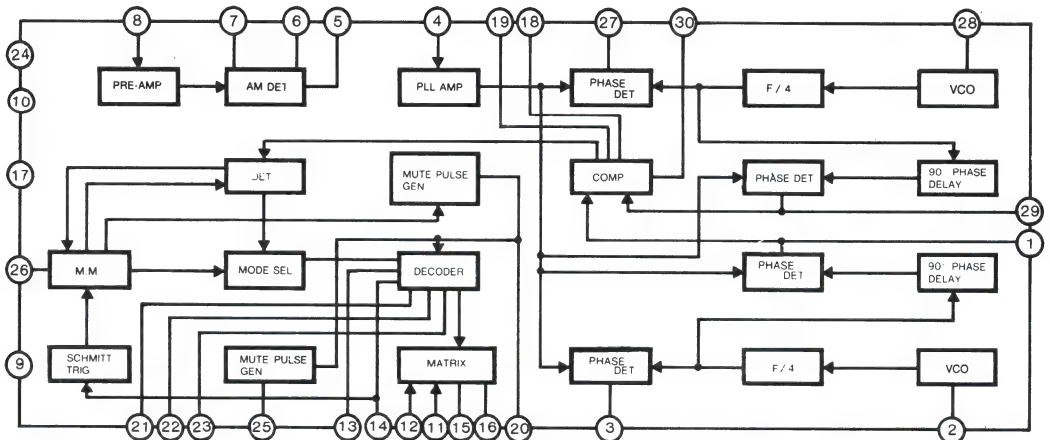
Features

- Integrated Matrix and Identification Signal Discrimination
- Good Characteristic of Identification Signal Discrimination in Weak Field
- Good Characteristic of Stereo Separation and Crosstalk in Matrix
- Automatic Mode Change-Over in a Broadcasting Status Change
- Possible to interface with μ -Processor for Mode Selection
- LED Direct Drive

Pin Configuration



Block Diagram



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

Supply Voltage	V_{CC}		14	V
Allowable Power Consumption	P_D		570	mW
Operating Temperature	T_{OPR}	-20 to	70	$^\circ\text{C}$
Storage Temperature	T_{STG}	-40 to	125	$^\circ\text{C}$
LED Drive Current	I_{LED}		20	mA
Muting Pulse Saturation Current	I_{MP}		2.0	mA

Electrical Characteristics: $T_A=25^\circ\text{C}$, $V_{CC}=12\text{V}$ (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		10.8	12	13.2	V
Quiescent Current	I_{CC}		20	36	50	mA
Pin DC Voltage	V_{P4}		2.0	2.5	3.0	mA
Pin DC Voltage	V_{P5}		0.1	0.4	0.8	V
Pin DC Voltage	V_{P6}, V_{P7}		9.2	10.0	10.8	V
Pin DC Voltage	V_{P8}		2.0	2.5	3.0	V
Pin DC Voltage	V_{P11} V_{P12}		4.3	4.8	5.2	V
Pin DC Voltage	V_{P15}, V_{P16}		3.1	4.3	5.7	V
Matrix Gain	G_{MT}	$V_I=250\text{mV}_{\text{rms}}, 1\text{kHz}$	-1	0	1	dB
Matrix Input Impedance	R_{IMT}	$V_I=250\text{mV}_{\text{rms}}, 1\text{kHz}$	10	20	—	K Ω
Matrix Output Impedance	R_{OMT}	$V_O=250\text{mV}_{\text{rms}}, 1\text{kHz}$	—	100	200	Ω
Matrix Input Dynamic Range	D_{MT}		2.8	3.2	—	V_{P-P}
Total Harmonic Distortion	THD	$V_I=250\text{mV}_{\text{rms}}, 1\text{kHz}$	—	0.1	0.5	%
Hum Rejection Ratio	HRR	$V_{CC}=50\text{mV}_{P-P}, 60\text{Hz}$	30	—	—	dB
Crosstalk, Main→Sub and Sub→Main	CT	$V_I=250\text{mV}_{\text{rms}}, 1\text{kHz}$	60	—	—	dB

Electrical Characteristics: $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Stereo Separation	SEP	$V_i = 125\text{mV}_{\text{rms}}, 1\text{kHz}$	35	—	—	dB
Muting Pulse Saturation Voltage	$V_{\text{MP(sat)}}$	$I_{\text{MP}} = 1\text{mA}$	—	0.2	0.3	V
Muting Pulse Width (Matrix change-over)	$T_{\text{MP(M)}}$		80	100	120	msec
Muting Pulse Width (Power On)	$T_{\text{MP(P)}}$		600	700	900	msec
LED Drive Saturation Voltage	$V_{\text{LED(sat)}}$	$I_{\text{LED}} = 10\text{mA}$	—	1.0	2.0	V
State Input Threshold Voltage	V_{TH1}	L→H H→L	2.2	2.6	3.0	V
Mode Selection Input Threshold Voltage	$V_{\text{TH2(U)}}$	L→H	4.4	4.9	5.3	V
Mode Selection Input Threshold Voltage	$V_{\text{TH2(D)}}$	H→L	2.0	2.9	3.9	V
AM DET Input Impedance	R_{IAM}		10	20	—	k Ω
AM DET Output Impedance	R_{OAM}		—	100	200	Ω
AM DET Input Level	V_{iAM}		—	—	100	mV _{p-p}
AM Detection Output Level	V_{ODET}	$V_i = 15\text{mV}_{\text{p-p}}, f_c = 55.069\text{KHz}$ $f_m = 276\text{Hz}, \text{AM Mod } 50\%$	40	85	150	mV _{p-p}
PLL AMP Input Impedance	R_{iPLL}		7	10	—	k Ω
PLL Capture Range	$2\Delta f_c$	$V_i = 50\text{mV}_{\text{p-p}}$	40	50	60	Hz
PLL Lock Range	$2\Delta f_L$	$V_i = 50\text{mV}_{\text{p-p}}$	45	55	65	Hz
PLL Discriminating Level	$V_{\text{iPLL(U)}}$	$f = 149.8, 276\text{Hz}$ Vi Level Up	14.0	—	—	mV _{p-p}
PLL Discriminating Level	$V_{\text{iPLL(D)}}$	$f = 149.8, 276\text{Hz}$ Vi Level Down	—	—	1.0	mV _{p-p}
DPCS ON Level	$V_{\text{DPCS(ON)}}$	Pin1 = 10V, $T_{\text{DPCS}} = 10\text{mSec}$	1.2	—	—	V
DPCS OFF Level	$V_{\text{DPCS(OFF)}}$	Pin1 = 10V, $T_{\text{DPCS}} = 10\text{msec}$	—	—	0.5	V
DPCS ON Time	T_{DPCS}	Pin1 = 10V, $V_{\text{DPCS}} = 1.2\text{V}$	10	—	—	msec

Logic Table

COMPARATOR O/P (BROADCASTING STATUS)		MODE SELECTION I/P		MODE SELECTION O/P			MATRIX STATUS
Pin19	Pin18	Pin14	Pin13	Pin23	Pin22	Pin21	
H	H (Mono)	Serial pulse I/P	V _{CC}	H	L (Not changed)	H	Mono*
H	L (Stereo)	Serial pulse I/P	V _{CC}	L	H	H	Stereo*
				H	L	H	Mono
L	H (Dual)	Serial pulse I/P	V _{CC}	H	L	H	Main*
				H	H	L	Sub
				L	H	H	Main-Sub
X	X	H	H	H	L	H	Mono or Main
X	H	L	L	H	H	L	Sub
X	H	H	L	L	H	H	Main-Sub
X	L	H	L	L	H	H	Stereo

* Initial mode for the broadcasting status change
 Comments: Comparator O/P never becomes L, L.

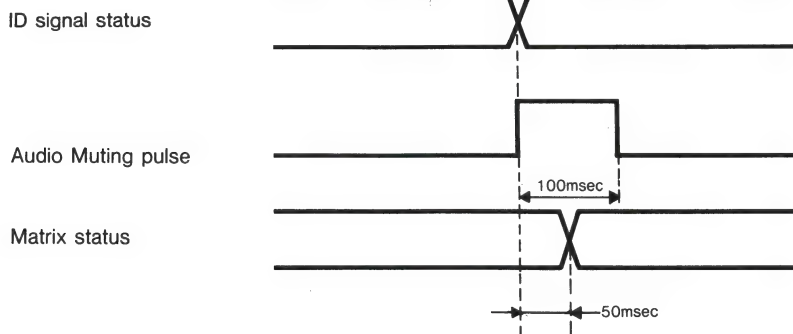
Logic Table Supplement

Pin19	Pin18	Pin14	Pin13	Pin23	Pin22	Pin21	Matrix Status	
							Left	Right
H	H	H	H	H	L	H	CH1*	CH1
		H	L	L	H	H	CH1	CH2*
		L	L	H	H	L	CH2	CH2
		L	H	H	L	L	DC	CH1
H	L	H	H	H	L	H	CH1	CH1
		H	L	L	H	H	CH1+CH2	CH1-CH2
		L	L	H	H	L	CH2	CH1-CH2
		L	H	H	L	L	DC	CH1
L	H	H	H	H	L	H	CH1	CH1
		H	L	L	H	H	CH1	CH2
		L	L	H	H	L	CH2	CH2
		L	H	H	L	L	DC	CH1

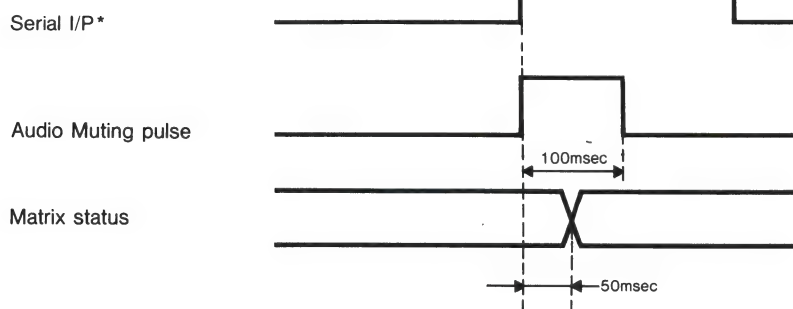
* Channel 1: Main Channel (Composite Sound I/P)
 Channel 2: Sub Channel (Composite Sound I/P)

Logic Time Chart

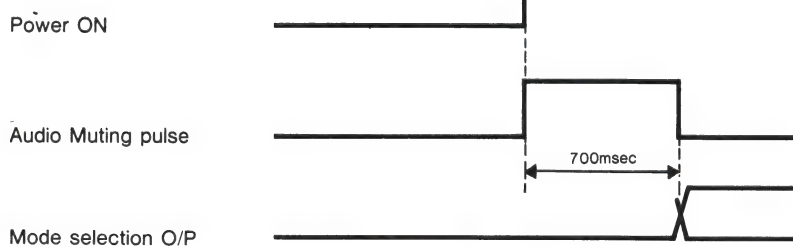
1. When ID signal status is changed



2. In using Serial I/P in Mode Selection



3. Power ON



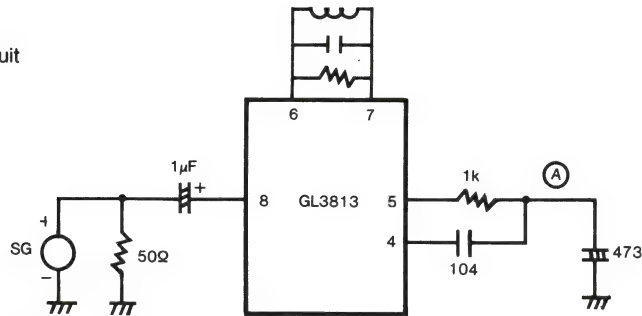
- IF ID SIGNAL STATUS IS MONO, NOT OPERATES
- IN PARALLEL I/P, AUDIO MUTING PULSE IS NOT GENERATED

Pin Description

No.	NAME	Explanation	No.	NAME	Explanation
1	Dual Detection O/P 276	If ID signal O/P is Hz, pin 1 DC voltage becomes above 4V	17	GND 1	Ground for only Matrix block
2	VCO I/P	Pin for the oscillation of VCO. (276×4Hz)	18,19	Comparator O/P	Indicates the state of broad-casting. (Possible to drive LED)
3	Loop Filter	Pin for the loop filter of PLL	20	Muting Pulse O/P	Generates the sound muting pulse in case of power on and mode change
4	AM Detection O/P	Input Terminal for PLL AMP	21,22,23	Mode Selection O/P	Indicates the states of mode selection. (Possible to drive LED)
5	PLL I/P	Output terminal for AM Detector	24	GND2	Ground
6,7	AM Detector Coil	Pin for tuning coil of AM Detector	25	TCPO	Pin for setting the time constant of Muting pulse Generator in Power-on.
8	AM Detection I/P	Input terminal for Pre-AMP of AM Detector	26	TCMM	Pin for setting the time constant of Muting pulse Generator in Matrix change-over
9	Injector Line	Pin of I ² L injector current	27	Loop Filter	Pin for the loop filter of PLL
10	V _{CC}	—	28	VCO I/P	Pin for the oscillation of VCO (149.8×4Hz)
11,12	Composite Sound I/P	Pin 11: Sub channel sound I/P Pin 12: Main channel sound I/P	29	Stereo Detection O/P	If ID signal O/P is 150Hz, pin 29 DC Voltage becomes above 4V
13,14	Mode Selection I/-	1) Parallel I/P pin for the change-over of Mono (Main)/Stereo/ Sub/ Main-Sub forcibly 2) If pin13=V _{CC} , Pin 14 becomes serial I/P for the change-over of Stereo/Mono and Main/Sub/Main-Sub.	30	DPCS (Discharging pin for channel switching)	Pin for discharging pin1 and pin29 when channel is changed
15,16	Sound O/P	Pin 15: Left Sound O/P Pin 16: Right Sound O/P			

Adjustment

1. Q signal tank circuit



Set SG to $f=55.069\text{kHz}$, $50\text{mV}_{\text{p-p}}$.

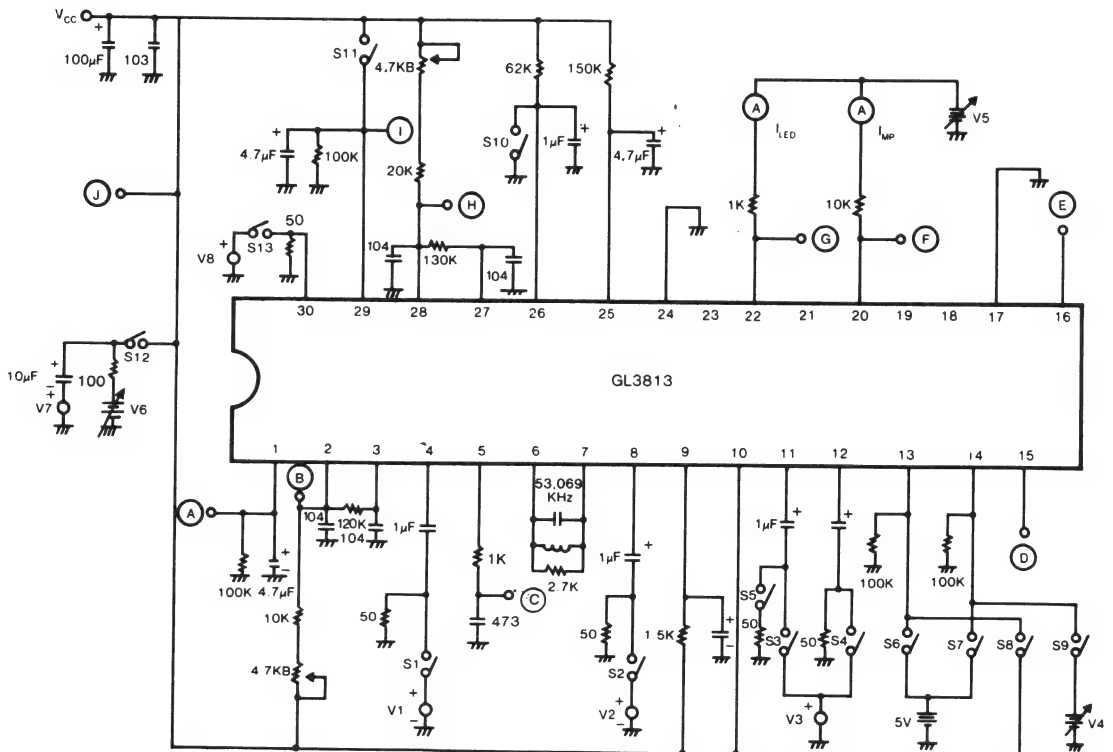
And adjust L of Q signal tank circuit (Pin6, 7) so that DC voltage at node A is maximized.

2. VCO free-running frequency

Connect a counter to pin28 of the GL3813 with 10:1 probe at the state where no input is applied to pin8 or pin4.

Adjust 4.7kB (pin 28) to obtain 599Hz ($149.8 \times 4\text{Hz}$).

In like manner, connect a counter to pin 2 and adjust to obtain 1104Hz ($276 \times 4\text{Hz}$).



GL3820

VIDEO SWITCH

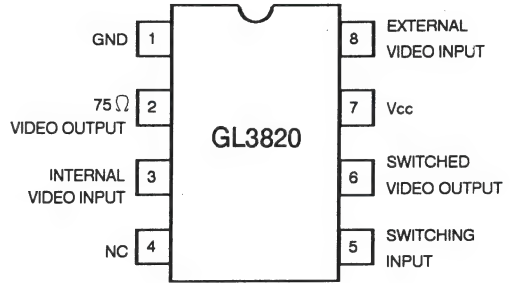
Description

This integrated circuit provides all video switching allowing connections between the peri TV plug and video sections in the TV set.

Features

- 1 Video Output $75\ \Omega$ - 1 V_{pp} No Switched
- 1 Switched Video Output 2 V_{pp}
- Video Cross Talk : 50 dB Typical
- Short Circuit Protection of Inputs and Outputs
- Clamped Video Inputs

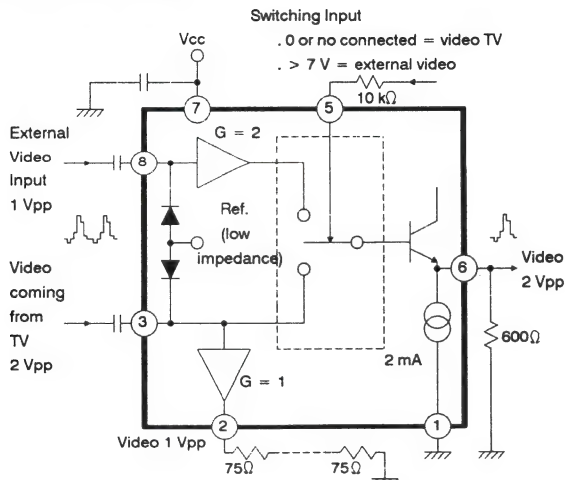
Pin Configuration



Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{cc}	18	V
Operating Temperature	T_{opr}	- 10 to + 100	°C
with Load > $150\ \Omega$		- 10 to + 70	
with Load = $75\ \Omega$			
Junction Temperature	T_j	- 40 to + 150	°C
Storage Temperature	T_{stg}	- 40 to + 150	°C
Minimum DC Load Resistor P_6		600	Ω
Minimum DC Load Resistor P_2		75	Ω

Typical Application and Test Circuit



Note : We advice to protect the $75\ \Omega$ output through a $75\ \Omega$ resistor for supply voltage upper than 9 V.

Electrical Characteristics : $T_a = +25^\circ\text{C}$, $V_{CC} = 9\text{ V}$ (unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage Range	V_{CC}	8	-	14	V
Supply Current (no load on pin 2 and pin 6)	I_{CC}	-	-	20	mA
Supply Current (with $75\ \Omega$ between pin 2-1, with $600\ \Omega$ between pin 6-1)	I_{CC}	-	75	-	mA
Total Power Dissipation with Load	P_{tot}	-	450	-	mW
Internal Video Input Swing from PIF (positive video)	-	-	-	4.5	V_{pp}
Internal Video Input Impedance (positive video)	-	50	-	-	$k\Omega$
Internal Video Input Bias Current (positive video)	-	10	25	40	μA
External Video Input Swing (positive video)	-	-	-	2	V_{pp}
External Video Input Impedance (positive video)	-	50	-	-	$k\Omega$
Switched Video Output Swing	-	-	-	4.5	V_{pp}
Switched Video Output Dynamic Impedance	-	-	-	20	Ω
Switched Video DC Output Voltage (sync. pulse level, note) ($600\ \Omega$)	-	1.7	2	2.4	V
Switched Video Band Width (-1 dB)	-	6	-	-	MHz
Switched Video Output Gain					
Pin 6 - Pin 8 (gain with $600\ \Omega$ load)	-	+ 5	+ 6	+7	dB
Pin 6 - Pin 3 (gain with $600\ \Omega$ load)	-	- 1	- 0.5	0	
External Video Output Swing (with $75\ \Omega$ load)	-	-	2	2.2	V
External Video Dynamic Output Impedance	-	-	10	-	Ω
External Video DC Output Voltage (sync. pulse level, note) ($75\ \Omega$)	-	1.7	2	2.4	V
External Video Output Gain (pin 2 - pin 3 gain with $75\ \Omega$ load)	-	- 1.8	- 1	- 0.4	dB
Switching Input Unactive Low Level or Unconnected Pin (TV receiving)	-	0	-	3	V
Switching Input Active Level (ext. receiving)	-	7	-	V_{CC}	V
Switching Input Impedance	-	10	-	-	$k\Omega$
Video Rejection between Two Inputs					
0 to 5 MHz	-	-	- 50	-	dB
1 kHz	-	- 50	-	-	
Differential Group Delay	-	-	15	-	ns
Linearity Distortion					%
Luma	-	-	2	-	
Chroma	-	-	2	-	
Intermodulation Luma - Chroma	-	-	5	-	
Supply Voltage Rejection (1 kHz)	-	40	50	-	dB

Note : Use a video signal with a synchro pulse in order to make the clamp work in a correct way ($75\ \Omega$ to the ground and $10\ \mu\text{F}$ in series).

	DATA SHEET INDEX	
	QUALITY ASSURANCE MANUAL	
1.	TV APPLICATION	
2.	VCR APPLICATION	
3.	AUDIO APPLICATION	
4.	TELECOM APPLICATION	
5.	REMOTE CONTROL APPLICATION	
6.	INDUSTRY APPLICATION	
	GOLDSTAR SEMICONDUCTOR SALES NETWORK	

GL3130

VIF+SIF CIRCUIT For TV Sets, VTR's

Description

The GL3130 is an IC containing the VIF and SIF on a single chip in the 20DIPS package of shrink type. The use of the small-sized package serves to make VCR Tuner units smaller.

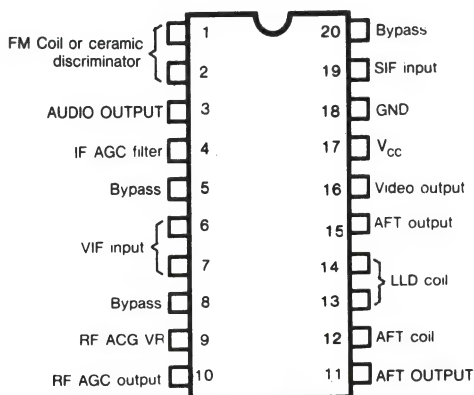
Features

- High Gain VIF Amp Requiring No Preamp
- Possible to Mute Video and Sound for VCR
- Good to Make Tuner Small by Small Sized Package and Reduced External Parts.

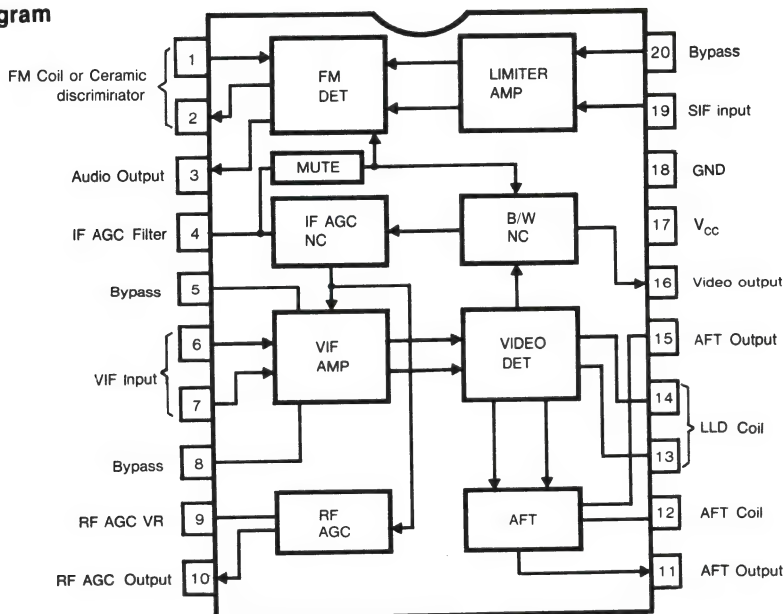
Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Power Supply	V_{CC}	14	V
Pin 16 Out Current	I_{16}	5	mA
Pin 20 Supply Voltage	V_{20}	V_{CC}	V
Power Dissipation	P_d	1.1	W
Operating Temperature	T_{OPR}	$-20 \sim 70$	$^\circ\text{C}$
Storage Temperature	T_{STG}	$-55 \sim 125$	$^\circ\text{C}$

Pin Configuration



Block Diagram



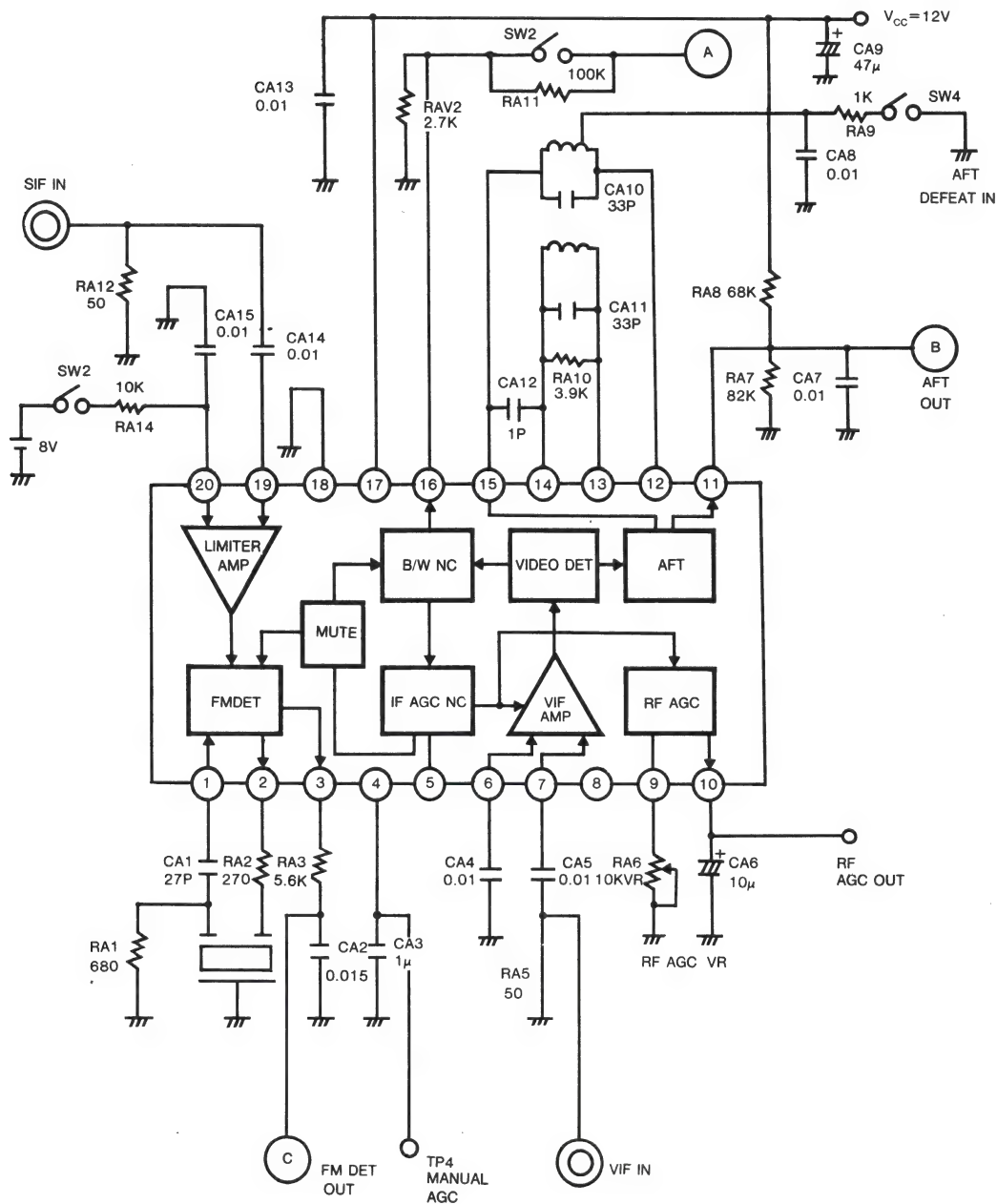
Electrical Characteristics: $T_A=25^{\circ}\text{C}$, $V_{CC}=12\text{V}$, $f_p=58.75\text{MHz}$, $f_s=54.25\text{MHz(VIF)}$, $f_o=4.5\text{MHz (SIF)}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Total Circuit Current	I_{17}	SW1→ON	47	58	74	mA
Maximum RF AGC Voltage	V_{10H}	SW1→ON	8.5	8.9	9.2	V
Minimum RF AGC Voltage	V_{10L}	SW1→OFF		0	0.5	V
Quiescent Video Output Voltage	V_{16}	SW1→ON	5.1	6.1	6.5	V
Quescent AFT Output Voltage	V_{11}	SW1→OFF	4.5	6.5	7.5	V
Input Sensitivity	V_i	Internal AGC 400Hz, 40% S_2 →OFF	30	36	42	dB μ
AGC Range	GR	$V_4=1.5\text{V}$ S_2 →ON	57	64		dB
Maximum Permitting Input	$V_{I, \text{MAX}}$	Internal AGC S_2 →ON 15KHz, 78%	100	200		mV _{rms}
Video output Amplitude	$V_{O(\text{Video})}$	S_2 →ON Internal AGC 15KHz, 78% 10mVrms	1.9	2.2	2.5	V _{pp}
Sync. Signal Edge Level	$V_{16, \text{tip}}$	S_2 →ON Internal AGC $V_i=10\text{mVrms}$	3.4	3.65	3.9	V
Output S/N	S/N	S_2 →ON Internal AGC $V_i=10\text{mVrms}$	48	54		dB
Carrier Rejection	CR	S_2 →ON External AGC 15KHz, 78% 10mVrms	50	55		dB
Maximum AFT Output Voltage	V_{11H}	S_2 →ON Internal AGC $f_p=45.75\pm 1.5\text{MHz}$	11.0	11.4		V
Minimum AFT Output Voltage	V_{11L}	$V_i=10\text{mVrms}$ S_2 →ON, Internal AGC $f_p=45.75\pm 1.5\text{MHz}$		0.5	1.0	V
AFT Det. Sensitivity	S_f	$V_i=10\text{mVrms}$, S_2 →ON Internal AGC $f_p=45.75\pm 1.5\text{MHz}$	80	110	150	mV/KHz
White Noise Thershold Level	V_{WTH}	S_2 →ON $V_4=4.5\text{V}$ $f_p=45.75\pm 1.5\text{MHz}$	6.4	6.8	7.2	V
White Noise Clamp Level	V_{WCL}	S_2 →ON $V_4=4.5\text{V}$ $f_p=45.75\pm 1.5\text{MHz}$	4.2	4.6	5.0	V
Black Noise Thershold Level	V_{BTH}	S_2 →ON $V_4=4.5\text{V}$ $f_p=45.75\pm 1.5\text{MHz}$	2.1	2.4	2.7	V
Black Noise Clamp Level	V_{BCL}	S_2 →ON $V_4=4.5\text{V}$ $f_p=45.75\pm 1.5\text{MHz}$	3.8	4.2	4.6	V
SIF Output Signal Voltage	$V_{O(\text{SIF})}$	S_2 →ON, Internal AGC 45.75MHz : 10mVrms 42.25 MHz : 1mVrms	80	140	210	mVrms
Frequency Characteristic	f_C	S_2 →ON, Internal AGC 45.75MHz : 10mVrms 45.65~35MHz : 2mVrms	5	7		MHz

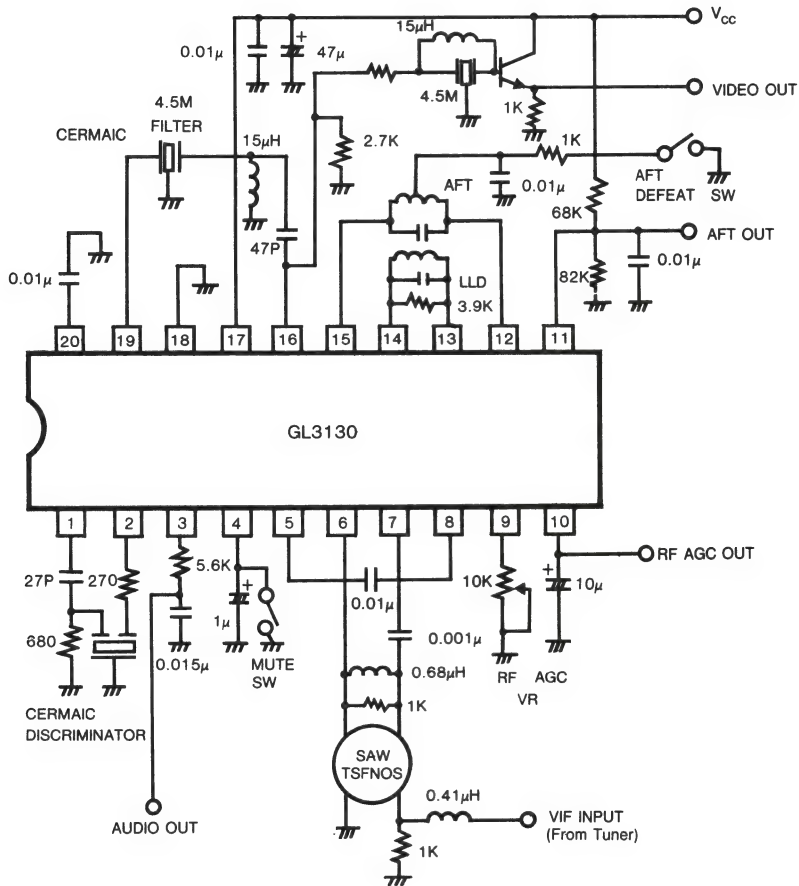
Electrical Characteristics: $T_A = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Gain	DG	$S_2 \rightarrow \text{ON}$, Internal AGC 45.75MHz, APL 50% 87.5%, -27dBm		3		%
Differential Phase	DP	$S_2 \rightarrow \text{ON}$, Internal AGC 45.75MHz, APL 50% 87.5%, -27dBm		3		deg
VIF Input Resistance	V_{IFRi}		1	1.5	2.0	k Ω
VIF Input Capacitance	V_{IFCi}			3.0	6.0	Pf
SIF Limiting Voltage THD _(DET)	$V_{I(lim)}$	$V_4 = 4.5\text{V}$ 4.5MHz, 400Hz $\Delta f = \pm 25\text{KHz}$		200	500	μVrms
FM Det. Output Voltage	$V_{O(DET)}$	$V_4 = 4.5\text{V}$ 4.5MHz, 400Hz $\Delta f = \pm 25\text{KHz}$, 100mVrms	450	680	850	mVrms
FM DET Output Distortion	THD _(DET)	$V_4 = 4.5\text{V}$ 4.5MHz, 400Hz $\Delta f = \pm 25\text{KHz}$, 100mVrms		0.5	1.3	%
AM Rejection Ratio	AMR	$V_4 = 4.5\text{V}$ 4.5MHz, 400Hz 30%, 100mVrms	50	60		dB
Noise Output Voltage	V_N	$V_4 = 4.5\text{V}$			3.5	mVrms
Pin 4 Mute Starting Voltage	$V_{M(4)}$	$S_2 \rightarrow \text{ON}$ $V_4 = 4.5\text{V}$	0.5	0.7		V
Pin 20 Mute Attenuation	ATTM ₍₂₀₎	$S_3 \rightarrow \text{ON}$, $V_4 = 4.5\text{V}$ 4.5 MHz, 400Hz $\Delta f = \pm 25\text{KHz}$, 50mVrms	60			dB

Test Circuits



Application Circuit



GL3615

VCR AUDIO PLAY/RECORD AMP

Function

- PB Amp, Line Amp, REC Amp, ALC Amp with detector inside
- REC/EE, PB/EE, line mute control circuit

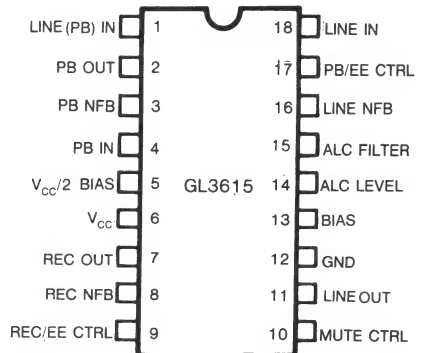
Features

- Low Power Consumption
- Little External Components
- Excellent S/N, THD Characteristic due to High-Level ALC VR
- Little Power ON-OFF Noise
- Little Shock Noise when Mode Switches
- Noise Immune REC Amp due to Line Buffer Amp

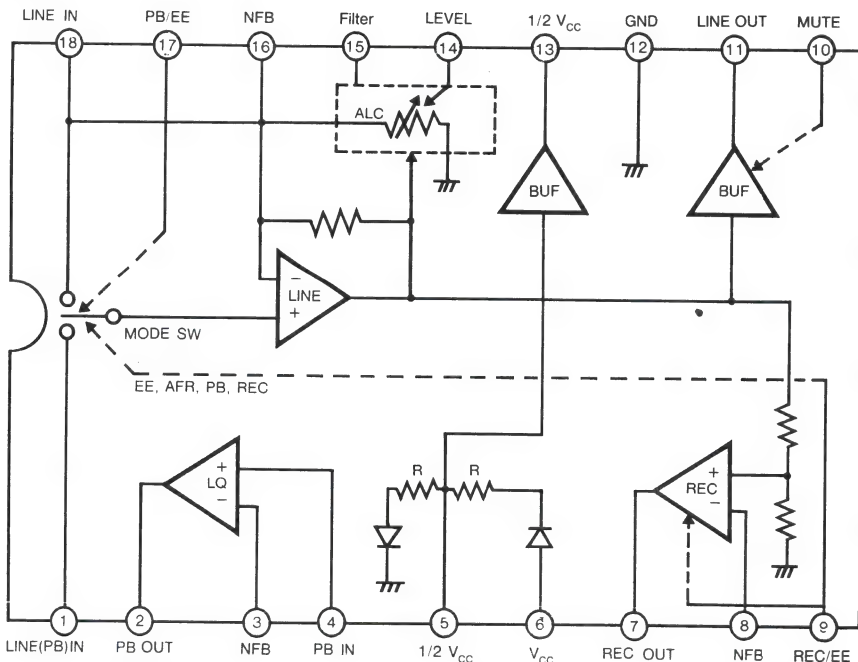
Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage	V_{CC}	13	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	$-10 \sim 65$	$^\circ\text{C}$
Storage Temperature	T_{STG}	$-55 \sim 125$	$^\circ\text{C}$

Pin Configuration



Block Diagram



Electrical Characteristics: $T_A=25^{\circ}\text{C}$, $V_{CC}=5\text{V}$, $f=1\text{kHz}$

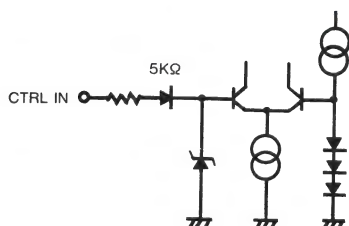
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Operation Voltage	V_{CC}	EE Mode	4	5	13	V
Quiescent Current	I_{CC}	EE Mode		4.0	6.2	mA
EE mode Total Gain	G_{VEE}	ALC off, $V_{IN}=-25\text{dBm}$	14.5	17.5	20.5	dB
EE mode THD	THD_{EE}	ALC off, $V_O=0\text{dBm}$		0.08	0.3	%
LINE Amp Max. Output	V_{OML}	$\text{THD}=1\%$	0.8	1.2		Vrms
Noise in EE mode	V_{NOL}	$R_g=5.6\text{k}\Omega$, DIN Audio		-76	-68	dBV
ALC Level	V_{OA}	$V_{IN}=-15\text{dBm}$	0.41	0.54	0.73	Vrms
ALC THD	THD_A	$V_{IN}=-15\text{dBm}$		0.06		%
ALC THD with Strong Input	THD_{ST}	$V_{IN}=10\text{dBm}$		0.12		%
REC mode Total Gain	G_{VR}	ALC off	14.5	17.5	20.5	dB
REC mode Open Loop Gain	G_{VOR}	ALC off		44		dB
REC mode THD	THD_R	$V_O=0\text{dBm}$		0.064	0.3	%
REC Amp Max. Output	V_{OMR}	$\text{THD}=1\%$	0.8	1.2		Vrms
PB mode Total Gain	G_{VPB}		76.5	80.0	83.5	dB
PB mode THD	THD_{PB}			0.11	0.4	%
PB Amp Gain	G_{VE}			40		dB
PB Amp Open Loop Gain	G_{VOE}			70		dB
PB Amp THD	THD_E	$V_O=0\text{dBm}$		0.016	0.2	%
PB Amp Noise converted to Input	V_{NINE}	$R_g=620\text{k}\Omega$, DIN Audio		-122	-114	dBV

Pin Description

NO	NAME	Explanations	No	NAME	Explanations
1	LINE(PB) IN	Playback Mode, Line Amp Input	10	MUTE CTRL	Mute Input
2	PB OUT	Playback EQ Amp Output	11	LINE OUT	LINE AMP Output
3	PB NFB	SP/LP/EP Mode Feedback	12	GND	Ground Pin
4	PB IN	PB Head Signal Input	13	Buffered Bias	ALC Level Adj. Output
5	$V_{CC}/2$ Bias	$1/2V_{CC}$, Bias Filter	14	ALC LEVEL	ALC V_{ref} Bias pin $V_{OA(rms)} = [V_{Bias} - V_{ref}] / \sqrt{2}$
6	V_{CC}	V_{CC}	15	ALC FILTER	ALC Attack Time Set Recovery Time
7	REC OUT	REC Amp Output	16	LINE LFB	Line Amp Feedback
8	REC NFB	REC Amp Feedback	17	PB/EE CTRL	PB/EE Mode Input
9	REC/EE CTRL	REC/EE Mode Input	18	LINE IN	Tuner, Aux, Input

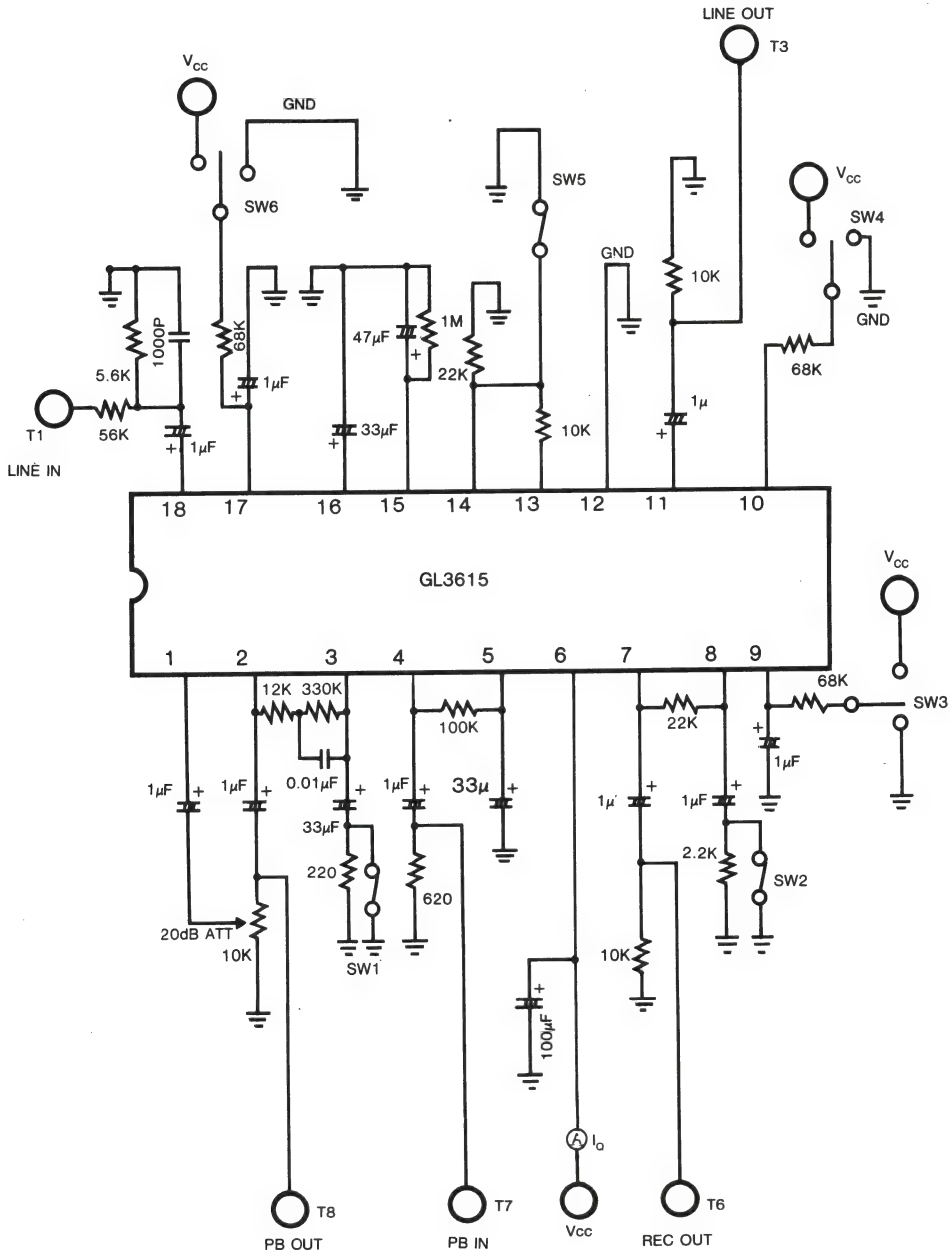
CONTROL MODE TABLE

MODE	CTRL TERMINAL			FUNCTION				
	REC/EE	PB/EE	MUTE	EQ AMP	LINE SW	LINE OUT	REC OUT	ALC
EE	L	L	L	(ON)	REC	ON	OFF	ON
EE MUTE	L	L	H	(ON)	REC	OFF	OFF	ON
REC	H	L	L	(ON)	REC	ON	ON	ON
REC MUTE	H	L	H	(ON)	REC	OFF	ON	ON
PB	L	H	L	ON	PB	ON	OFF	OFF
PB MUTE	L	H	H	ON	PB	OFF	OFF	OFF
AFR	H	H	L	(ON)	REC	ON	ON	ON
AFR MUTE	H	H	H	(ON)	REC	OFF	ON	ON



Threshold Voltage V_{TH} of the CTRL Terminal is $4 V_F (\div 2.5V)$
 PB/EE, REC/EE CTRL needs Time Constant Circuit ($68K\Omega$, $1\mu F$)
 MUTE CTRL may not need $68 K\Omega$ resistor when V_{CC} is higher than CTRL Voltage.

Test Circuit



GL3667

VCR FINE SLOW-STILL MOTION CONTROL

Description

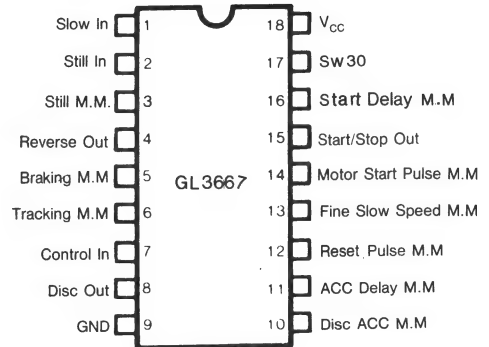
GL3667 is a Monolithic IC designed for VCR Motion Control. In operation, Capstan Motor is Controlled according to the PB CTL pulse with the time delay adjusted by external resistors and capacitors.

In addition, this IC contains compensation circuit for Head-Drum Noise Reduction.

Features

- Time Delay is Controlled by the External Resistor and Capacitor
- Built-in Reset Circuit with no CTL Signal Input
- Fine Still, Fine Slow, Frame Advance
- Compensation Circuit for Head Drum Noise Reduction

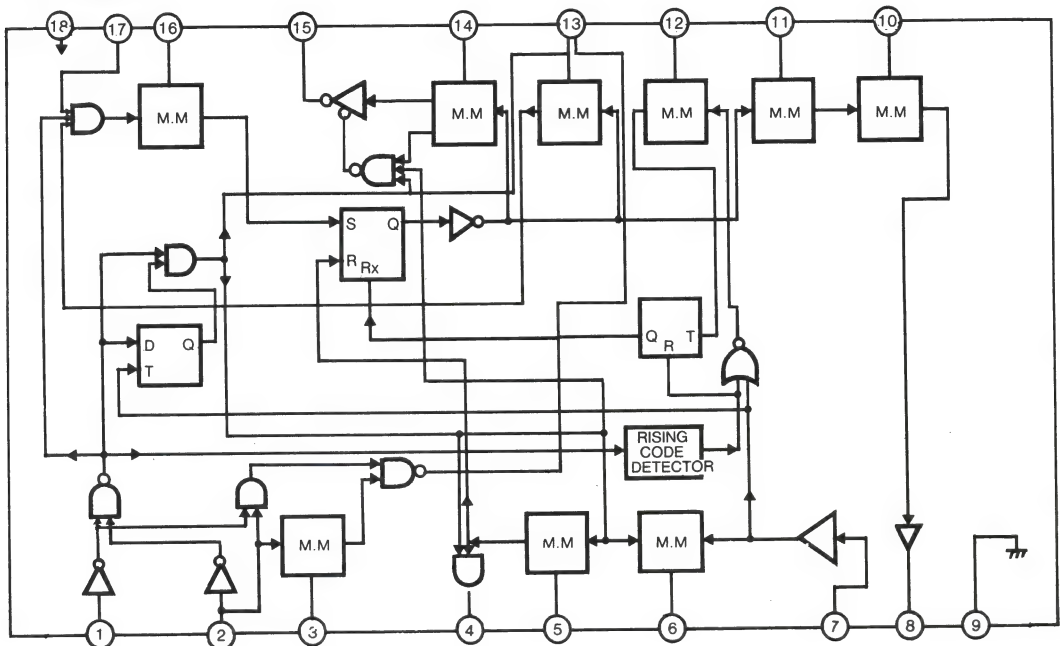
Pin Configuration



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage	V_{CC}	13	V
Power Dissipation	P_D	550	mW
Operating Temperature	T_{OPR}	-25	75 $^\circ\text{C}$
Storage Temperature	T_{STG}	-55	125 $^\circ\text{C}$

Block Diagram



Electrical Characteristics: $T_A = 25^\circ\text{C}$, $V_{CC} = 9\text{V}$

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Quiescent Current	I_O	TEST CKT	—	14	21	mA
DC Voltage Level	V_7	TEST CKT	4.5	4.9	5.4	V
M.M Stand-by Voltage	V_{MO3}	TEST CKT	1.2	1.5	1.7	V
M.M Stand-by Voltage	V_{MO12}	TEST CKT	0.5	0.7	0.9	V
M.M Threshold Level	V_{TH3}	TEST CKT	4.3	4.6	4.9	V
M.M Threshold Level	V_{TH5}	TEST CKT	4.1	4.4	4.7	V
M.M Threshold Level	V_{TH6}	TEST CKT	4.2	4.5	4.8	V
M.M Threshold Level	V_{TH10}	TEST CKT	4.2	4.5	4.8	V
M.M Threshold Level	V_{TH11}	TEST CKT	4.2	4.5	4.8	V
M.M Threshold Level	V_{TH12}	TEST CKT	4.0	4.3	4.7	V
M.M Threshold Level	V_{TH13}	TEST CKT	4.6	4.9	5.2	V
M.M Threshold Level	V_{TH14}	TEST CKT	4.2	4.5	4.8	V
M.M Threshold Level	V_{TH16}	TEST CKT	4.0	4.35	4.8	V
REV OUT "L"	V_{4L}	TEST CKT	—	0.5	1.05	V
REV OUT "H"	V_{4H}	TEST CKT	8.9	9	—	V
CTL Input Sensitivity	V_{ID}	TEST CKT	120	200	270	mV
Input Threshold V1	V_{TH1}	TEST CKT	1.5	2	2.7	V
Input Threshold V2	V_{TH2}	TEST CKT	3.0	3.9	5.0	V
DISC OUT "H"	V_{8H}	TEST CKT	8	9	—	V
DISC OUT "L"	V_{8L}	TEST CKT	—	0.2	0.5	V
S/S Out Put "H"	V_{15H}	TEST CKT	6.1	6.95	7.3	V
S/S Out Put "M"	V_{15M}	TEST CKT	4.1	4.5	4.9	V
S/S Out Put "L"	V_{15L}	TEST CKT	0.6	0.9	1.6	V
M.M. Z-State	V_{13Z}	TEST CKT	0.6	0.8	1.1	V
SW30 Threshold Level	V_{TH17}	TEST CKT	1.5	2	2.7	V

Timing Diagram

MODE	TEST CONDITION	TEST PIN	TIMING DIAGRAM	REMARKS
NO OPERATION	PIN1 LOW PIN2 LOW			ALL M.M Rest
SLOW MODE	Pin1 High	1		T1=15mS
	Pin7 CTL In	7		
	Pin17 SW30	17		
	Start Delay M.M	16		
	F.S. Speed M.M	13		
	Motor Start Pluse M.M	14		
	ACC Delay M.M	11		
	DISC Acc. M.M	10		
	S/S Out	15		
	Tracking M.M	6		
	Brake M.M	5		
	REV Out	4		
	DISC Out	8		
	Reset M.M	12		
				T2=60mS
STILL MODE	Pin1 Low			T3=60mS
	Pin2 High	2		
	Pin7 CTL In	7		
	Pin17 SW30	17		
	Still M.M	3		
	Start Delay M.M	16		
	F.S. Speed M.M	13		
	Motor Start Pluse M.M	14		
	ACC Delay M.M	11		
	DISC Acc. M.M	10		
	TRACKING M.M	6		
	BRAKE M.M	5		
	S/S Out	15		
	Reset M.M	12		

Pin Description

1) Pin 1 (Slow Input)

pin 1 is a slow input terminal. Pin 1 voltage is divided by two series 40K Ω , 20K Ω resistors, and the voltage at 20K Ω resistor switches internal transistor on.

2) Pin 2 (Still Input)

Pin 2 is a still input terminal. Pin 2 voltage is divided by 40K Ω resistor three diodes, and 20K Ω resistor and the voltage at 20K Ω resistor turns internal transistor on.

When still and slow input remain Low, SW30 pulses cannot trigger start delay M.M, so slow or still motion do not be performed any more.

3) Pin 17 (SW 30)

Pin 17 is a reference 30 Hz input terminal. Pin 17 voltage is divided by two series 40K Ω , 20K Ω series resistors, and the voltage at 20K Ω resistor switches internal transistor on.

4) Pin 16 (Start Delay M.M)

Pin 16 is to set delay time before slow or still mode starts. Start delay M.M is triggered at SW30 falling edge and it begins charging. At the sometime, FS speed M.M begins charging also. Start delay M.M does not operate when FS speed M.M keeps charging or slow and still input level keep low.

5) Pin 13 (Fine Slow Speed M.M)

Pin 13 is to set Fine Slow Speed. It is triggered by RS flip flop output, also RS flip flop is triggered high when start delay M.M operation is over.

When slow input is kept high, CTL pulses are needed to continue changing state of RS flip flop output.

6) Pin 14 (Motor Start Pulse M.M)

Pin 14 is to set pulse width of motor start M.M. Motor start pulse M.M begins to charge when RS flip flop output Q changes its state from "Low" to "High".

During motor start M.M charges, S/S output is kept high state, and at this time capstan motor is accelerated.

When charging is over, S/S output becomes medium state from high state, and at this state voltage of pin 15 is determined by external resistors.

7) Pin 7 (Control In)

Pin 7 is control pulse input terminal. CTL pulses are amplified at CTL pulse AMP via coupling capacitor, and CTL pulses require minimum 270 V_{p-p}.

8) Pin 6 (Tracking M.M)

Pin 6 is to set tracking time of capstan motor. Only when RS flip flop output Q is high and slow or still input remain high, CTL pulse falling edge triggers tracking M.M.

At this time capstan motor receives neither acceleration nor deceleration force from capstan motor driver and S/S output becomes medium state.

9) Pin 5 (Braking M.M)

Pin 5 is to set braking time of capstan motor. Braking M.M is only triggered at falling edge of tracking M.M. If tracking M.M is not activated, braking M.M does not operate also. Falling edge of braking M.M changes RS flip flop output from high to low, and makes RS flip flop be ready to receive start delay M.M output.

Consequently, individual M.M operates only once in spite of sequential input of SW30, because start delay M.M is forced to be locked during FS speed M.M operation.

10) Pin 4 (Reverse Out)

Pin 4 is a open collector output, and collector output load resistor requires minimum 5K Ω resistor, and internally 500 Ω resistor is connected in series for current overload protection.

The period of REV. Out is determined by the brake M.M, in other words REV. Out has same period with Brake M.M. When Rev. Out is low, capstan motor is forced to stop.

11) Pin 15 (Start/Stop Out)

Pin 15 has 3 state output. And 3-state is "High", "Medium", "Low".

Pin 15 is externally connected by two resistor and medium state voltage can be obtained freely by combination of two resistors.

During motor speed M.M operation S/S out is high, and capstan motor is accelerated. When motor speed M.M operation is over S/S out becomes medium state and capstan motor keeps on tracking.

Braking M.M operation make S/S out be low, at this time capstan motor is forced to stop. Also, S/S output falls to low state when reset pulse M.M operation is over.

12) Pin 12 (Reset Pulse M.M)

Pin 12 is for retriggerable M.M to generate reset pulse.

Reset pulse M.M starts charging with slow or still input, and discharges by every CTL pulse input. Reset pulse M.M Keeps charging with no CTL pulse input, after that generates reset pulse so that RS flip flop changes its state. RS flip flop out reset all circuit.

If slow or still motion is to be performed, slow and still input must be low and high again.

13) Pin 11 (Acceleration Delay M.M)

Pin 11 is to set delay time to accelerate head drum. Acceleration delay M.M starts charging at start delay M.M falling edge.

14) Pin 10 (Disc Acceleration M.M)

Pin 10 is to set time to accelerate head drum. Disc acceleration M.M starts charging at acceleration delay M.M falling edge.

15) Pin 8 (Disc Out)

Pin 8 is a transistor collector output with internal 10K Ω load resistor.

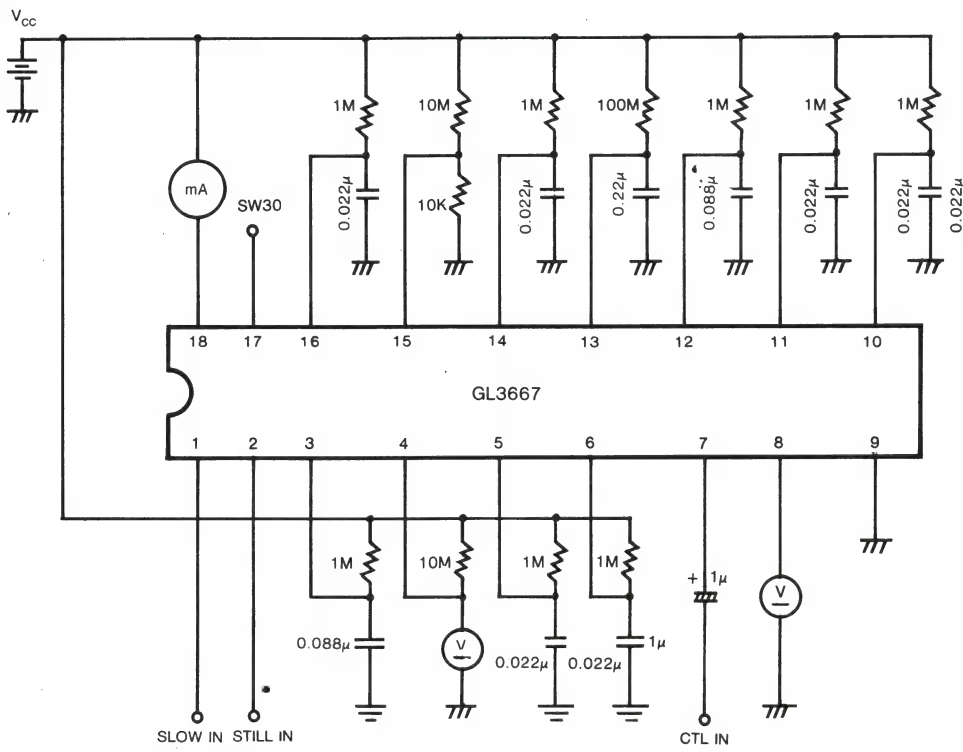
Disc out is normally low. Only when disc acceleration M.M operates, its output becomes high.

16) Pin 3 (Still M.M)

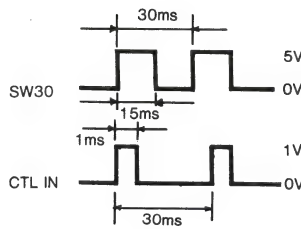
Pin 3 is to determine time for still mode. Still M.M is triggered by still input rising edge, only when slow input is low.

When still M.M operation is over, with still input being high and slow input being low, FS speed M.M becomes impedance state so that start delay M.M is not activated any more. As a result, start delay M.M operates only once during still M.M operation, and still mode is performed.

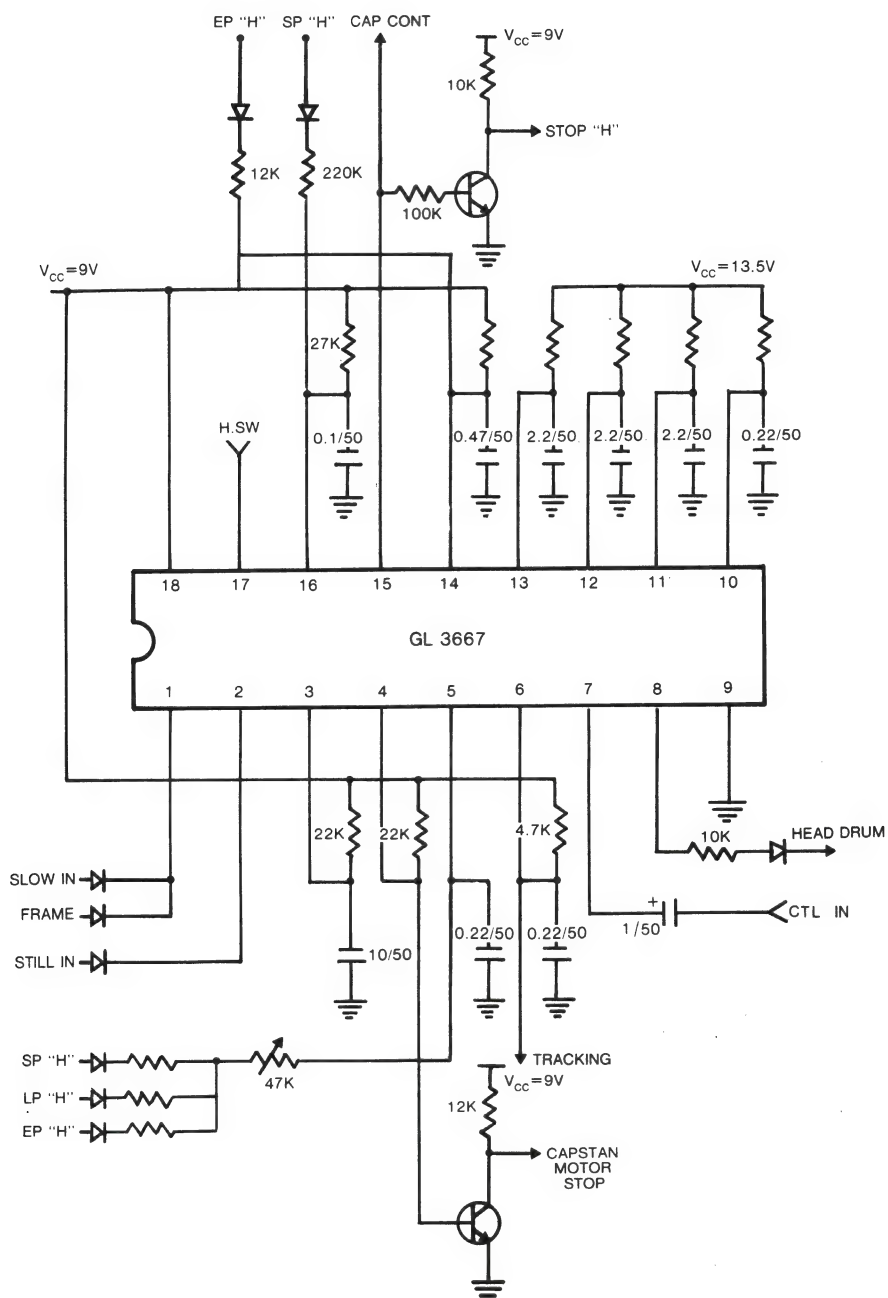
Test circuit



SLOW IN HIGH : 5V
LOW : 0V
STILL IN HIGH : 5V
LOW : 0V



Application Circuit



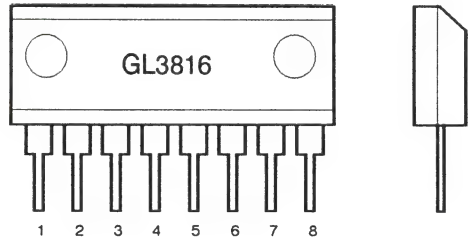
GL3816

ELECTRONIC SWITCH

Features

- Adjust to Switching of Large Signal
- Low Distortion
- Good Frequency Characteristic
- Wide Input Dynamic Range

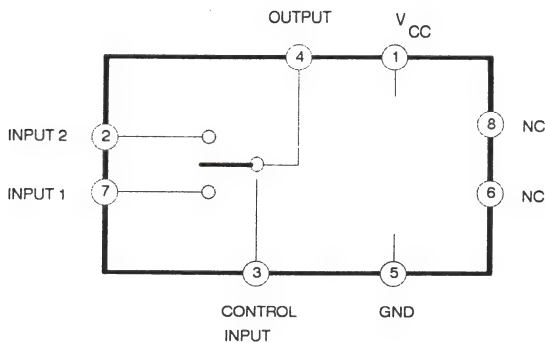
Pin Configuration



Maximum Ratings ($T_A = 25^{\circ}\text{C}$)

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Supply Voltage	V_{CC} max				15	V
2	Allowable Power Consumption	P_D max	$T_A \leq 85^{\circ}\text{C}$			300	mW
3	Operating Temperature	T_{OPG}		-20		65	$^{\circ}\text{C}$
4	Storage Temperature	T_{STG}		-40		125	$^{\circ}\text{C}$

Block Diagram



Electrical Characteristics ($T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$)

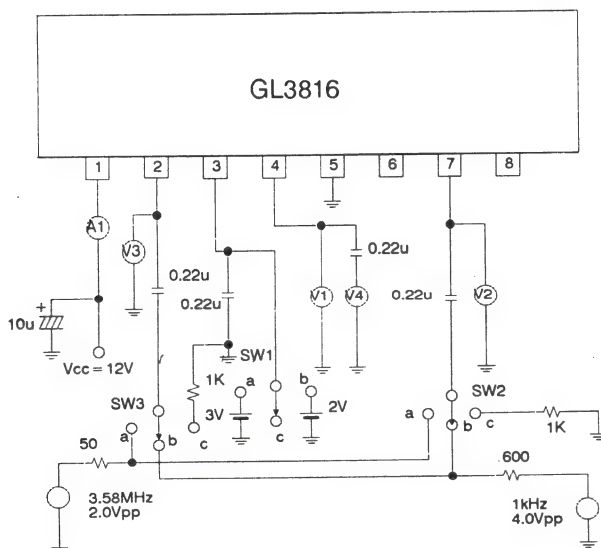
No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Supply Current	I_{CC}		7.5	9.3	12.5	mA
2	Pin DC Voltage	V_4			6.9		V
3	Pin DC Voltage	V_7	$V_3 = 2.0\text{V}$ $V_3 = 3.0\text{V}$		7.6 7.6		V
4	Pin DC Voltage	V_2	$V_3 = 2.0\text{V}$ $V_3 = 3.0\text{V}$		7.6 7.6		V
5	Control Threshold Voltage	V_{TH}		2.2	2.6	3.0	V
6	Total Harmonic Distortion	THD	* $R_g = 600\Omega$, 4.5V_{p-p} , $f = 1\text{kHz}$, $R_L = \text{inf.}$	-	0.007	0.1	%
7	Noise	e_n	* $R_L = \text{inf.}$	-	-93	-80	dBs
8	Crosstalk	I_s	*Input A : $R_g = 50\Omega$, $f = 3.58\text{MHz}$, 2V_{p-p} Input B : $R_g = 1\text{K}\Omega$	50	68		dB
9	Pedestal	V_{PED}	$V_3 = 2.0\text{V} \sim 3.0\text{V}$	-100	0	+100	mV
10	Second Harmonic	$V^{(2)}$	$R_g = 50\Omega$, $f = 1\text{MHz}$, 4.0V_{p-p} , $R_L = \text{inf}$	46	55	-	dB
11	Third Harmonic	$V^{(3)}$	$R_g = 50\Omega$, $f = 1\text{MHz}$, 4.0V_{p-p} , $R_L = \text{inf}$	46	52	-	dB

Remarks : * Measure with input 1 and input 2 respectively

when measured by input 1, $V_3 = 2.0\text{V}$

when measured by input 2, $V_3 = 3.0\text{V}$

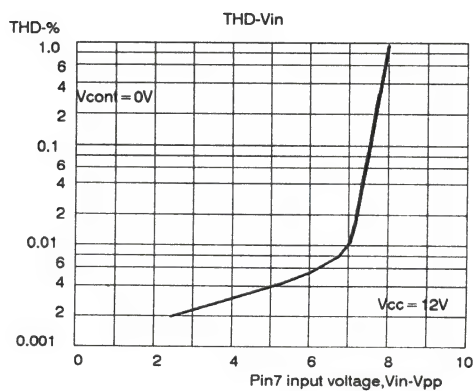
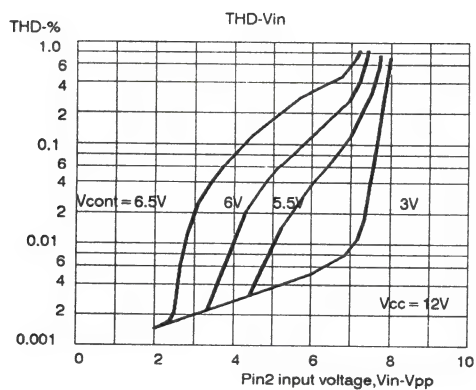
Test Circuit

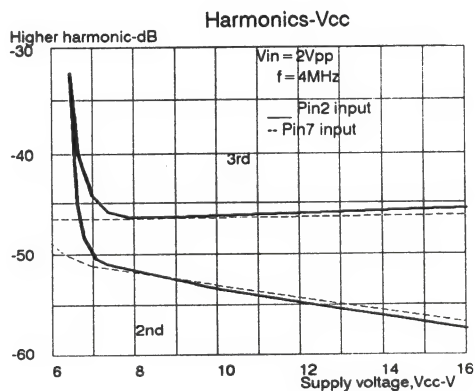
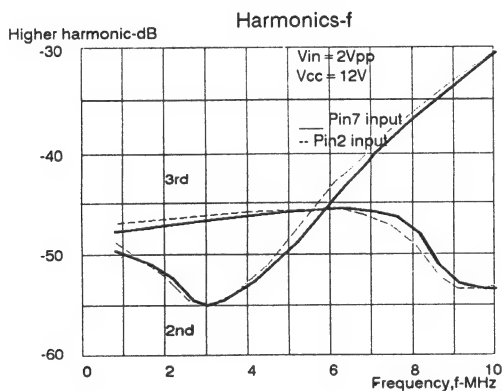
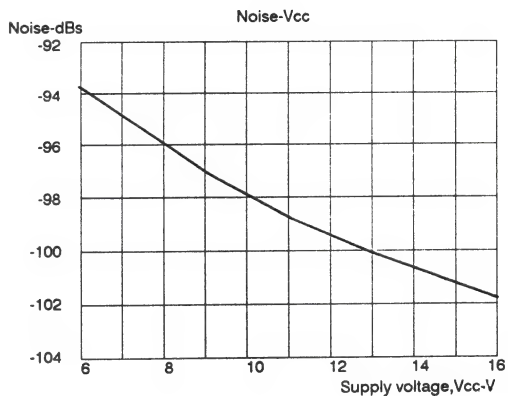
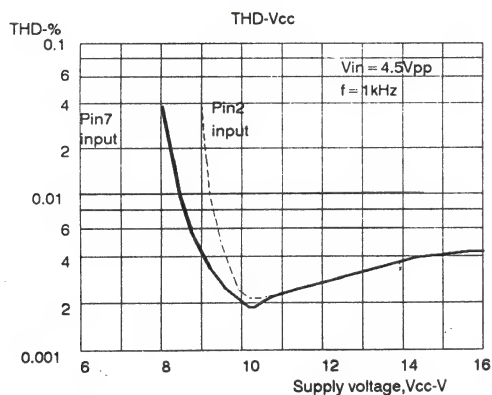
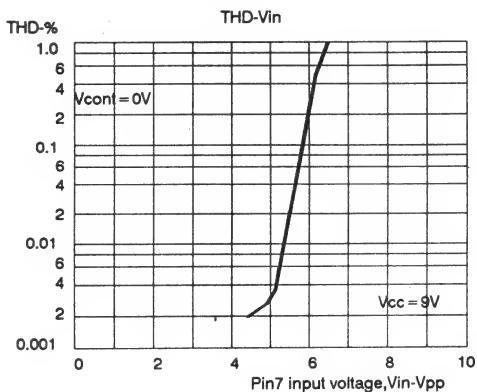
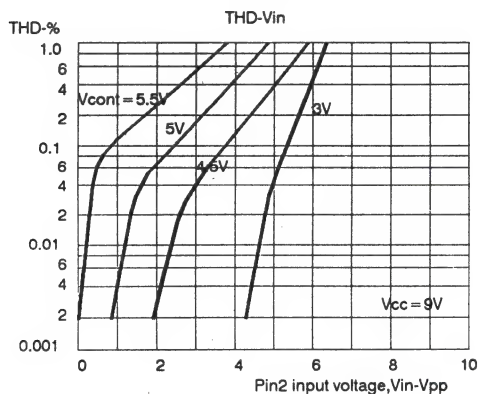


Test Condition

Item	Symbol	SW1	SW2	SW3	Test Point
Circuit Current	I_{CC}	c	c	c	A1
Distortion(1)	THD	b	b	c	V4
Distortion(2)	THD	a	c	b	V4
Noise(1)	e_n	b	c	c	V4
Noise(2)	e_n	a	c	c	V4
Crosstalk(1)	I_{S1}	b	c	a	V4
Crosstalk(2)	I_{S2}	a	a	c	V4
Pedestal	V_{PED}	a-b	c	c	V1
Pin Voltage(pin4)	V_4	c	c	c	V1
Pin Voltage(pin7)	V_7	b	c	c	V2
Pin Voltage(pin7)	V_7	a	c	c	V2
Pin Voltage(pin2)	V_2	b	c	c	V3
Pin Voltage(pin2)	V_2	a	c	c	V3

Typical Performance Curves





	DATA SHEET INDEX	
	QUALITY ASSURANCE MANUAL	
1.	TV APPLICATION	
2.	VCR APPLICATION	
3.	AUDIO APPLICATION	
4.	TELECOM APPLICATION	
5.	RFMOTE CONTROL APPLICATION	
6.	INDUSTRY APPLICATION	
	GOLDSTAR SEMICONDUCTOR SALES NETWORK	

GL386

LOW VOLTAGE AUDIO POWER AMP

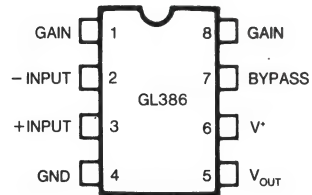
Description

The GL386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the GL386 ideal for battery operation.

Pin Configuration

(Top View)



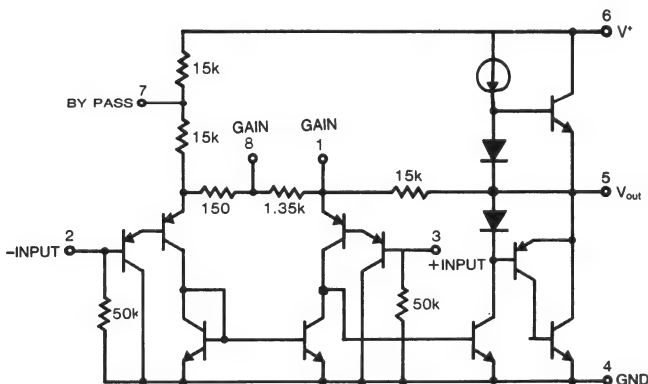
Features

- Battery Operation
- Minimum External Parts
- Wide Supply Voltage Range: 4V-12V or 5V-18V
- Low Quiescent Current Drain: 4mA
- Voltage Gains from 20 to 200
- Ground Referenced Input
- Self-Centering Output Quiescent Voltage
- Low Distortion
- Eight Pin Dual-In-Line Package

Absolute Maximum Ratings

Supply Voltage	15	V
Package Dissipation	1.25	mW
Input Voltage	± 0.4	V
Storage Temperature	-65°C to $+150^{\circ}\text{C}$	$^{\circ}\text{C}$
Operating Temperature	-0 to $+70$	$^{\circ}\text{C}$
Junction Temperature	$+150$	$^{\circ}\text{C}$
Lead Temperature	$+300$	$^{\circ}\text{C}$

Schematic Diagram



Electrical Characteristics $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V^*		4		12	V
Quiescent Current	I^*	$V^* = 6\text{V}$, $V_{IN} = 0$		4	8	mA
Output Power	P_o	$V^* = 6\text{V}$, $R_L = 8\Omega$, THD = 10% $V^* = 9\text{V}$, $R_L = 8\Omega$, THD = 10%	500	700 1000		mW mW
Voltage Gain	A_v	$V^* = 6\text{V}$, $f = 1\text{kHz}$ $10\mu\text{F}$ from Pin 1 to 8		26 46		dB dB
Bandwidth	BW	$V^* = 6\text{V}$, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion	THD	$V^* = 6\text{V}$, $R_L = 8\Omega$, $P_{OUT} = 125\text{mW}$ $f = 1\text{kHz}$, Pins 1 and 8 Open		0.2		%
Power Supply Rejection Ratio	PSRR	$V^* = 6\text{V}$, $f = 1\text{kHz}$, $C_{BYPASS} = 10\mu\text{F}$ Pins 1 and 8 Open		50		dB
Input Resistance	R_{IN}			50		k Ω
Input Bias Current	I_B	$V^* = 6\text{V}$, Pins 2 and 3 Open		250		nA

Application Information

GAIN CONTROL

To make the GL386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35k Ω resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 k Ω resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15k Ω resistor). For 6 dB effective bass boost: $R \cong 15\text{k}\Omega$, the lowest value for good stable operation is $R = 10\text{k}\Omega$ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 k Ω can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater the 9.

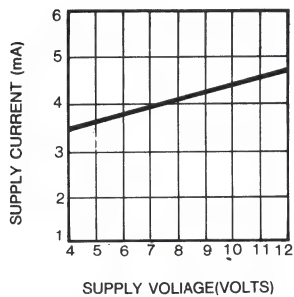
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 k Ω resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the GL386 is higher than 250 k Ω it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 k Ω , then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

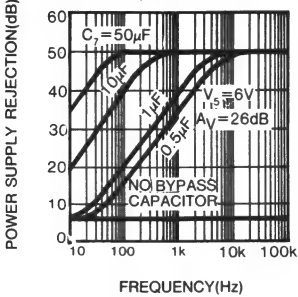
When using the GL386 with higher gains (by passing the 1.35 k Ω resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Curves

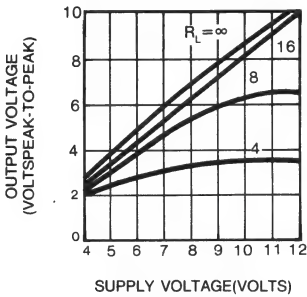
QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE



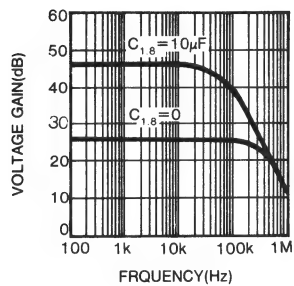
POWER SUPPLY REJECTION RATIO (REFERRED TO THE OUTPUT) vs FREQUENCY



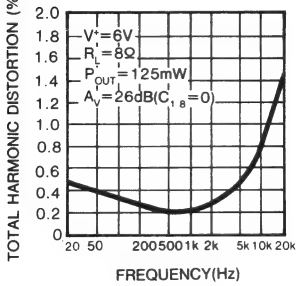
PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



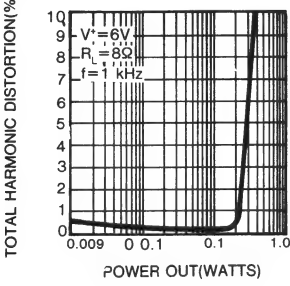
VOLTAGE GAIN vs FREQUENCY



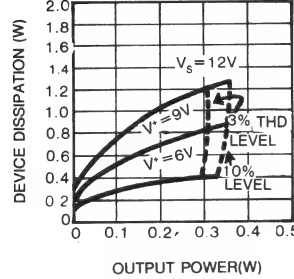
DISTORTION vs FREQUENCY



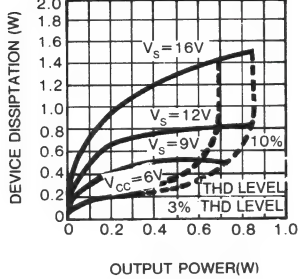
DISTORTION vs OUTPUT POWER



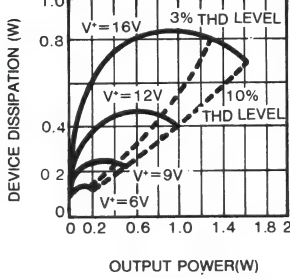
DEVICE DISSIPATION vs OUTPUT POWER-4Ω LOAD



DEVICE DISSIPATION vs OUTPUT POWER-8Ω LOAD

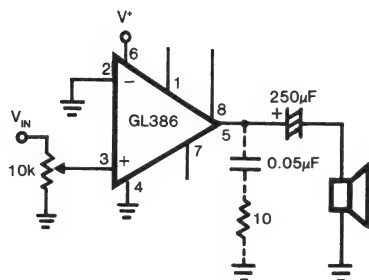


DEVICE DISSIPATION vs OUTPUT POWER (W) OUTPUT POWER-16Ω LOAD

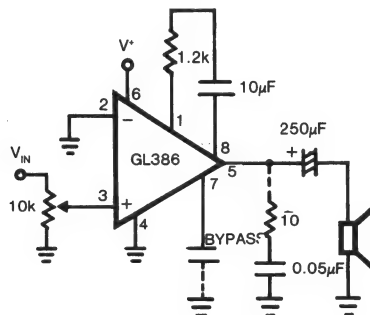


Typical Application

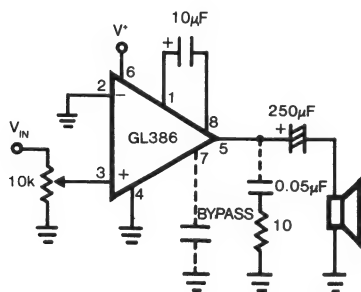
AMPLIFIER WITH GAIN = 20



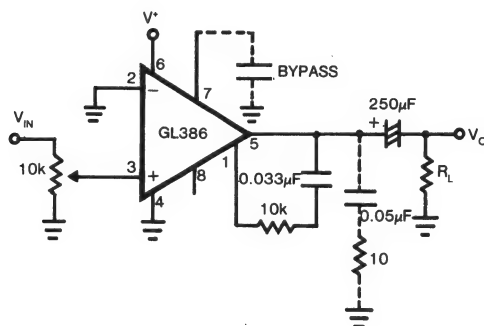
AMPLIFIER WITH GAIN = 50



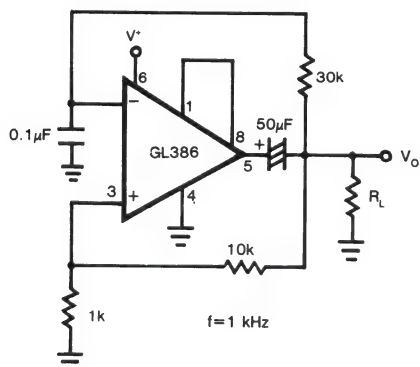
AMPLIFIER WITH GAIN = 200



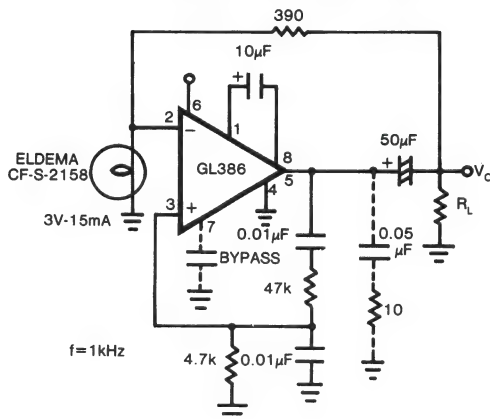
AMPLIFIER WITH BASS BOOST



SQUARE WAVE OSCILLATOR



LOW DISTORTION POWER WIENBRIDGE OSCILLATOR



GL3230

DUAL VOLUME/BALANCE/TONE (BASS/TREBLE) DC CONTROL IC

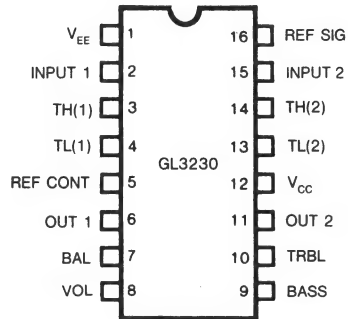
Description

The GL3230 is a DC controlled dual volume, balance, tone (BASS, treble) IC. As these dual channels are constructed on one chip, this IC is excellent in pair characteristic. It is suitable for automobile stereo, radio cassette, music center, TV multiplex sound receiver and remote controlled applications.

Feature

- **Wide Power Supply Voltage Range;**
Single Supply $V_{CC(opr)} = 8 \sim 14V$
Dual Supply $V_{CC} - V_{EE(opr)} = \pm 4 \sim \pm 7V$
- **Wide Volume Control Range:** $V_R = 80dB$ (Typ.)
- **Excellent Cross Talk:** $CT = 70dB$ (Typ.)
- **Stable for Temperature Drift.**
- **Wide Tone Control Range**
Control Range: $V_B = 10dB$ (Typ.) at $f = 1kHz \rightarrow 100Hz$
 $V_T = 12dB$ (Typ.) at $f = 1kHz \rightarrow 20kHz$

Pin Configuration (Top View)



Absolute Maximum Ratings

Supply voltage	V_{CC}	14	V
Power Dissipation (Note)	P_D	750	mW
Operating Temperature	T_{OPR}	-25 to 75	°C
Storage Temperature	T_{STG}	-55 to 150	°C

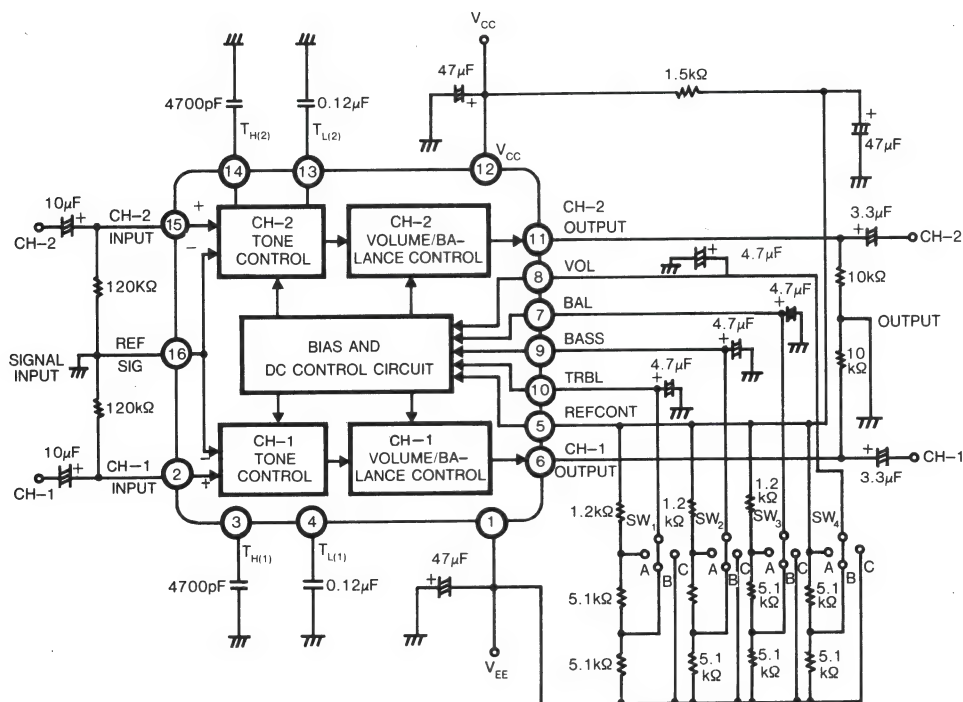
Note: Derated above $T_A = 25^\circ C$ in the proportion of $6mW/^\circ C$.

Electrical Characteristics

(Unless otherwise specified, $V_{CC}=6V$, $V_{EE}=-6V$, $f=1kHz$, $T_A=25^{\circ}C$)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT
Quiescent Current	$I_{CCQ(1)}$	$V_{OL}/BAL/BASS/$	$V_{CC}, V_{EE}=\pm 4V$	—	11	17	mA
	$I_{CCQ(2)}$	$SW_{1\sim 4}:B$		10	18	25	
Maximum Input Voltage	V_{IN}	BASS/TRBL/BAL $SW_{1\sim 3}:B$		—	—	1	Vrms
Maximum Output Voltage	V_{OUT}	VOL $SW_4:A$, THD=1%		1	—	—	Vrms
Voltage Gain	G_V	BASS/TRBL/BAL $SW_{1,3}:B$		-0.5	2.0	4.5	dB
Channel Balance	C.B-1	$V_{IN}=1V_{rms}$, $V_{OL} SW_4:A$		-3	0	3	dB
	C.B-2	VOL/BAL/BASS/TRBL $SW_{1\sim 4}:B$ $V_{IN}=0.1V_{rms}$ $f=100Hz\sim 20kHz$		-3.5	0	3.5	
Volume Control Range	V_R	BASS/TRBL/BAL $SW_{1\sim 3}:B$ $V_{OL} SW_4:A\rightarrow C$ $V_{IN}=1V_{rms}$		70	80	—	dB
Bass Control Range	V_B MAX	V_{OL}/BAL $SW_{3,4}:B$	BASS/TRBL $SW_{1,2}:A$	7	11	14	dB
	V_B MIN	$V_{IN}=1V_{rms}$ $f=1kHz\rightarrow 100Hz$	BASS/TRBL $SW_{1,2}:C$	-15	-11.5	-7	
Treble Control Range	V_T MAX	V_{OL}/BAL $SW_{3,4}:B$	BASS/TRBL $SW_{1,2}:A$	7	11	14	dB
	V_T MIN	$V_{IN}=1V_{rms}$ $f=1kHz\rightarrow 20kHz$	BASS/TRBL $SW_{1,2}:C$	-20	-14	-10	
Tone Error	ΔG	VOL/BAL $SW_{3,4}:B$, $V_{IN}=1V_{rms}$ BASS/TRBL $SW_{1,2}:C\rightarrow A$		—	6	10	dB
Total Harmonic Distortion	THD	BASS/TRBL/BAL $SW_{1\sim 3}:B$ VOL $SW_4:A$, $V_O=150mV_{rms}$		—	0.1	0.35	%
Output Noise Voltage	V_{NO}	BASS/TRBL/BAL $SW_{1\sim 3}:B$ VOL $SW_4:A$ BPF=50Hz~20kHz INPUT OPEN		—	130	300	μV_{rms}
Cross Talk	CT	BASS/TRBL/BAL $SW_{1\sim 3}:B$ VOL $SW_4:A$, $V_{OUT}=1V_{rms}$		—	70	—	dB
Control Terminal Input Resitance	R_{IN}	8, 9, 10 PIN		—	500	—	k Ω
		7 PIN		—	200	—	

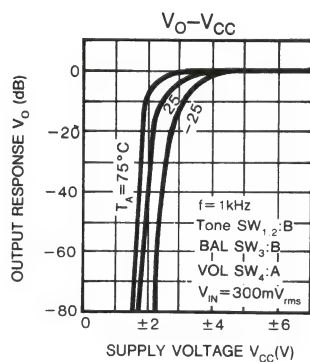
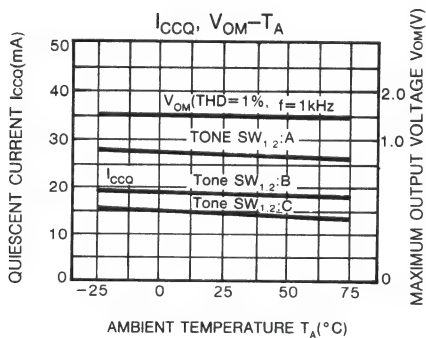
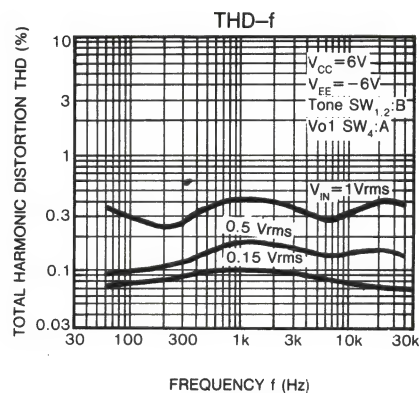
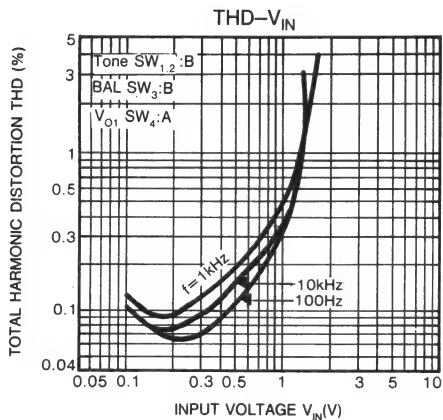
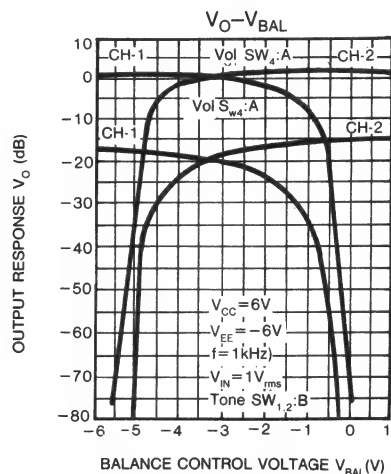
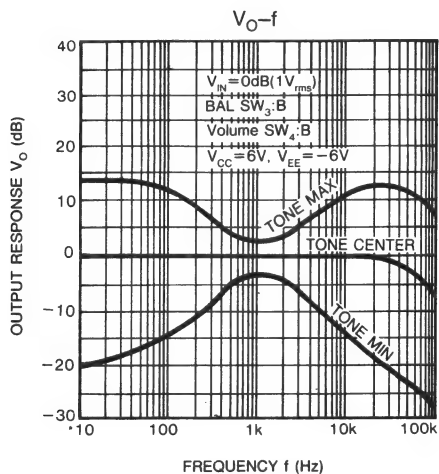
Test Circuit/ Block Diagram

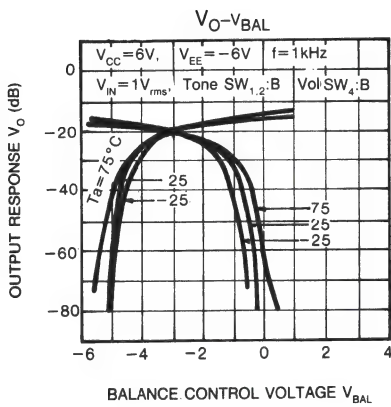
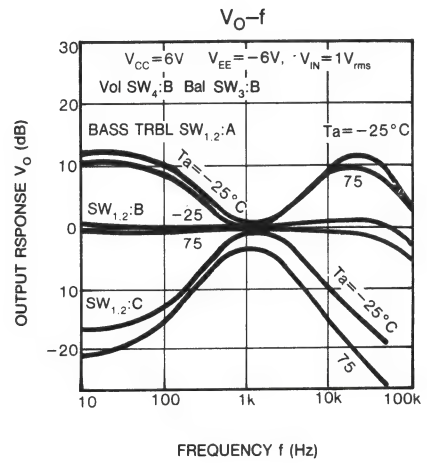
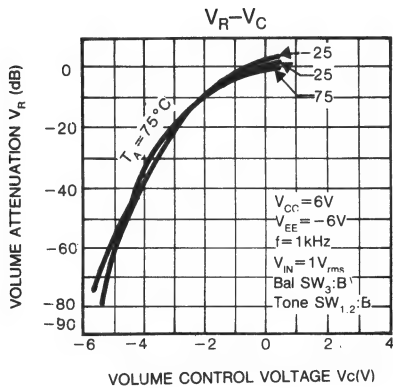


Pin Connection

PIN NO.	SYMBOL	EXPLANATION	PIN NO.	SYMBOL	EXPLANATION
1	V_{EE}	Negative power supply	9	BASS	Bass control
2	INPUT-1	Input channel 1	10	TRBL	Treble control
3	TH(1)	Treble turning frequency setting	11	Output-2	Output channel 2
4	TL(1)	Bass turning frequency setting.	12	V_{CC}	Power supply
5	REF CONT	Reference control	13	TL(2)	Bass turning frequency setting
6	OUTPUT-1	Output channel 1	14	TH(2)	Treble turning frequency setting
7	BAL	Balance control	15	INPUT-2	Input channel 2
8	VOL	Volume control	16	REF SIG	Reference signal

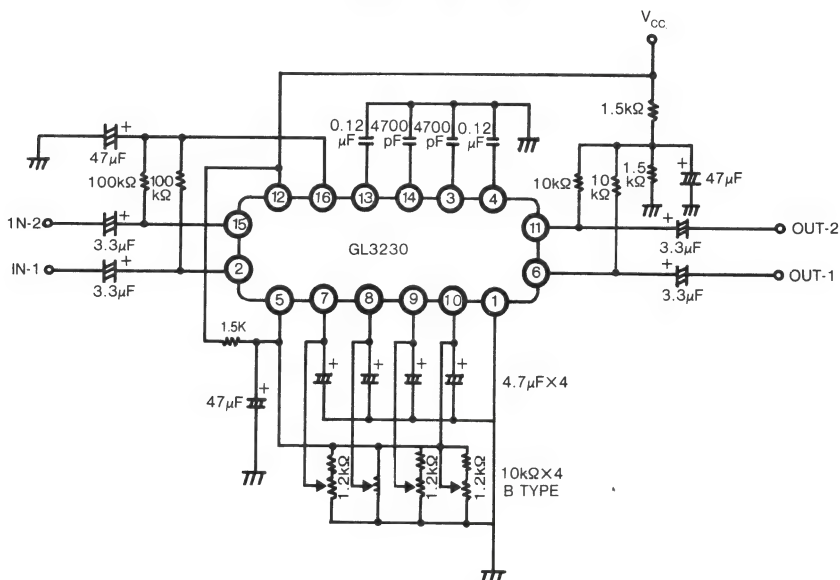
Typical Performance Curves



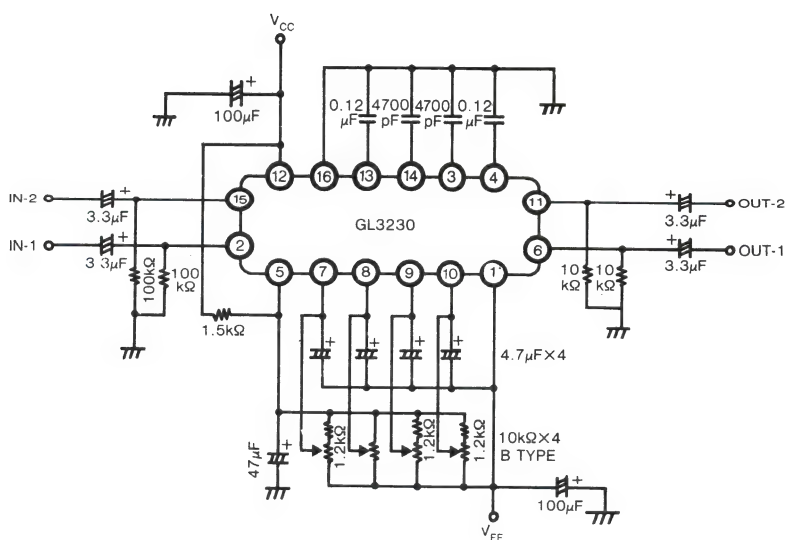


Typical Application

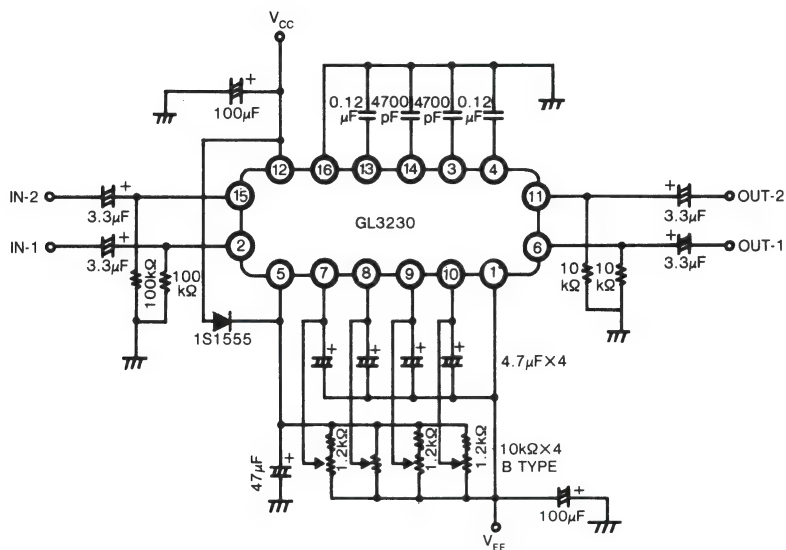
1. Single Power Supply



2. Dual Power Supply



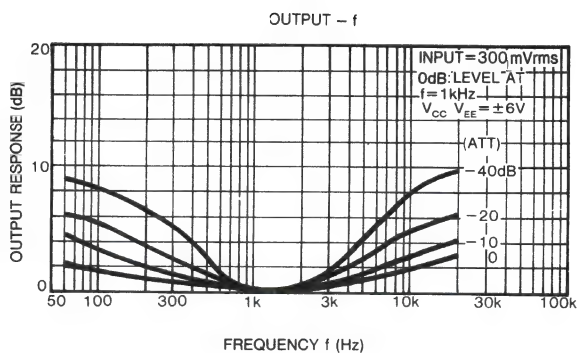
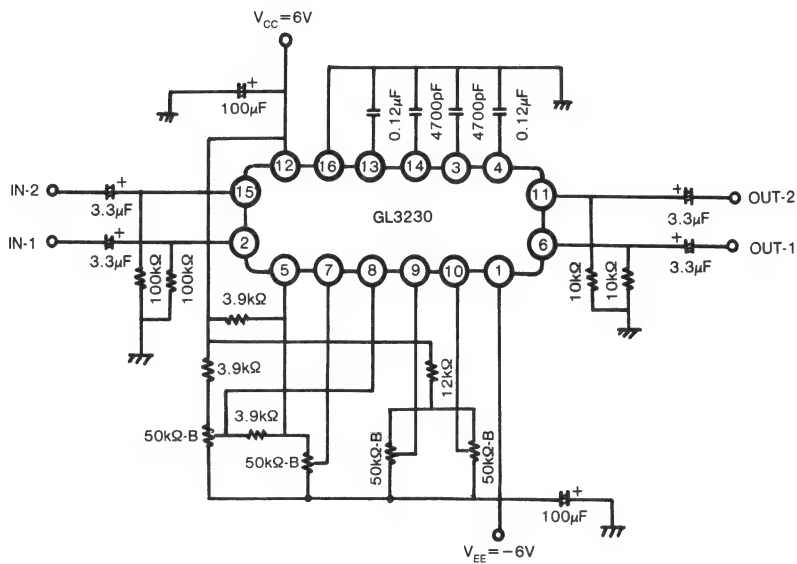
3. Application Circuit Using Diode at Reference Terminal



The application circuit using diode between Pin 5 and Pin 12 has the following merits.

1. When each control terminal is driven by high impedance, the electrolytic capacitor between terminal 5 and GND operates as the back up capacitor, so that the rise time is short at the ON-OFF repetition of supply voltage.
2. When the current drain into the each control terminal varies by control voltage, the voltage of terminal 5 scarcely varies. It means a stable reference voltage.

4. Quasi-Loudness Circuit



GL3630

CDP SERVO CONTROL

Functions

- GL3630 is a Bipolar IC Designed for CD Servo.
- HF (Sensor Output) Amplification
- Focus Error Amplification & Focus Drive Amplification
- Including Focus Search Circuit
- Focus ON Detection
- Tracking Error Amplification & Tracking Drive Amplification
- Tracking Jump Control.
- Tracking Zero Cross Detection
- HF Detection
- Tracking Drive Limiter
- Feed Servo Drive Amplification
- Disc Servo Drive Amplification

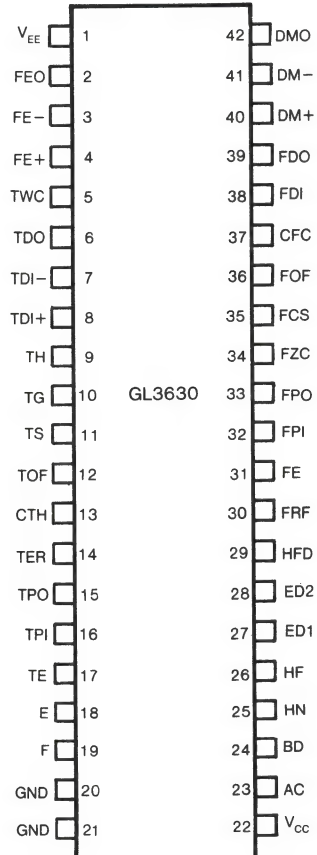
Features

- Easy to use GL3630 in 3 Laser Beam Pick up System.
- One Chip CD Analog Servo.
- GL3630 Contains HF Pre-Amp.
- Possible to use GL3630 for Another Optical Disc Servo.

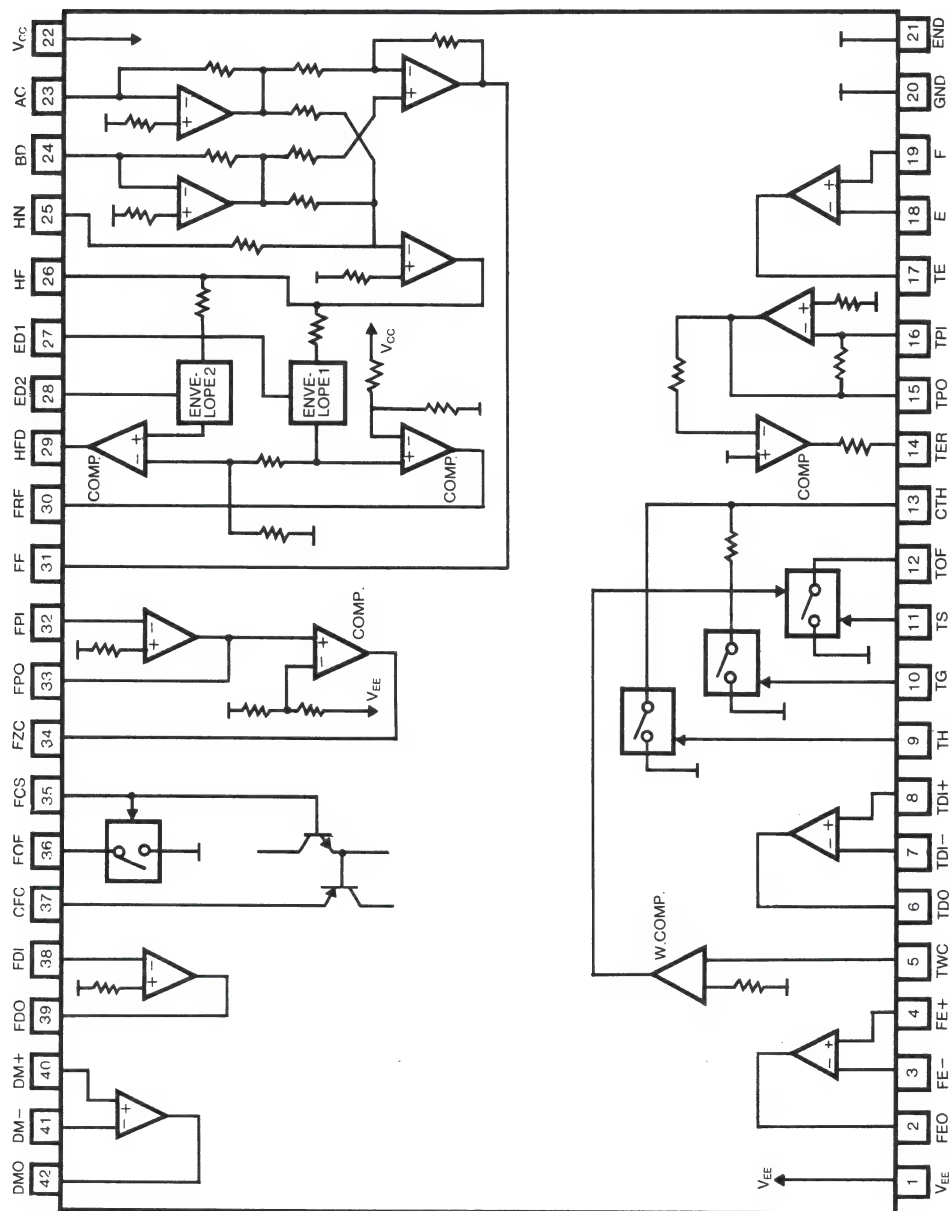
Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage	V_{CC}/V_{EE}	$\pm 8\text{V}$
Power Dissipation	P_D	700mW
Operating Temperature	T_{OPR}	-25 to $+75^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 125°C

Pin Configuration



Block Diagram



Electrical Characteristics: $T_A = 25^\circ\text{C}$, $V_{CC}/V_{EE} = \pm 5\text{V}$, $f = 1\text{kHz}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}/V_{EE}		± 4.5	± 5	± 7.5	V
Quiescent Current	I_{CC}			11	17	mA
Quiescent Current	I_{EE}			12	18	mA
HF-Amp Output Voltage	V_{HF}	$V_{in} = 10\text{mV}_{p-p}$, $f = 2\text{MHz}$	0.7	1.3	2.2	V_{p-p}
Focus Offset Voltage	V_{FEO}		-0.5	2.3	4.3	V
Tracking Offset Voltage	V_{TEO}		-0.49	-0.09	0.19	V
FRF Comparator Threshold Voltage	V_{thF}	When V_6 is high with increasing E_3	0.25	0.38	0.51	V
HFD Comparator Threshold Value	T_{hD}	$V_{in} = 10\text{mV}_{p-p}$, $f = 1\text{MHz}$ when V_5 is high with increasing E_3	0.33	0.39	0.51	—
FZC Comparator Threshold Voltage	V_{thC}	When V_8 is high with increasing E_3	-0.25	-0.15	-0.09	V
TER Comparator Threshold Voltage	V_{thR}	When V_2 is Low with decreasing E_2	-0.45	-0.10	0.25	V
Focus off Attenuation Rate	ATT_{FOF}	$V_{in} = 10\text{mV}_{p-p}$ E_4 : 0V/5V	24	33		dB
Tracking S/W Attenuation Rate 1	ATT_{TOF1}	$V_{in} = 10\text{mV}_{p-p}$ 11 Pin: 0V/5V	39	53		dB
Tracking S/W Attenuation Rate 2	ATT_{TOF2}	$V_{in} = 10\text{mV}_{p-p}$ 10 Pin: 0V/5V	2.2	4.5	6.9	dB
Tracking S/W Attenuation Rate 3	ATT_{TOF3}	$V_{in} = 10\text{mV}_{p-p}$ 9 Pin: 0V/5V	22	28	35	dB
Tracking S/W Attenuation Rate 4	ATT_{TOF4}	$V_{in} = 10\text{mV}_{p-p}$ $E_1 = 0\text{V}/\pm 1\text{V}$	42	53		dB
DM-Amp Output Voltage	V_{DM}	$V_{in} = 1 V_{rms}$	0.85	1.00	1.15	V_{rms}
FEM-Amp Output Voltage	V_{FEM}	$V_{in} = 1 V_{rms}$	0.85	1.00	1.15	V_{rms}
Focus Search Voltage	V_{FS}	$E_4 = 5\text{V}$	-1.11	-0.85	-0.59	V
Focus Output Voltage	V_{FDO}	$V_{in} = 0.5 mV_{rms}$	0.5	0.85	1.10	V_{rms}
Tracking Output Voltage	V_{TDO}	$V_{in} = 5\text{mV}_{p-p}$	1.16	1.65	2.15	V_{p-p}
Focus Search Offset Voltage	V_{FSO}	$E_4 = 5\text{V}$	-40	0	40	mV
Tracking Pre-Amp Slew Rate	T_{SR}	$V_{in} = \pm 3 V_{p-p}$ Rectangular wave $f = 1\text{kHz}$	0.15			$\text{V}/\mu\text{S}$
Tracking Drive-Amp Slew Rate	T_{DSR}	$V_{in} = \pm 3 V_{p-p}$ Rectangular wave $f = 1\text{kHz}$	0.15			$\text{V}/\mu\text{S}$

Test Method

ITEM	SYMBOL	SWITCH CONDITIONS										BIAS				INPUT	TEST POINT
		1	2	3	4	5	6	7	8	14	15	16	E ₁	E ₂	E ₃	E ₄	
Quiescent Current	I _{CC}	ON	GND	GND	GND	OPEN	OFF	OFF	OFF	ON	1	1	0V	—	—	0V	I ₁
	I _{EE}	OFF	GND	GND	GND	OPEN	ON	OFF	OFF	ON	1	1	0V	—	—	0V	I ₂
HF Amp Output Voltage	V _{HF}	ON	GND	GND	GND	OPEN	ON	ON	ON	ON	1	1	0V	—	0V	0V	V ₄
Focus Offset Voltage	V _{FEO}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	1	1	0V	—	—	0V	V ₁₀
Tracking Offset Voltage	V _{TEO}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	1	1	0V	—	—	0V	V ₁
FRF COMP. Threshold Voltage	V _{thF}	ON	GND	GND	GND	OPEN	ON	ON	ON	ON	1	1	0V	—		0V	V ₄
HFD COMP. Threshold Value	V _{hD}	ON	GND	GND	GND	OPEN	ON	ON	ON	ON	1	1	0V	—		0V	V ₄ , V ₄
FZC COMP. Threshold Voltage	V _{thC}	ON	GND	GND	GND	OPEN	ON	ON	ON	ON	1	1	0V	—		0V	V ₇
TER COMP. Threshold Voltage	V _{thR}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	1	1	0V		—	0V	V ₃
Focus off Attenuation	ATT _{FOF}	ON	GND	GND	GND	OPEN	ON	ON	OFF	ON	1	1	0V	—	0V	0V	V ₅
Tracking SW Attenuation 1	ATT _{TOF1}	ON	GND	GND	GND/5V	OPEN	ON	OFF	OFF	ON	1	1	0V	—	—	0V	V ₃
Tracking SW Attenuation 2	ATT _{TOF2}	ON	GND	GND/5V	GND	e ₂	ON	OFF	OFF	ON	1	1	0V	—	—	0V	V ₃
Tracking SW Attenuation 3	ATT _{TOF3}	ON	GND/5V	GND	GND	e ₂	ON	OFF	OFF	ON	1	1	0V	—	—	0V	V ₃
Tracking SW Attenuation 4	ATT _{TOF4}	ON	GND	GND	GND	e ₂	ON	OFF	OFF	ON	1	1	±1V	—	—	0V	V ₃
DM AMP Output Voltage	V _{DM}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	1	1	0V	—	—	0V	V ₇
FEM AMP Output Voltage	V _{FEM}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	1	1	0V	—	—	0V	V ₇
Focus Search Voltage	V _{FS}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	1	1	0V	—	—	5V	V ₁₀
Focus Output Voltage	V _{FDO}	ON	GND	GND	GND	OPEN	ON	ON	OFF	ON	1	1	0V	—	0V	0V	V ₆
Tracking Output Voltage	V _{TDO}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	1	1	0V	—	—	0V	V ₂
Focus Search Offset Voltage	V _{FSD}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	1	1	0V	—	—	5V	V ₁₀
Tracking PRI Slew Rate	T _{SR}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	2	1	0V	—	—	0V	T ₁
Tracking Driver Slew Rate	T _{DSR}	ON	GND	GND	GND	OPEN	ON	OFF	OFF	ON	2	2	0V	—	—	0V	T ₂

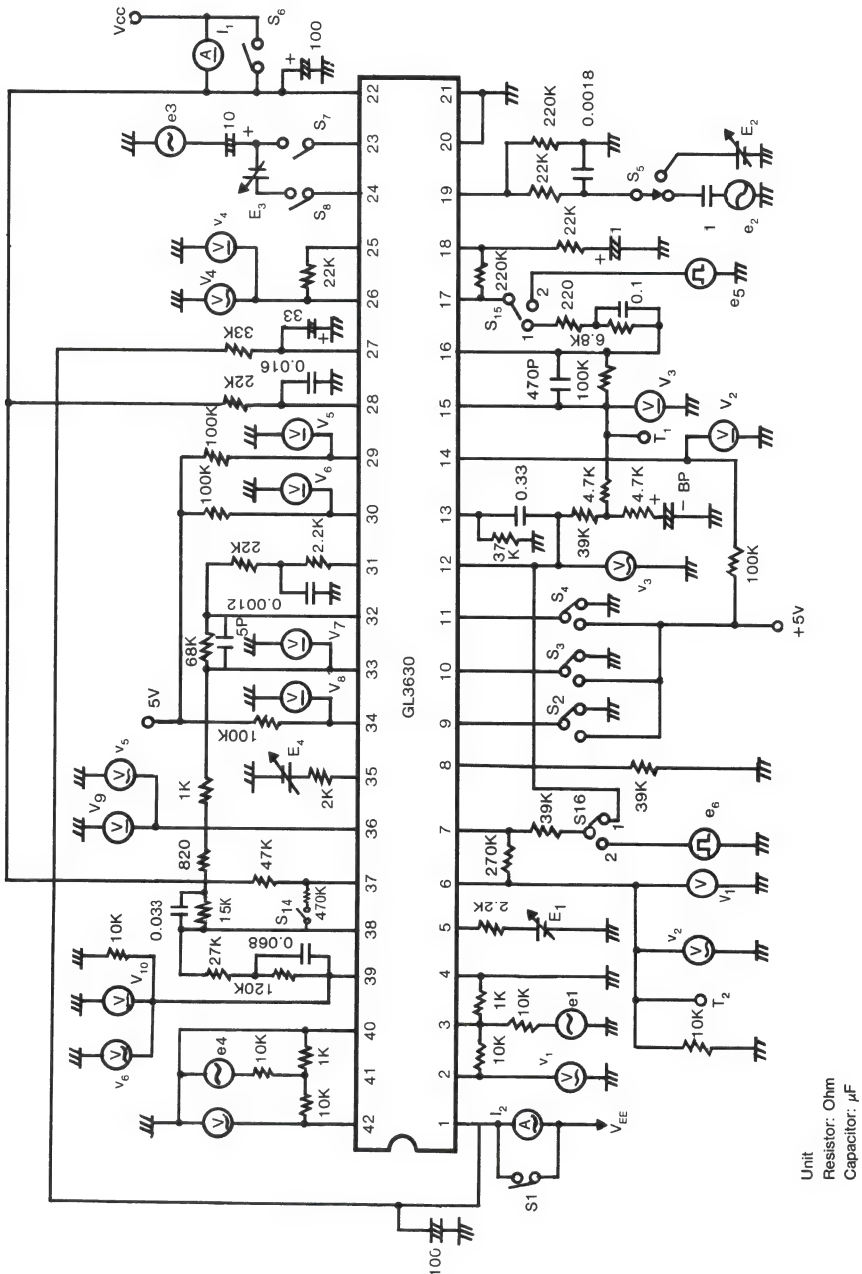
* REMARKS: DC VOLTAGE INCREASING FROM 0V TO 5V.

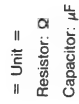
DC VOLTAGE DECREASING FROM 5V TO 0V.

Pin Description

No.	NAME	Explanation	No.	NAME	Explanation
1	V _{EE}	-5V	24	BD	Input Terminal of I-V Converter, B and D are Output Signals of Main Spot Sensors
2	FEO	Feed Amp Output which is used for driving Feed Motor	25	HN	Negative Feed Back Terminal of HF-Amp.
3	FE-	Feed Amp Inputs	26	HF	Summing Output Signal of Main Spot Sensors
4	FE+	Feed Amp Inputs	27	ED1	Peak Hold Pin of HF Signal. It is designed for holding time constant following 30 kHz traverse.
5	TWC	Tracking Drive Limiter Terminal	28	ED2	Bottom Hold Pin of HF Signal
6	TDO	Tracking Drive Amp Output which is Driving Tracking Actuator.	29	HFD	HF Drop Detection. Output is Low ON the track Output is high in drop out and between tracks
7	TDI-	Tracking Drive Amp Inputs	30	FRF	Generating Focus ON Signal
8	TDI+	Tracking Drive Amp Inputs	31	FE	Focus Error Output
9	TH	Tracking Hold Switch	32	FPI	Focus Pre-Amp Input
10	TG	Gain Control Switch	33	FPO	Focus Pre-Amp Output
11	TS	Tracking OFF Switch	34	FZC	Focus Zero Cross Detection
12	TOF	TS Control Terminal	35	FCS	Input Terminal for Focus Search Control.
13	CTH	TH, TG Control Terminal	36	FOF	Focus Servo OFF Switch on Focus Search.
14	TER	Output of Tracking Zero Crossing Comparator	37	CFC	Pin for Controlling Focus Drive Amp on the Focus Search.
15	TPO	Tracking Pre-Amp Output	38	FDI	Focus Drive Amp Input.
16	TPI	Tracking Pre-Amp Input	39	FDO	Focus Drive Amp Output.
17	TE	Tracking Error Output Converted from the Differential Current of Two Photo Diodes (that is, sub-spot sensors)	40	DM+	Disc Motor Drive Amp Inputs.
18	E	Input Terminal of Tracking Error Generating Amp. that is, Sensor Output.	41	DM-	Disc Motor Drive Amp Inputs.
19	F	Same as 18 Pin.	42	DMO	Disc Motor Drive Amp Output.
20	GND	Ground			
21	GND	Ground			
22	V _{CC}	+5V			
23	AC	Input Terminal of I-V Converter, A and C are Output Signals of Main Spot Sensors.			

Test Circuit





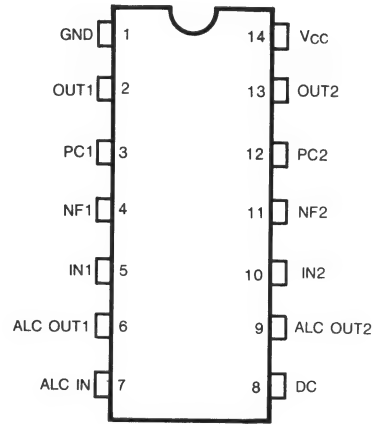
GL5501

AUDIO EQ AMP

Features

- DIP 14 PIN (Dual In-Line Package)
- Dual pre-amp with built-in ALC (pre-amp×2+ALC×2)
- Due to high gain, recording amp can be formed separately. (Variable Monitor Possible)
- ALC and director motor drive obtained through SEPP output stage.
- Good ALC response balance between channels.
- Good lessening of voltage characteristic.
- Excellent channel separation.
- Quick stabilization during power supply input.

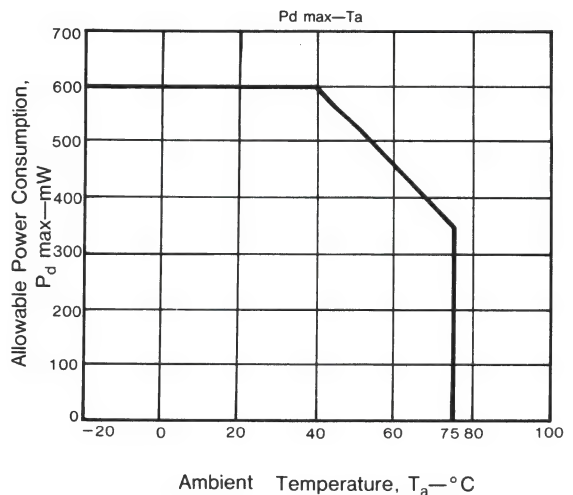
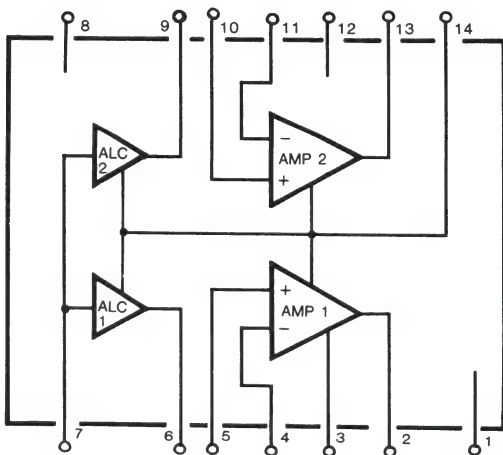
Pin Configuration



Description

The GL5501 is a dual preamplifier with ALC (Automatic Level Control) designed for use in a record playback amplifier of tape recorder. It is suitable for a stereo set and a radiocassette recorder.

Block Diagram



Maximum Ratings/ $T_a = 25^\circ\text{C}$

PARAMETER	SYMBOL		RATING	UNIT
Maximum power supply voltage	V_{CC} max	$T_a \leq 40^\circ\text{C}$	14	V
Allowable power consumption	P_d max		600	mW
Operating ambient temperature	T_{OPR}		$-20 \sim +75$	$^\circ\text{C}$
Storage ambient temperature	T_{stg}		$-40 \sim +125$	$^\circ\text{C}$
ALC Tr. allowable current			3.5	mA

Recommended Operating Conditions/ $T_a = 25^\circ\text{C}$

PARAMETER	SYMBOL		RATING	UNIT
Recommended power supply Voltage	V_{CC}		5 ~ 13	V
Load resistance	R_L		not less than 680	Ω

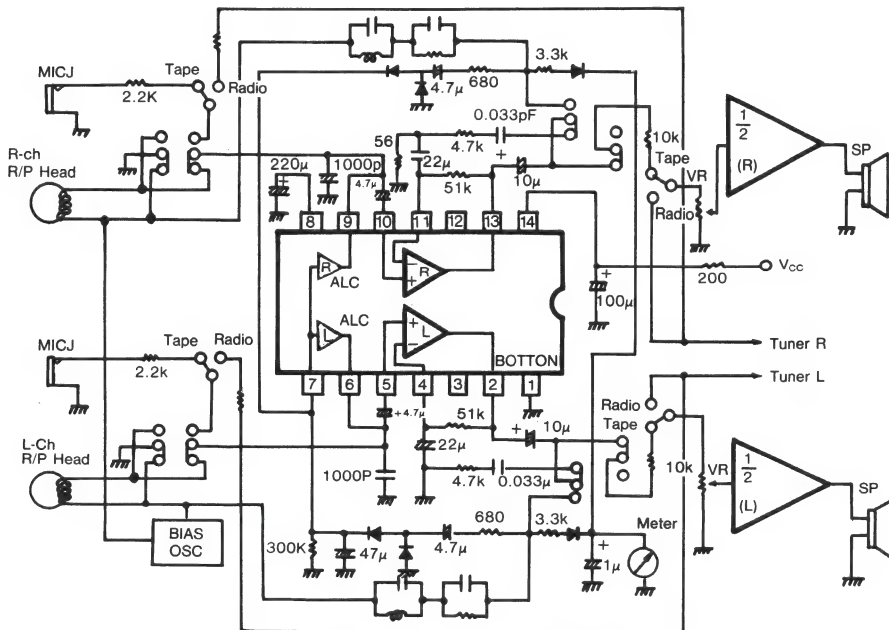
Operating Characteristics/ $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $f = 1\text{ kHz}$, $R_L = 10\text{ k}\Omega$ (PLAY), $R_L = 680\Omega$ (REC)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent current	I_{CCO}			4.5	10	mA
Open voltage gain	VG_O			85		dB
Voltage gain	VG	PLAY		40		dB
		REC		58		dB
Maximum output voltage	v_o max	THD = 1%, PLAY	0.9	1.2		V
Total harmonic distortion	THD	$v_o = 0.5\text{V}$, PLAY		0.1	1.0	%
Input resistance	r_i		21	30		$\text{k}\Omega$
Channel separation	SEP	$R_g = 2.2\text{ k}\Omega$, $v_o = 0\text{ dBm}$, PLAY	40	50		dB
Noise voltage converted to input	V_{NI}	$R_g = 2.2\text{ k}\Omega$, B.P.F. = 20 Hz~20 kHz, PLAY		1.0	2.0	μV
ALC width		$v_i = -60\text{ dBm}$, REC	35	45		dB
ALC balance		$v_i = -20\text{ dBm}$, REC		0	2.0	dB
ALC distortion		$v_i = -20\text{ dBm}$, REC		0.5	2.0	%

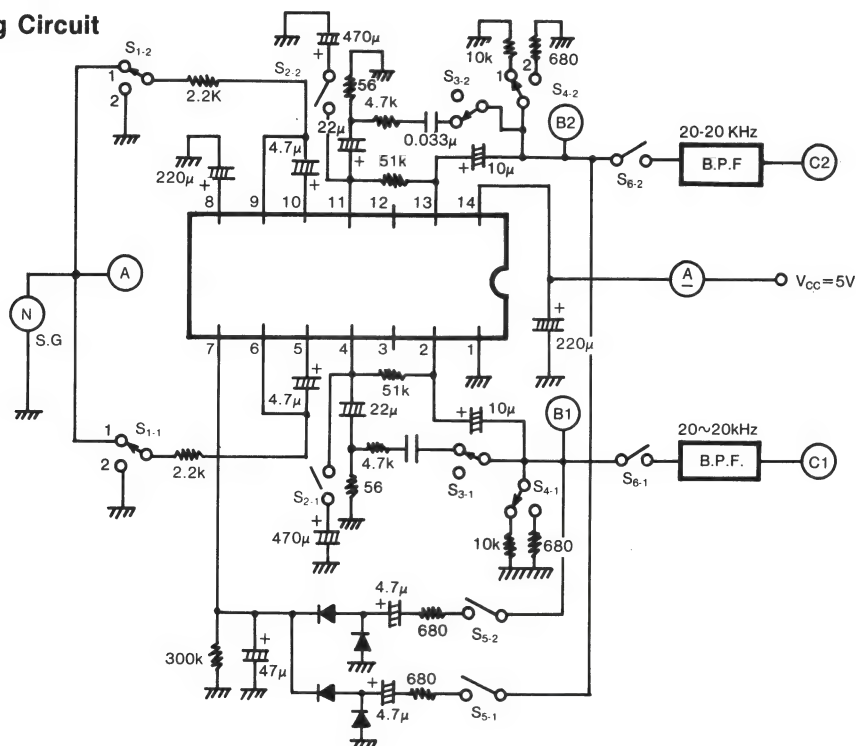
Measurement Procedure

Item	S1	S2	S3	S4	S5	S6	Measurement location	Procedure
I_{CCO}	2	off	off	1	off	off	—	Read ammeter.
VG_O	1	on	off	1	off	off	A,B	Measure at $VG_O = 20 \log V_O/V_I$ (dB) with input voltage at V_I ; output voltage at V_O
VG	1	off	on	1	off	off	A,B	$VG = 20 \log V_O/V_I$ (dB)
V_O max	1	off	on	1	off	off	B	Measure output voltage V_O at THD = 1%
THD	1	off	on	1	off	off	B	Measure distortion factor at $V_O = 0.5V$
SEP	S_{1-1} S_{1-2} 1 2 2 1	off	on	1	off	off	B	Measure crosstalk of amp 1, 2 at output voltage $V_O = 0$ dBm
V_{NI}	2	off	on	1	off	on	C	Convert output noise voltage at 1 kHz gain when $R_g = 2.2$ k
ALC width	1	off	off	2	on	off	B	Input voltage range from when input voltage $V_I = -60$ dBm until output voltage V_O goes up 3 dB
ALC balance	1	off	off	2	on	off	B	Output voltage V_O level difference of amp 1,2 when input voltage $V_I = -20$ dBm is applied.
ALC distortion	1	off	off	2	on	off	B	Measure distortion factor when input voltage $V_I = -20$ dBm is applied.

Example of Application Circuit: Variable Monitor System

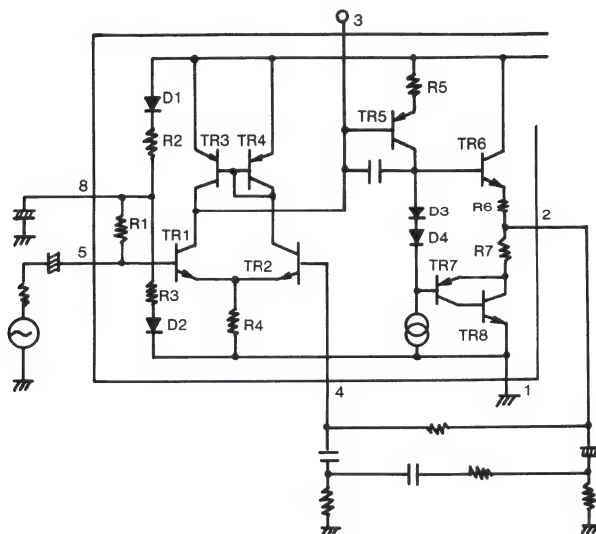


Measuring Circuit



1. Circuit Construction

- 1) This is a dual pre-amp composed of AMP x 2, ALC x 2. Input is obtained from NPN differential TR1, TR2; and differential load uses active element TR3 to obtain high voltage gain. The output stage is push-pull system with drive for low load impedance, and can be directly connected to ALC circuit and meter circuit. Also, because the amp open loop gain is sufficiently high, it can be used for recording amp and variable monitor is possible. Input impedance is determined by built-in resistor R1, and is 30 kΩ.

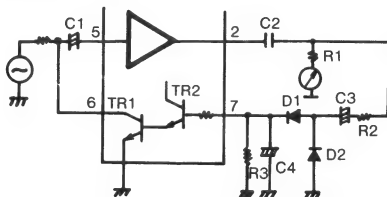


2. ALC Circuit

The ALC circuit is composed of TR1, TR2, and due to DC voltage applied to the 7 control terminals, allows variable impedance between TR1 collector and emitter and controls pre-amp input level.

1. Attack Time and Recover Time

Attack time is between when input signal is applied until ALC begins to operate. Recover time is between when R2, C3 time constant and input signal disappear to when amp level returns to the original level. These are adjusted by C4, R3 time constant. The rectification circuit, which obtains ALC control voltage, should be a double voltage circuit with superior compression ratio. Also, for low voltage 6 V sets, etc., a germanium diode is recommended for D1, D2.



2. Closed loop gain VG (f = 1 kHz)

Closed loop voltage gain is gotten at (f = 1 kHz) $VG \approx 20 \log Z1/Z3$

$$\text{if } Z1 = 7.2 \text{ k}\Omega$$

$$Z3 = 56 \Omega$$

$$VG = 20 \log 7.2 \times 10^3 / 56 \text{ becomes } = 42 \text{ dB}$$

Therefore, equalizer response is determined by these constants.

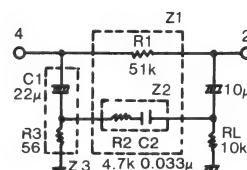
So, playback amp gain is:

a. $20 \log R1/R3$ in low frequency regions

b. $20 \log Z2/Z3$ in high frequency regions

Recording amp gain is

$$VG = 20 \log R1/R3$$

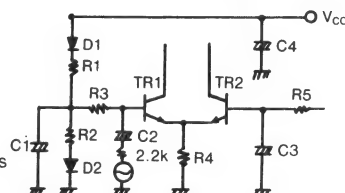


3. External Constants

External constants are related to the operation starting time of the amp. The operation starting time is designed to be within 0.2 sec, but in this case it is necessary that the differential TR1 and TR2 is the same time constant. The condition is:

$$C1(R1/R2) = R5 \cdot C3$$

Example: If $C1 = 220 \mu\text{F}$, $R1/R2 = 5 \text{ k}\Omega$, $R5 = 51 \text{ k}\Omega$ then $C3$ is $22 \mu\text{F}$.



- C1 is a decoupling capacitor, and its capacity changes the ripple rejection rate. (If capacity is large, ripple rejection rate is large.) It is also related to the amp operation starting time, and when R5, C3 time constants are large, C1 must also be made large. The recommended value is $220 \mu\text{F}$.
- C2 is an input capacitor, and more than $4.7 \mu\text{F}$ is recommended.
- C3 is an NF capacitor, and determines the low region cut-off frequency. If C3 is increased, operation starting time lengthens. $10 \mu\text{F}$ is recommended. The recommended time constants therefore are:

R5 (R _F)	C1 (CD)	C2 (IN)	C3 (NF)
51 k~100kΩ	220μF	4.7μF	22μF
220kΩ	330μF	10μF	10μF

We do not recommend more than 200 kΩ for R5 because of the relationship of Amp. operation starting time.

4. Notes on Use

1) Oscillation

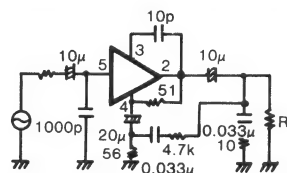
When the amp closed loop gain is lowered, oscillation will occur, so when using it with under 40 dB gain, connect 10pF between pin 3 and pin 2, and $0.033 \mu\text{F}$ (mylar) + 10Ω to the load end. When closed loop gain is below $VG = 30 \text{ dB}$, it should not be used.

2) Wave Obstruction Prevention Use

Connect about 1000pF between input pin (pin 5) and the ground.

3) Maximum Rating

V_{CC} max is $V_{CC} = 14 \text{ V}$ and it should not go over this. The recommended power supply voltage is $5 \text{ V} \sim 13 \text{ V}$.

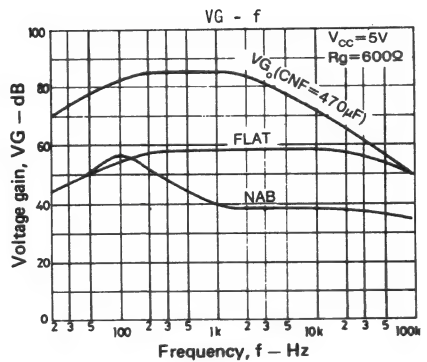
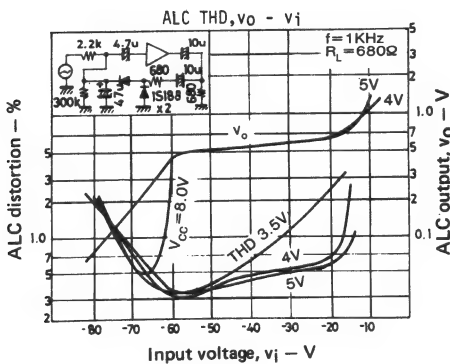
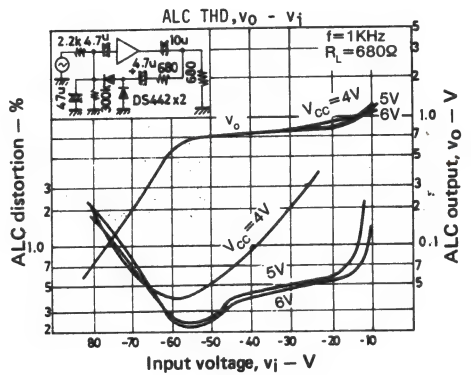
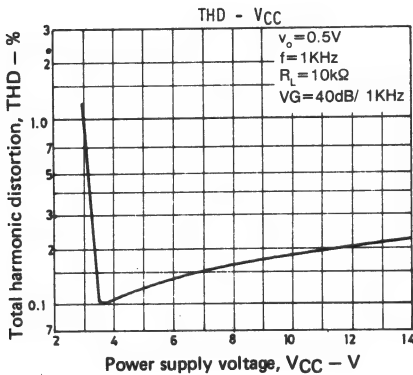
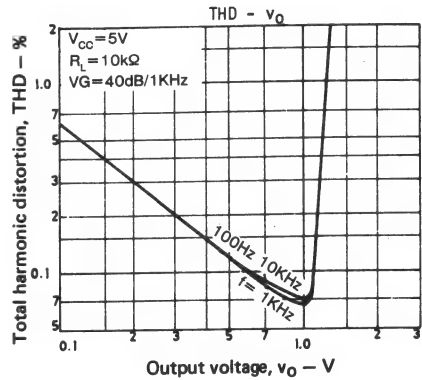
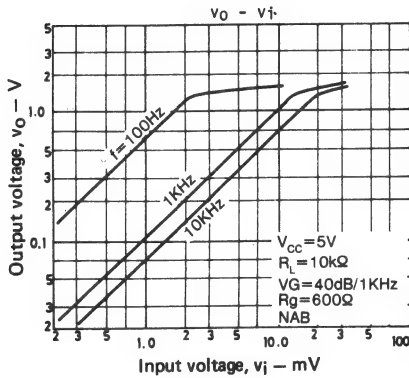


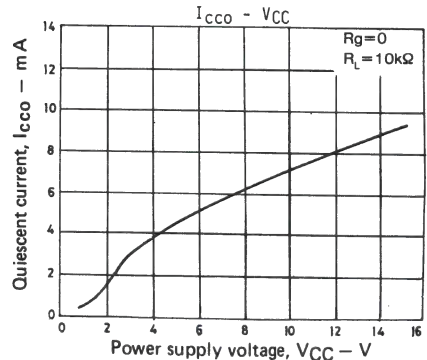
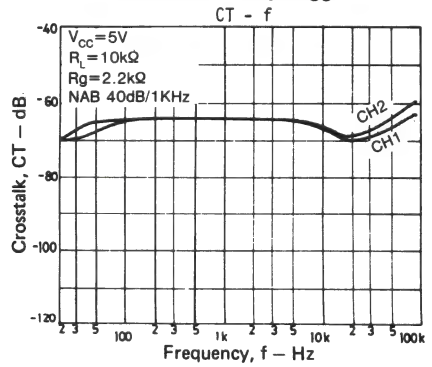
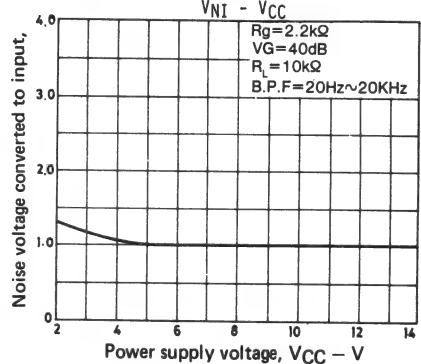
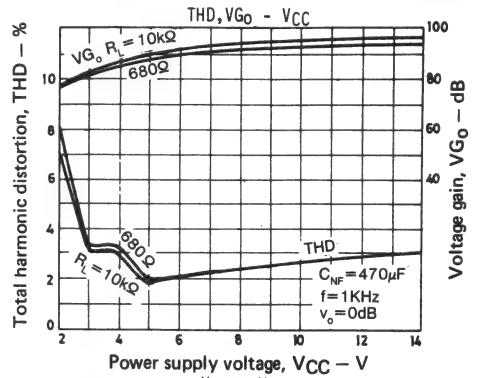
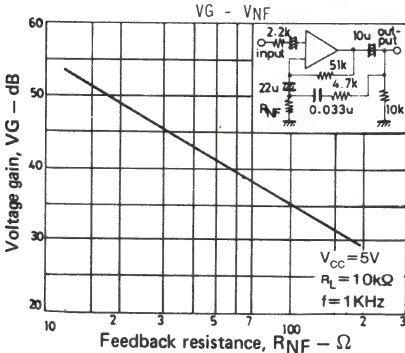
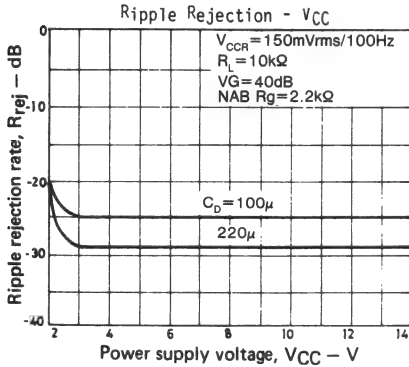
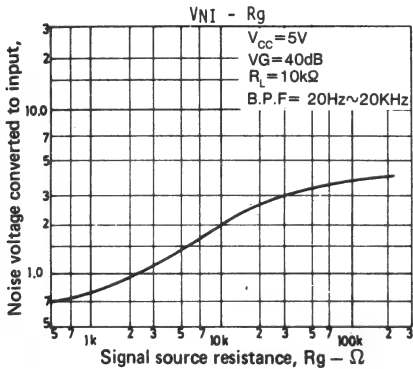
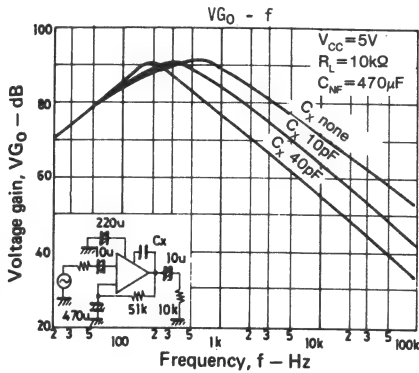
4) Load Impedance

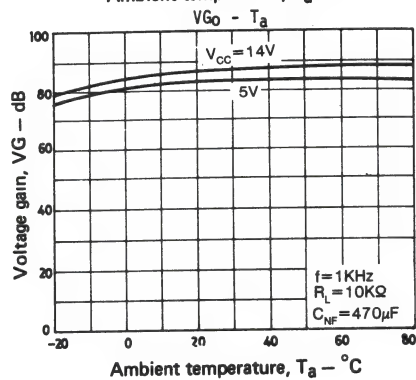
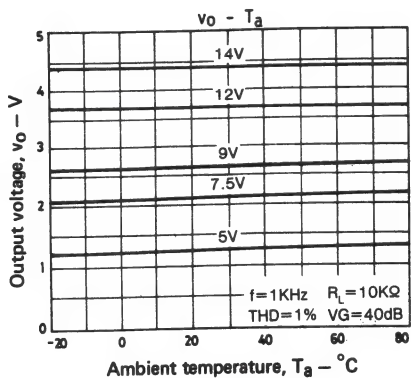
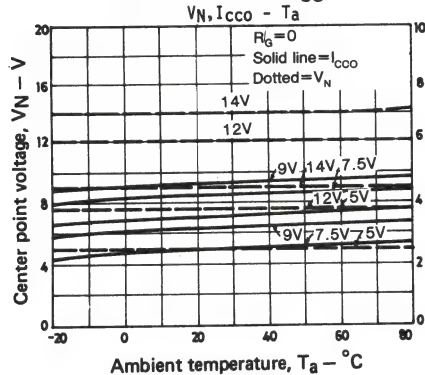
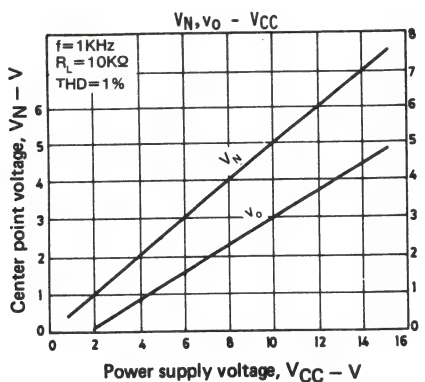
The total load impedance as seen from the output terminal should not be less than 680Ω.

5) A short between pins will cause breakdown or deterioration.

6) A load short will cause breakdown or deterioration.







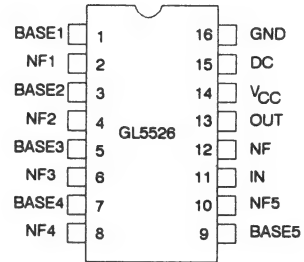
GL5526

5-BAND GRAPHIC EQUALIZER

Description

The GL5526 is 5-band graphic equalizer IC, which have 5 resonance circuit and a output buffer amplifier. This 5 band graphic equalizer for one channel can be formed easily by externally connecting capacitors and variable resistors which fix to (resonance frequency). It is suitable for a portable component stereos, radio cassette recorders & car stereos.

Pin Configuration



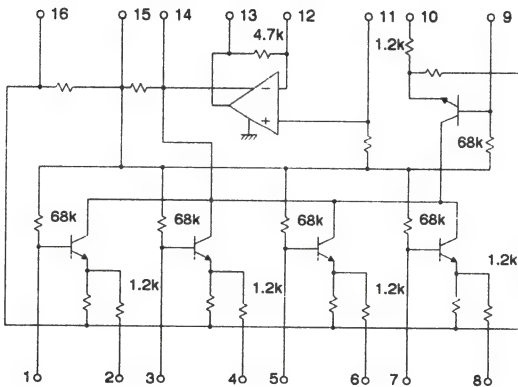
Features

- 16DIP (Dual in-line Package)
- Highly stable to capacitive Load
- Series connection of two GL5526's makes multi-band (6 to 10 bands) available
- Wide Operating Voltage Range : $V_{CC} = 5 \sim 15 \text{ V}$

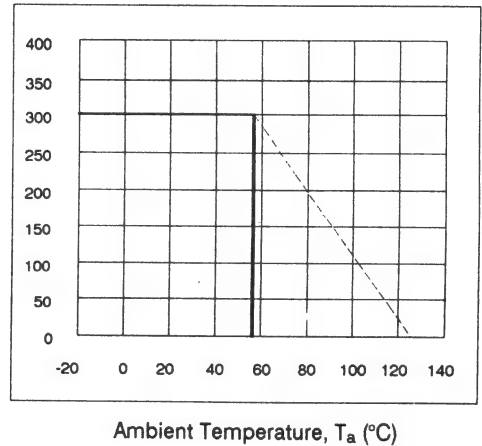
Absolute Maximum Rating ($T_a = 25^\circ\text{C}$)

Supply Voltage	V_{CC}	20 V
Power Dissipation	P_D	300 mW
Operating Temperature	T_{opr}	-20°C to $+75^\circ\text{C}$
Storage Temperature	T_{stg}	-40°C to $+125^\circ\text{C}$

Equivalent Circuit



Allowable Power
Dissipation, P_D (Max.) (mW)



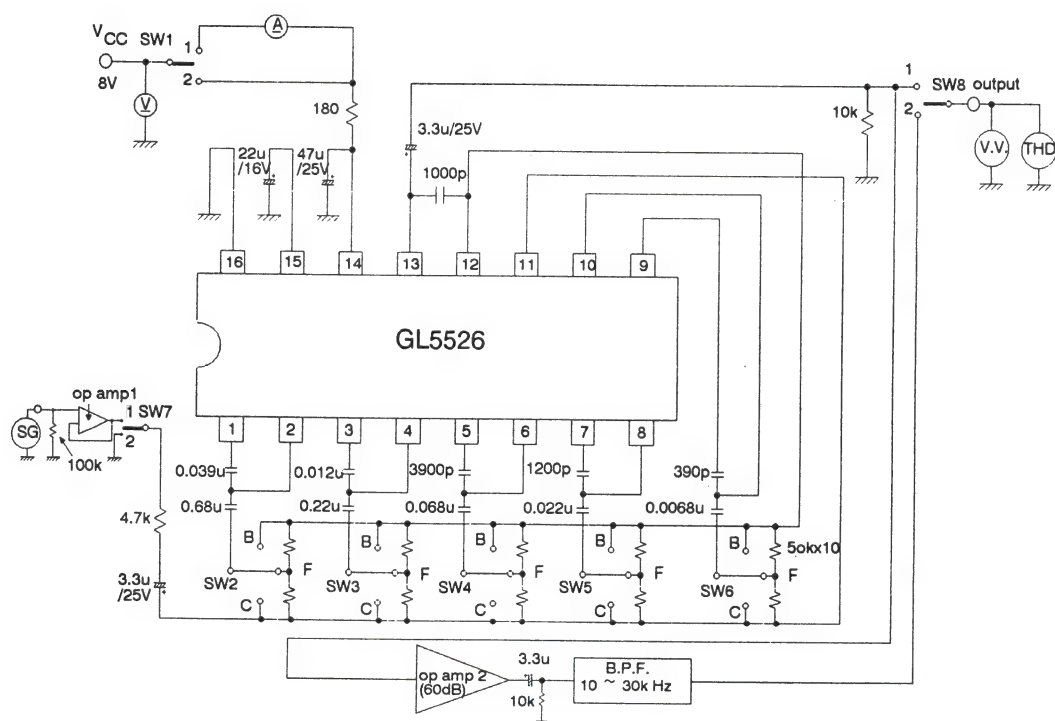
Electrical Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 8\text{V}$, $R_L = 10\text{k}\Omega$, $R_g = 600\Omega$)

PARAMETER	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Quiescent Current	I _{CCQ}			3.0	5.0	8.0	mA
Voltage Gain	VG	f = 1kHz, Vin = -10dB at all flat mode		-3.8	0.8	+2.2	dB
Boost Amount	BOOST	f = 100Hz	V _O = -10dB is taken as 0dB at all flat mode at f = 1kHz.	8	10	12	dB
		f = 340Hz		8	10	12	dB
		f = 1kHz		8	10	12	dB
		f = 3.4kHz		8	10	12	dB
		f = 10kHz		8	10	12	dB
Cut Amount	CUT	f = 100Hz		-12	-10	-8	dB
		f = 340Hz		-12	-10	-8	dB
		f = 1kHz		-12	-10	-8	dB
		f = 3.4kHz		-12	-10	-8	dB
		f = 10kHz		-12	-10	-8	dB
Total Harmonic Distortion	THD	f = 1kHz, V _O = 1.0V		-	0.03	0.1	%
Output Noise Voltage	V _{NO}	R _g = 0, All flat B.P.F. 10Hz to 30kHz		-	2.0	20	uV

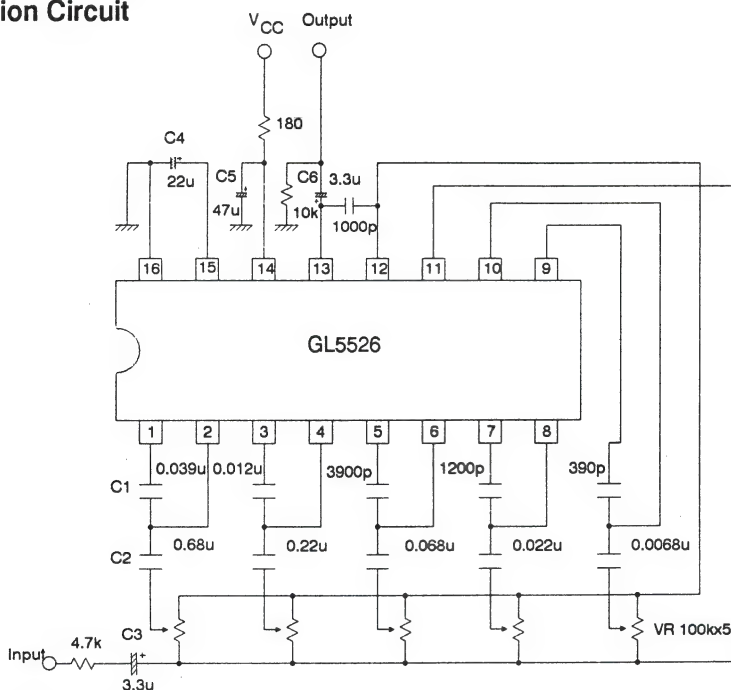
Test Method

ITEM	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	CONDITIONS
I_{CCQ}	1	-	-	-	-	-	2	1	
VG	2	F	F	F	F	F	1	1	$f = 1\text{kHz}$, $V_{in} = -10\text{dB}$
BOOST	2	B	F	F	F	F	1	1	$f = 100\text{Hz}$
BOOST	2	F	B	F	F	F	1	1	$f = 340\text{Hz}$
BOOST	2	F	F	B	F	F	1	1	$f = 1\text{kHz}$
BOOST	2	F	F	F	B	F	1	1	$f = 3.4\text{kHz}$
BOOST	2	F	F	F	F	B	1	1	$f = 10\text{kHz}$
CUT	2	C	F	F	F	F	1	1	$f = 100\text{Hz}$
CUT	2	F	C	F	F	F	1	1	$f = 340\text{Hz}$
CUT	2	F	F	C	F	F	1	1	$f = 1\text{kHz}$
CUT	2	F	F	F	C	F	1	1	$f = 3.4\text{kHz}$
CUT	2	F	F	F	F	C	1	1	$f = 10\text{kHz}$
THD	2	F	F	F	F	F	1	1	$f = 1\text{kHz}$, $V_O = 1.0\text{V}$
V_{NO}	2	F	F	F	F	F	2	2	

Test Circuit



Application Circuit



f_o (resonance frequency)

In the sample application circuit, f_o for each of 5 bands is set as follows:

$f_o = 108\text{Hz}, 343\text{ Hz}, 1.08\text{kHz}, 3.43\text{kHz}, 10.8\text{kHz}$

$$f_o = \frac{1}{2\pi\sqrt{C1 \times C2 \times R1 \times R2}} \quad (R1 = 1.2\text{kohms}, R2 = 68\text{kohms on-chip resistor})$$

Description of external parts

C1, C2 : Capacitors used to fix f_o (resonance frequency)

C3 : Input capacitor. Decreasing the capacitor value lowers the frequency response at low frequencies.

C4 : Decoupling capacitor. Decreasing the capacitor value makes the effect of power supply stronger, whereby ripple is liable to occur.

C5 : Power capacitor.

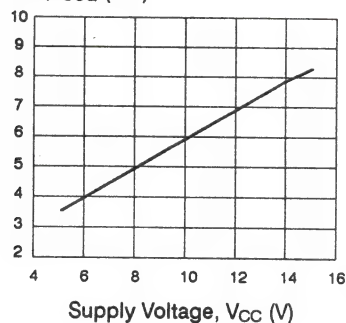
C6 : Output capacitor. Decreasing the capacitor value lowers the frequency response at low frequencies.

Proper cares in using IC

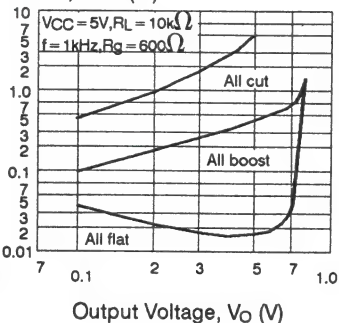
- Maximum supply voltage V_{CC} (Max.) 20V must not be exceeded. The operating voltage is in the range of 5 to 15V
- Application of power with the pin-to-pin spaces shorted causes breakdown or deterioration of the IC to occur. When mounting the IC on the board or applying power, make sure that the pin-to-pin spaces are not shorted with solder, etc.

Typical Performance Characteristics

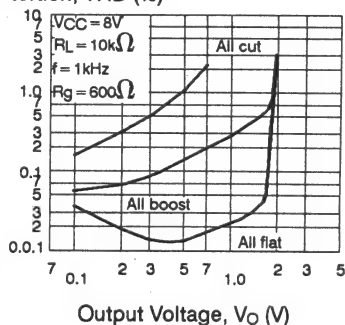
Quiescent Current, I_{CCQ} (mA)



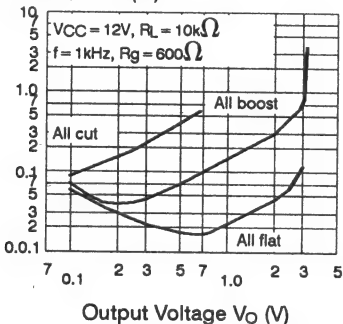
Total Harmonic Distortion, THD (%)



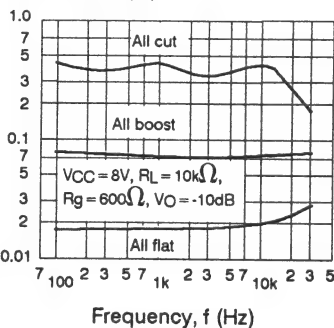
Total Harmonic Distortion, THD (%)



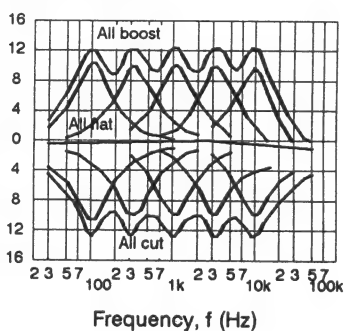
Total Harmonic Distortion, THD (%)



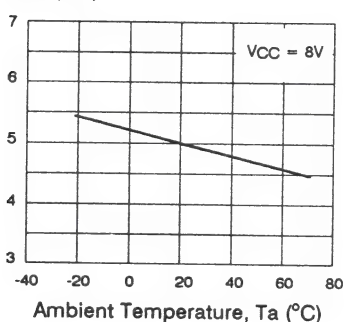
Total Harmonic Distortion, THD (%)



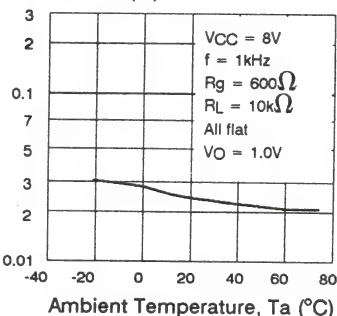
Response (dB)



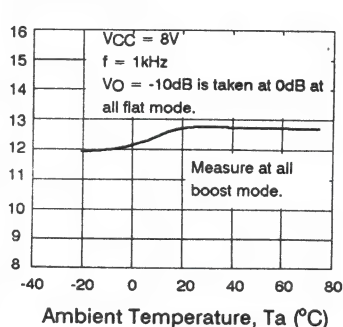
Quiescent Current, I_{CCQ} (mA)



Total Harmonic Distortion, THD (%)



Boost Amount



GL5529

SWITCHING TYPE DUAL PREAMPLIFIER AND LOW FRE QUENCY AMPLIFIER WITH ALC CIRCUIT

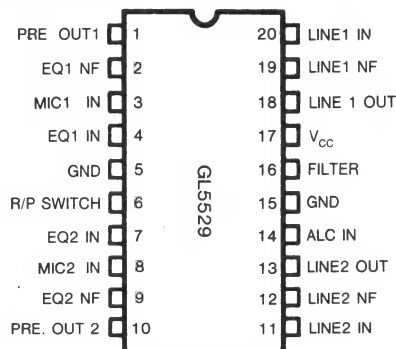
Function

- Amplification to set equalization for magnetic head
- Amplifying the signal from microphone
- Amplifying the signal from EQ, MIC and other amplifiers
- Automatic level control
- Switching the recording and playback mode
- Filtering pop noise

Features

- Including Preamplifiers with Electronic Switch for Switching Between the Recording and Playback Mode
- Built-in Line Amplifier with ALC Circuit
- Wide Range of Usable Power Supplies
- Fabricated in a 2-Channel Configuration

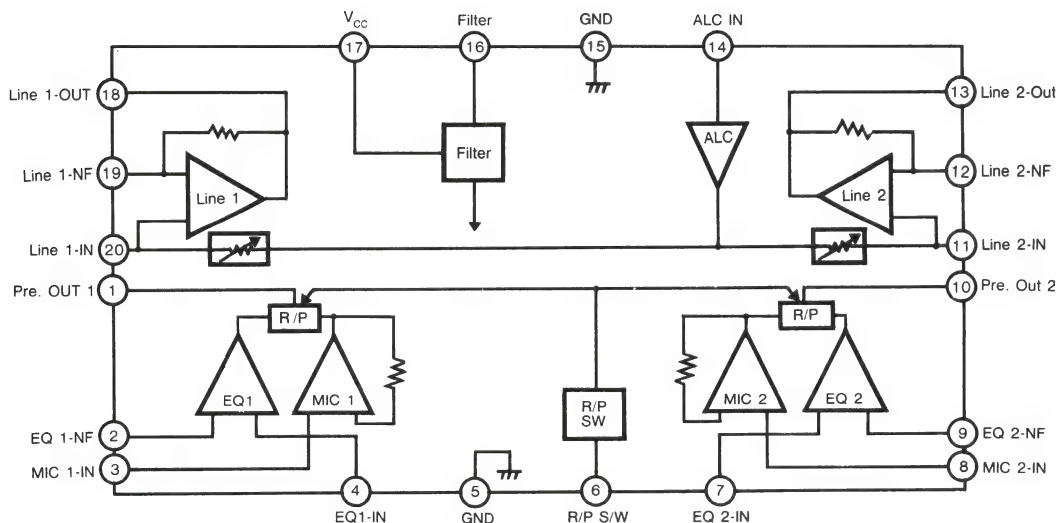
Pin Configuration



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage	V_{CC}	18	V
Circuit Current	I_{CC}	100	mA
Power Dissipation	P_D	1000	mW
Operating Temperature	T_{OPR}	-20°C to $+75^\circ\text{C}$	$^\circ\text{C}$
Storage Temperature	T_{STG}	-40°C to $+125^\circ\text{C}$	$^\circ\text{C}$

Block Diagram



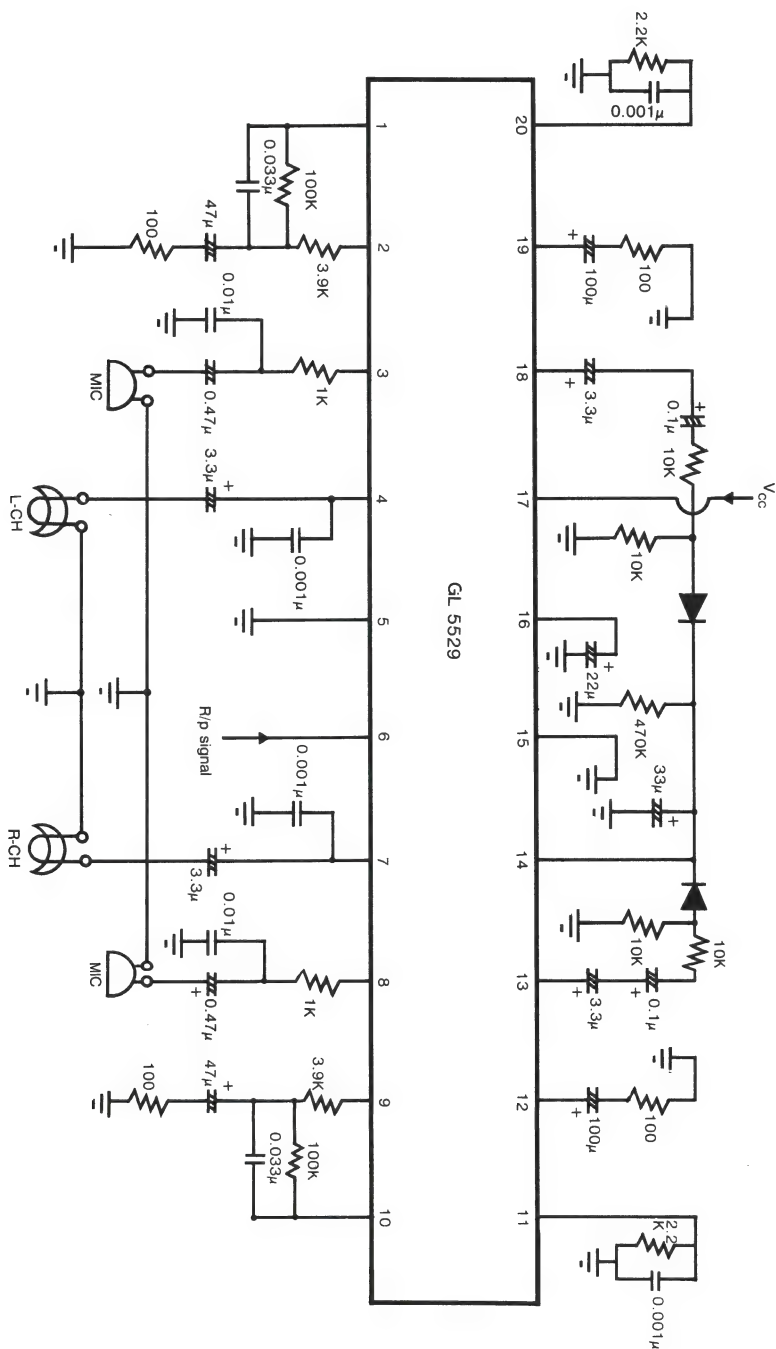
Electrical Characteristics: $T_A=25^{\circ}\text{C}$, $V_{CC}=9\text{V}$, $f=1\text{KHz}$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		3.5	9	12	V
Quiescent Current	I_{CCO}	Playback mode	5	10	15	mA
MIC-Amp Voltage Gain	G_{VM}	Amp. Output Voltage = 1 Vrms	23	24.5	26	dB
EQ-Amp Voltage Gain	G_{VP}	Amp. Output Voltage = 1 Vrms	35	38	41	dB
Line-Amp Voltage Gain	G_{VL}	Amp. Output Voltage = 1 Vrms	37	40	43	dB
MIC-Amp Maximum Output Voltage	V_{OM}	THD = 3%	1.5	2.5		Vrms
EQ-Amp Maximum Output Voltage	V_{OP}	THD = 3%	1.5	2.5		Vrms
Line-Amp Maximum Output Voltage	V_{OL}	THD = 3%	1.9	2.5		Vrms
MIC-Amp THD	THD_M	Amp. Output Voltage = 1 Vrms		0.2	0.5	%
EQ-Amp THD	THD_P	Amp. Output Voltage = 1 Vrms		0.2	0.5	%
Line-Amp THD	THD_L	Amp Output Voltage = 1 Vrms		0.2	0.5	%
MIC-Amp Input Impedance	Z_{IM}	$M_{1,2}$ Voltage When Input=10m Vrms	5	7.5	10	K Ω
EQ-Amp Input Impedance	Z_{IP}	$P_{1,2}$ Voltage When Input=10m Vrms	40	56	75	K Ω
Line-Amp Input Impedance	Z_{IL}	$L_{1,2}$ Voltage When Input=10m Vrms	20	33	45	K Ω
ALC range	ALC_A	From the point ALC is activated until output is 3 dB up	40	46		dB
ALC Distortion	ALC_{THD}	Distortion when input is 20dB up from the point ALC is activated			1.5	%
ALC Balance	ALC_B	The ALC output level difference in CH 1/CH 2 when input is 20dB up, from the point ALC is activated			3	dB
MIC-Amp Equivalent input Noise Voltage	N_{IM}	$R_g = 1\text{ K}\Omega$ 20~30 KHz BPF		1	2	μVrms
EQ-Amp Equivalent Input Noise Voltage	N_{IP}	$R_g = 1\text{ k}\Omega$ 20~30KHz BPF		1	2	μVrms
Line-Amp Equivalent Input Noise Voltage	N_{IL}	$R_g = 1\text{ K}\Omega$ 20~30 KHz BPF		1	3	μVrms

Pin Description

NO	NAME	Explanation	No.	Name	Explanation
1	Pre · Out 1	EQ/MIC output When input is play back mode Output Signal is EQ output When input is REC. mode Out put Signal is MIC output	10	Pre · Out 2	Same as Pin 1
2	EQ 1 – NF	EQ-Amp Negative feedback input	11	Line 2 – IN	Line-Amp input terminal to amplify the signal from the EQ, MIC and other amplifiers
3	MIC 1 – IN	MIC-Amp input terminal to amplify the Signal from a microphone.	12	Line 2 – NF	Line-Amp negative feedback input
4	EQ 1 – IN	EQ-Amp input terminal to amplify and to equalize the signal from the magnetic head.	13	Line 2 – Out	Line-Amp output
5	GND	Ground	14	ALC IN	ALC Input Pin
6	R/P switch	REC./Play switch control pin	15	GND	Ground
7	EQ 2 – IN	Same as Pin 4	16	Filter	Filtering POPNoise
8	MIC 2 – IN	Same as Pin 3	17	V _{CC}	Power Supply
9	EQ 2 – NF	Same as Pin 2	18	Line 1 – out	Same as 13
			19	Line 1 – NF	Same as 12
			20	Line 1 – IN	Same as 11

Application Circuit



GL5808

AM/FM TUNER

Description

The GL5808 is a monolithic IC designed for use in AM/FM receivers and radio cassettes. The IC incorporates for AM RF pre-amplifier with ALC, 'one-pin' oscillator, IF amplifier with AGC, demodulator and level detector for tuning indication. The FM circuitry comprises IF stages with limiter, quadrature detector and tuning indicator

Also, it has AM/FM switching function.

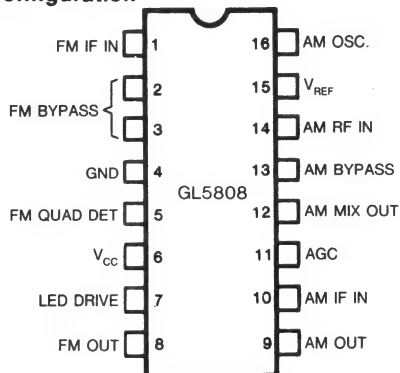
AM: RF preamplifier, Oscillator with ALC, Mixer IF Amplifier, Detector, AGC, Audio Preamplifier Tuning Indicator Driver.

FM: IF Amplifier, Limiter, Quadrature Detector. Tuning Indicator Driver, Audio Preamplifier

Features

- Extremely Low Number of External Components
- Low Noise: AM S/N 55dB
FM S/N 83dB
- Low Oscillator Voltage
Voltage at pin16: MW 130mV
SW 70mV ~ 90mV
(7MHz) (24MHz)
- Very Low Tweet
- Built-in Tuning Indicator Driver
- Simple DC Switching for AM-FM Sections
- Separated AM/FM Output Pins
- No Extra RF Prestage is Necessary
- Ceramic AM IF Filter is Used

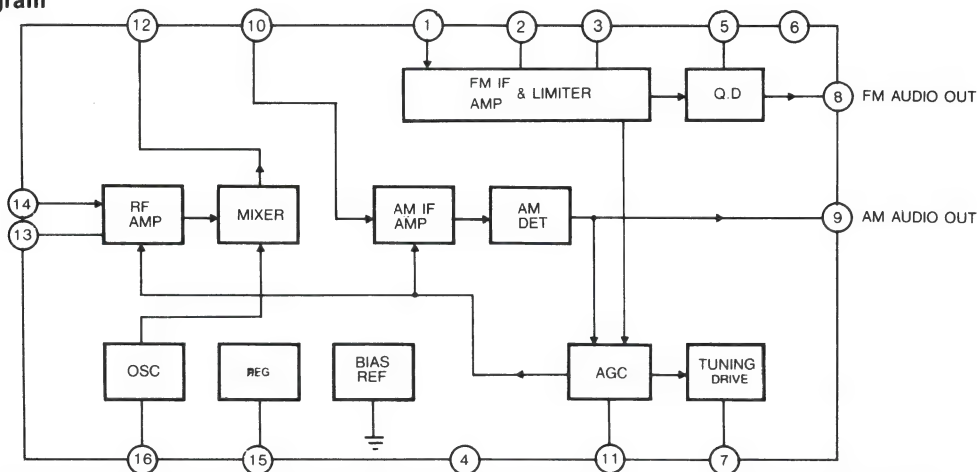
Pin Configuration



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage	V_{CC}	15V
Power Dissipation	P_D	450 mW
Operating Temperature	T_{OPR}	-20°C to $+70^\circ\text{C}$
Storage Temperature	T_{STG}	-40°C to $+250^\circ\text{C}$

Block Diagram



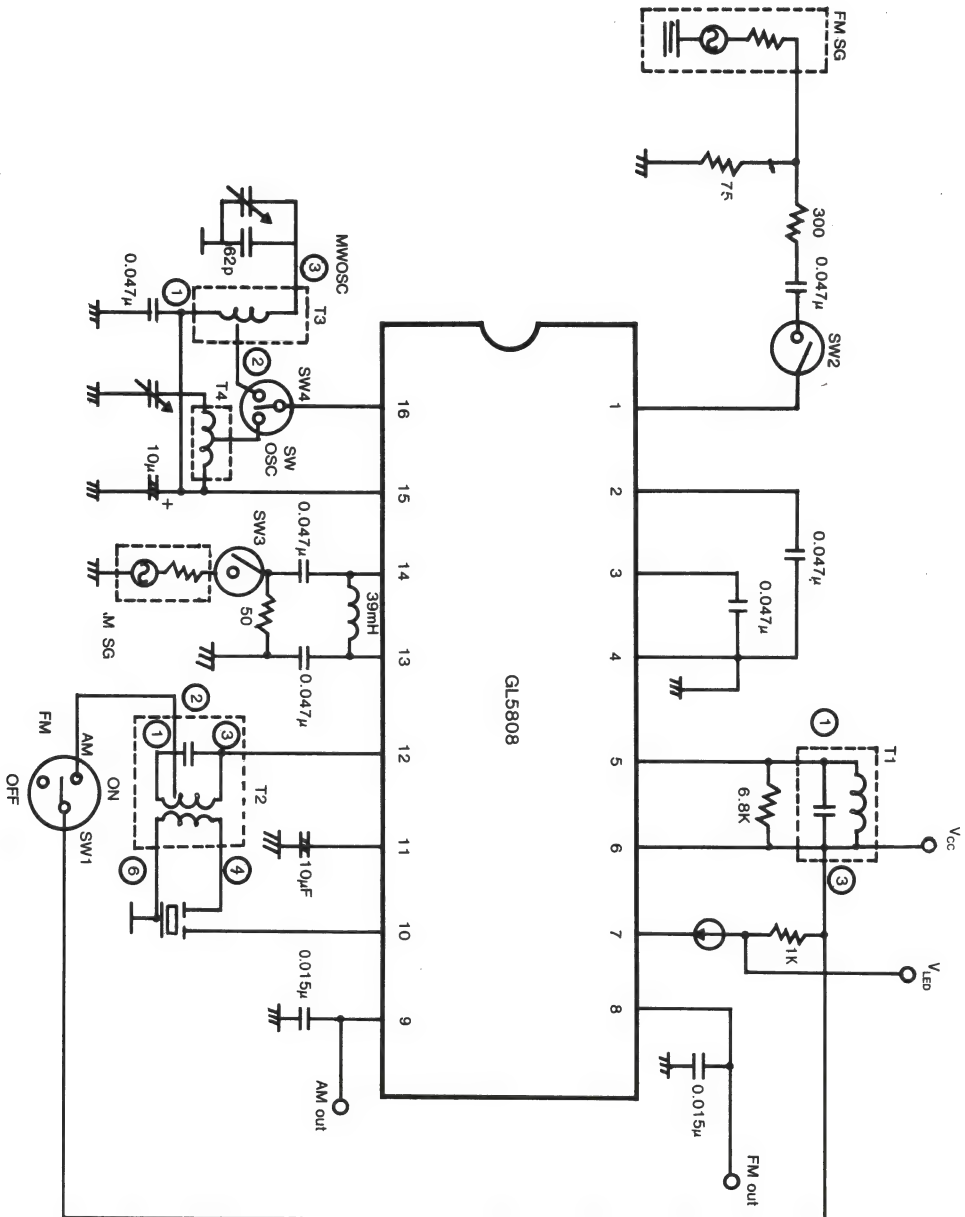
Electrical Characteristics: $T_A = 25^\circ\text{C}$, $V_{CC} = 4.5\text{V}$ (unless otherwise specified)

AM Section: $f = 1\text{MHz}$, $f_m = 400\text{Hz}$, 30% Mod.

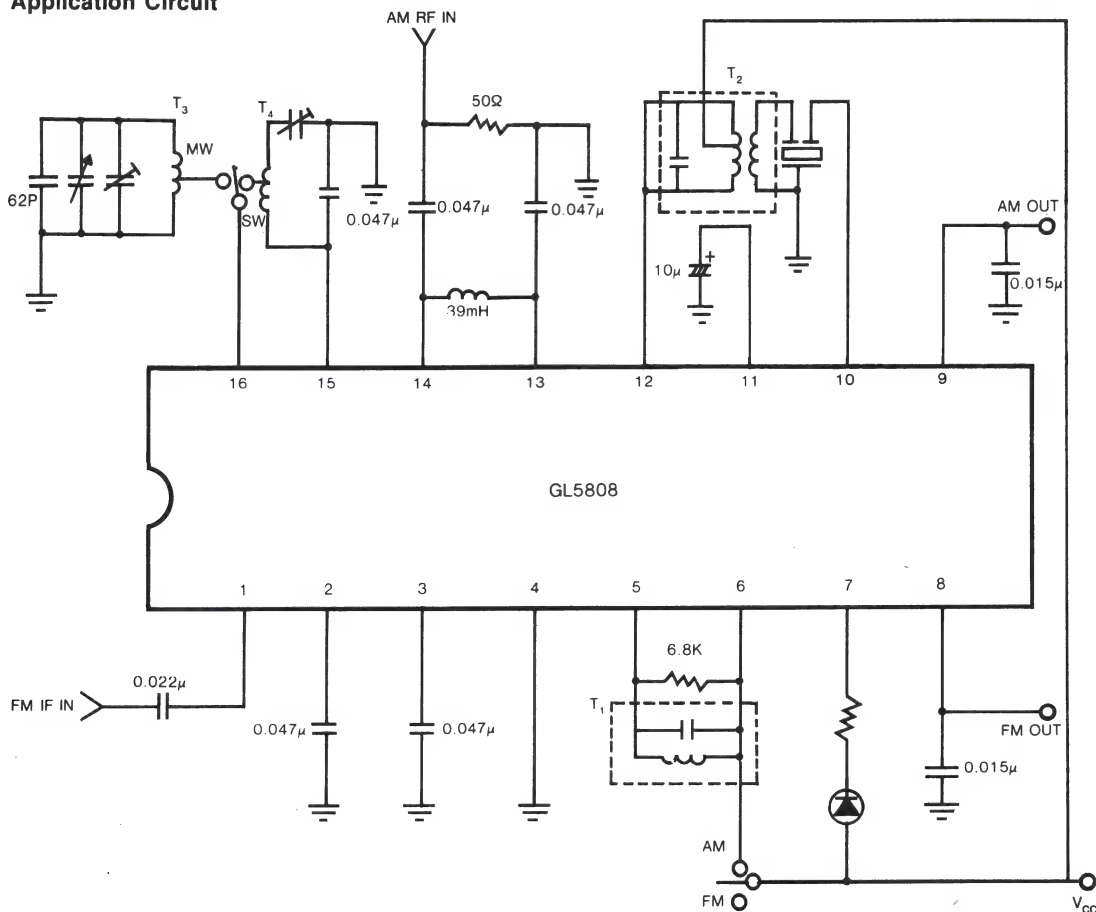
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Quiescent Current	I_{CC}			7.5	10.5	mA
Output Detection	V_{O1}	$V_{in} = 23\text{dB}\mu$	-33	-28	-23	dBm
Output Detection	V_{O2}	$V_{in} = 60\text{dB}\mu$	-19	-16	-13	dBm
Signal to Noise Ratio	S/N1	$V_{in} = 23\text{dB}\mu$	18	21.5		dB
Signal to Noise Ratio	S/N2	$V_{in} = 60\text{dB}\mu$	48	53		dB
Total Harmonic Distortion	THD1	$V_{in} = 60\text{dB}\mu$		0.45	1.3	%
Total Harmonic Distortion	THD2	$V_{in} = 100\text{dB}\mu$		1.5	3	%
Tuning Indication Voltage	V_{LED}	$I_{LED} = 1\text{mA}$	22	30	38	dBm
Oscillation Output Voltage	V_{OSC}	$f = 24\text{MHz}$	60	86	120	mV

FM Section: $f = 10.7\text{MHz}$, $\Delta f = \pm 75\text{KHz}$, $f_m = 400\text{Hz}$

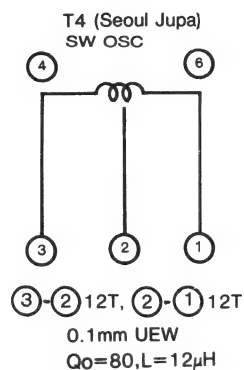
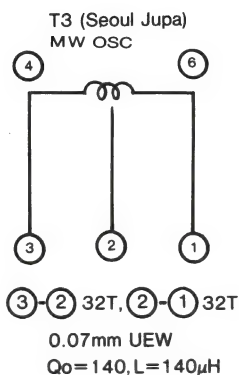
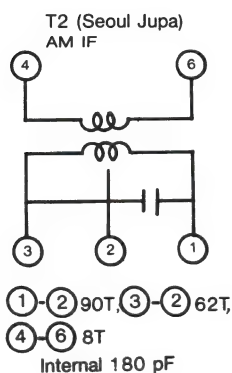
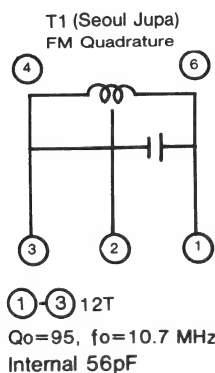
Quiescent Current	I_{CC}	CONDITIONS		8.5	12.0	mA
Output Detection	V_O	$V_{in} = 80\text{dB}\mu$	-12.5	-9.5	-6.5	dBm
Input Limiting Voltage	$V_{in(Lim)}$	-3dB point from V_O $V_{in} = 80\text{dB}\mu$		35	42	dB μ
Signal to Noise Ratio	S/N1	$V_{in} = 80\text{dB}\mu$	77	81		dB
Signal to Noise Ratio	S/N2	$V_{in} = 80\text{dB}\mu$, $\Delta f = 22.5\text{kHz}$		71		dB
Total Harmonic Distortion	THD1	$V_{in} = 80\text{dB}\mu$		0.55	1	%
Total Harmonic Distortion	THD2	$V_{in} = 80\text{dB}\mu$, $\Delta f = 22.5\text{kHz}$		0.05		%
Tuning Indication Voltage	V_{LED}	$I_{LED} = 1\text{mA}$		39	49	dB μ
AM Rejection Ratio	AMR	$V_{in} = 80\text{dB}\mu$ AM: $f_m = 1\text{KHz}$, 30%Mod		60		dB



Application Circuit



Coil Specification



	DATA SHEET INDEX	
	QUALITY ASSURANCE MANUAL	
1.	TV APPLICATION	
2.	VCR APPLICATION	
3.	AUDIO APPLICATION	
4.	TELECOM APPLICATION	
5.	REMOTE CONTROL APPLICATION	
6.	INDUSTRY APPLICATION	
	GOLDSTAR SEMICONDUCTOR SALES NETWORK	

GM16C450/82C50A

ASYNCHRONOUS COMMUNICATIONS ELEMENT

General Description

The GM16C450 is an improved specification version of the GM82C50A Asynchronous Communications Element (ACE). The improved specifications ensure compatibility with state-of-the-art CPUs. Functionally, the GM16C450 is equivalent to the GM82C50A.

The GM16C450 and GM82C50A each function as a serial data input/output interface in a microcomputer system. The functional configuration of the ACEs is programmed by the system software via a 3-state 8-bit bidirectional data bus; this includes the on-board baud rate generator.

The ACE performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the ACE, as well as any error conditions (parity, overrun, framing or break interrupt).

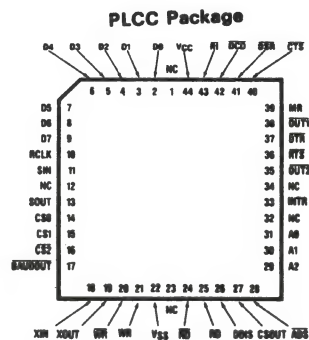
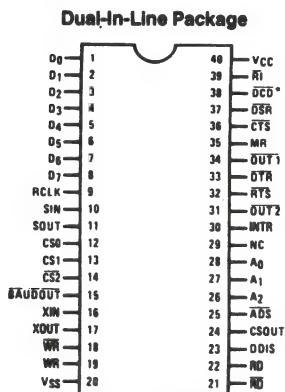
The ACE includes a programmable baud generator that is capable of dividing the timing reference clock input by a divisor between 1 and (2 to the power of 16 - 1), and producing a 16x clock for driving the internal transmitter logic. Provisions are also include to use this 16x clock to drive the receiver logic. Also included in the ACE is a complete modem control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

In addition, the GM16C450/GM82C50A runs at a maximum speed of 16 MHz.

Features

- Easily interfaces to most popular microprocessors
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from serial data stream
- Full double-buffering eliminates need for precise synchronization
- Independently controlled transmit, receive, line status and data set interrupts
- Programmable baud generator allows division of any input clock by 1 to (2 to the power of 16 - 1) and generates the internal 16x clock
- Independent receiver clock input
- Modem control functions (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial interface characteristics:
 - 5-, 6-, 7- or 8-bit characters
 - Even-, odd- or no-parity bit generation and detection
 - 1-, 1.5- or 2-stop bit generation
 - Baud generation (DC to 56k baud)
- False start bit detection
- Complete status reporting capabilities
- 3-state TTL drive capabilities for bidirectional
- Internal diagnostic capabilities:
 - Loopback controls for communications link fault isolation
 - Break, parity, overrun, framing error simulation
 - Fully prioritized interrupt system controls
- Compatible with PS/2 system speed data bus and control bus
- Line break generation and detection

Pin Configuration



*On the GM82 C50A, PIN38(PIN42 on the PLCC PACKAGE) is also called RLSD.

1.0 Absolute Maximum Ratings

Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	700 mW

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

2.0 DC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$, unless otherwise specified.

Symbol	Parameter	Conditions	GM16C450		GM82C50A		Units
			Min	Max	Min	Max	
V_{ILX}	Clock Input Low Voltage		−0.5	0.8	−0.5	0.8	V
V_{IHx}	Clock Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input Low Voltage		−0.5	0.8	−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6\text{ mA}$ on all (Note 2)		0.4		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -1.0\text{ mA}$ (Note 2)	2.4		2.4		V
$I_{CC(AV)}$	Avg. Power Supply Current (V_{CC})	$V_{CC} = 5.25\text{V}$, $T_A = 25^\circ\text{C}$ No Loads on output SIN, DSR, DCD, CTS, RI = 2.4V All other inputs = 0.4V Baud Rate Generator at 4 MHz Baud Rate at 50k		10		10	mA
I_{IL}	Input Leakage	$V_{CC} = 5.25\text{V}$, $V_{SS} = 0\text{V}$ All other pins floating.		± 10		± 10	μA
I_{CL}	Clock Leakage	$V_{IN} = 0\text{V}$, 5.25V		± 10		± 10	μA
I_{OZ}	TRI-STATE Leakage	$V_{CC} = 5.25\text{V}$, $V_{SS} = 0\text{V}$ $V_{OUT} = 0\text{V}$, 5.25V 1) Chip deselected 2) WRITE mode, chip selected		± 20		± 20	μA
V_{ILMR}	MR Schmitt V_{IL}			0.8		0.8	V
V_{IHMR}	MR Schmitt V_{IH}		2.0		2.0		V

Capacitance $T_A = 25^\circ\text{C}$, $V_{CC} = V_{SS} = 0\text{V}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{XIN}	Clock Input Capacitance	$f_c = 1\text{ MHz}$ Unmeasured pins returned to V_{SS}		15	20	pF
C_{XOUT}	Clock Output Capacitance			20	30	pF
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			10	20	pF

Note 1: Inputs on the CMOS parts are TTL compatible; outputs on the CMOS parts drive to GND and V_{CC} .

Note 2: Does not apply to XOUT.

3.0 AC Electrical Characteristics $T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = +5\text{V} \pm 5\%$

Symbol	Parameter	Conditions	GM 16C450		GM 82C50A		Units
			Min	Max	Min	Max	
t_{ADS}	Address Strobe Width		60		90		ns
t_{AH}	Address Hold Time		0		0		ns
t_{AR}	RD, \overline{RD} Delay from Address	(Note 1)	60		80		ns
t_{AS}	Address Setup Time		60		90		ns
t_{AW}	WR, \overline{WR} Delay from Address	(Note 1)	60		80		ns
t_{CH}	Chip Select Hold Time		0		0		ns
t_{CS}	Chip Select Setup Time		60		90		ns
t_{CSC}	Chip Select Output Delay from Select	@100 pF loading (Note 1)		100		125	ns
t_{CSR}	RD, \overline{RD} Delay from Chip Select	(Note 1)	50		80		ns
t_{CSW}	WR, \overline{WR} Delay from Select	(Note 1)	50		80		ns
t_{DH}	Data Hold Time		40		60		ns
t_{DS}	Data Setup Time		40		90		ns
t_{HZ}	RD, \overline{RD} to Floating Data Delay	@100 pF loading (Note 3)	0	100	0	100	ns
t_{MR}	Master Reset Pulse Width		5		10		μs
t_{RA}	Address Hold Time from RD, \overline{RD}	(Note 1)	20		20		ns
t_{RC}	Read Cycle Delay		175		500		ns
t_{RCS}	Chip Select Hold Time from RD, \overline{RD}	(Note 1)	20		20		ns
t_{RD}	RD, \overline{RD} Strobe Width		125		175		ns
t_{RDD}	RD, \overline{RD} to Driver Disable Delay	@100 pF loading (Note 3)		60		75	ns
t_{RVD}	Delay from RD, \overline{RD} to Data	@100 pF loading		125		175	ns
t_{WA}	Address Hold Time from WR, \overline{WR}	(Note 1)	20		20		ns
t_{WC}	Write Cycle Delay		200		500		ns
t_{WCS}	Chip Select Hold Time from WR, \overline{WR}	(Note 1)	20		20		ns
t_{WR}	WR, \overline{WR} Strobe Width		100		175		ns
t_{XH}	Duration of Clock High Pulse	External Clock (3.1 MHz Max.)	140		140		ns
t_{XL}	Duration of Clock Low Pulse	External Clock (3.1 MHz Max.)	140		140		ns
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$		360		755		ns
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$		360		755		ns
Baud Generator							
N	Baud Divisor		1	$2^{16} - 1$	1	$2^{16} - 1$	
t_{BHD}	Baud Output Positive Edge Delay	100 pF Load		125		250	ns
t_{BLD}	Baud Output Negative Edge Del. t_{Δ}	100 pF Load		125		250	ns
t_{HW}	Baud Output Up Time	$f_X = 3 \text{ MHz}, \div 3, 100 \text{ pF Load}$	330		330		ns
t_{LW}	Baud Output Down Time	$f_X = 2 \text{ MHz}, \div 2, 100 \text{ pF Load}$	425		425		ns
Receiver							
t_{RINT}	Delay from RD, \overline{RD} (RD RBR or RD LSR) to Reset Interrupt	100 pF Load		1		1	μs
t_{SCD}	Delay from RCLK to Sample Time			2		2	μs
t_{SINT}	Delay from Stop to Set Interrupt			1		1	RCLK Cycles (Note 2)

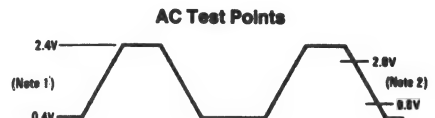
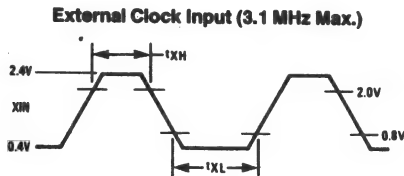
Note 1: Applicable only when \overline{ADS} is tied low. **Note 2:** RCLK is equal to t_{XH} and t_{XL} .

Note 3: Charge and discharge time is determined by V_{OL} , V_{OH} and the external loading.

3.0 AC Electrical Characteristics $T_A = 0^\circ\text{C to } +70^\circ\text{C}, V_{CC} = +5\text{V} \pm 5\%$ (Continued)

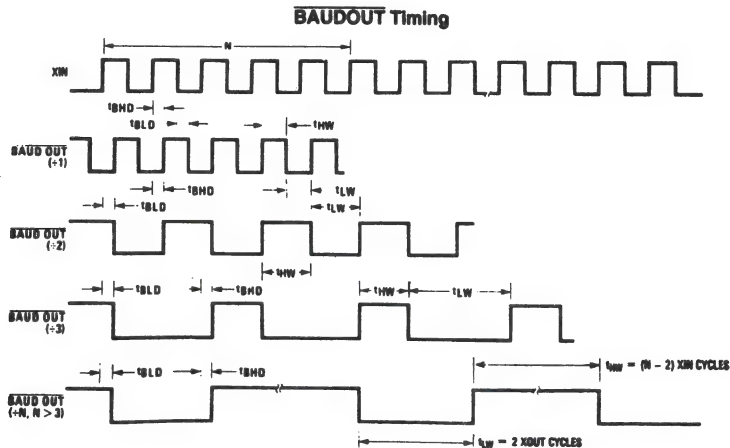
Symbol	Parameter	Conditions	GM16C450		GM82C50A		Units
			Min	Max	Min	Max	
Transmitter							
t _{HR}	Delay from WR, \overline{WR} (WR THR) to Reset Interrupt	100 pF Load		175		1000	ns
t _{IR}	Delay from RD, \overline{RD} (RD IIR) to Reset Interrupt (THRE)	100 pF Load		250		1000	ns
t _{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	8	24	BAUDOUT Cycles
t _{SI}	Delay from Initial Write to Interrupt		16	32	16	32	BAUDOUT Cycles
t _{STI}	Delay from Stop to Interrupt (THRE)		8	8	8	8	BAUDOUT Cycles
Modem Control							
t _{MDO}	Delay from WR, \overline{WR} (WR MCR) to Output	100 pF Load		200		1000	ns
t _{RIM}	Delay to Reset Interrupt from RD, \overline{RD} (RD MSR)	100 pF Load		250		1000	ns
t _{SIM}	Delay to Set Interrupt from MODEM Input	100 pF Load		250		1000	ns

4.0 Timing Waveforms (All timings are referenced to valid 0 and valid 1)



Note 1: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.

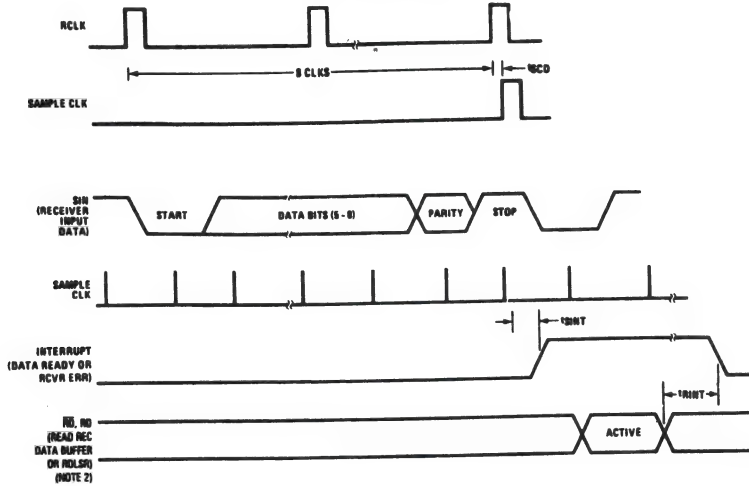
Note 2: The 2.0V and 0.8V levels are the voltages at which the timing tests are made.



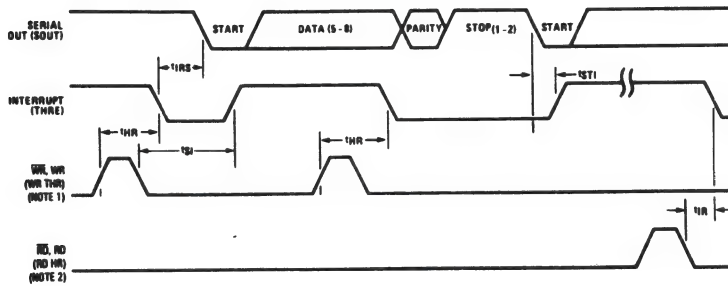


4.0 Timing Waveforms (Continued)

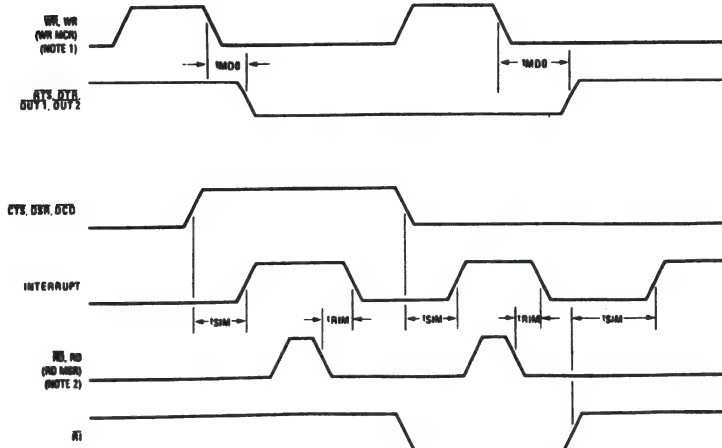
Receiver Timing



Transmitter Timing



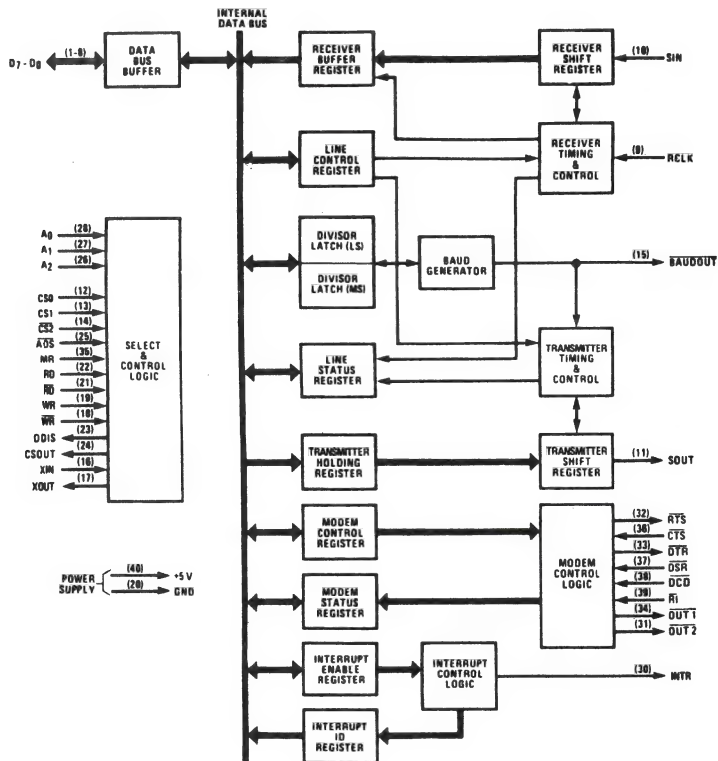
MODEM Controls Timing



Note 1: See Write Cycle Timing

Note 2: See Read Cycle Timing

5.0 Block Diagram



Note: Applicable pinout numbers are included within parenthesis.

6.0 Pin Descriptions

The following describes the function of all ACE pins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

6.1 INPUT SIGNALS

Chip Select (CS0, CS1, CS2), Pins 12–14: When CS0 and CS1 are high and CS2 is low, the chip is selected. This enables communication between the ACE and the CPU. The positive edge of an active Address Strobe signal latches the decoded chip select signals, completing chip selection. If ADS is always low, valid chip selects should stabilize according to the t_{CSW} parameter.

Read (RD, \overline{RD}), Pins 22 and 21: When RD is high or \overline{RD} is low while the chip is selected, the CPU can read status information or data from the selected ACE register.

Note: Only an active RD or \overline{RD} input is required to transfer data from the UART during a read operation. Therefore, tie either the RD input permanently low or the \overline{RD} input permanently high, when it is not used.

Write (WR, \overline{WR}), Pins 19 and 18: When WR is high or \overline{WR} is low while the chip is selected, the CPU can write control words or data into the selected ACE register.

Note: Only an active WR or \overline{WR} input is required to transfer data to the UART during a write operation. Therefore, tie either the WR input permanently low or the \overline{WR} input permanently high, when it is not used.

Address Strobe (ADS), Pin 25: The positive edge of an active Address Strobe (ADS) signal latches the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, CS2) signals.

Note: An active ADS input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the ADS input permanently low.

Register Select (A0, A1, A2), Pins 26–28: Address signals connected to these 3 inputs select a ACE register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain ACE registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

6.0 Pin Descriptions (Continued)

Register Addresses

DLAB	A ₂	A ₁	A ₀	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals (SOUT, INTR, OUT 1, OUT 2, RTS, DTR) are affected by an active MR input. (Refer to Table I.) This input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis.

Receiver Clock (RCLK), Pin 9: This input is the $16 \times$ baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send (CTS), Pin 36: When low, this indicates that the MODEM or data set is ready to exchange data. The CTS signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the CTS signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the CTS input has changed state since the previous reading of the MODEM Status Register. CTS has no effect on the Transmitter.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready (DSR), Pin 37: When low, this indicates that the MODEM or data set is ready to establish the communications link with the ACE. The DSR signal is a MODEM status input whose conditions can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the DSR signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the DSR input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Carrier Detect (DCD), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The DCD signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the DCD signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the DCD input has changed state

since the previous reading of the MODEM Status Register. DCD has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator (RI), Pin 39: When low, this indicates that a telephone ringing signal has been received by the MODEM or data set. The RI signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the RI signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the RI input signal has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status interrupt is enabled.

V_{CC}, Pin 40: +5V supply.

V_{SS}, Pin 20: Ground (0V) reference.

6.2 OUTPUT SIGNALS

Data Terminal Ready (DTR), Pin 33: When low, this informs the MODEM or data set that the UART is ready to establish a communications link. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

Request to Send (RTS), Pin 32: When low, this informs the MODEM or data set that the ACE is ready to exchange data. The RTS output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

Output 1 (OUT 1), Pin 34: This user-designated output can be set to an active low by programming bit 2 (OUT 1) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the X MOS parts this will achieve TTL levels.

Output 2 (OUT 2), Pin 31: This user-designated output can be set to an active low, by programming bit 3 (OUT 2) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state. In the X MOS parts this will achieve TTL levels.

Chip Select Out (CSOUT), Pin 24: When high, it indicates that the chip has been selected by active, CS0, CS1, and CS2 inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. CSOUT goes low when the UART is deselected.

Driver Disable (DDIS), Pin 23: This goes low whenever the CPU is reading data from the UART. It can disable or control the direction of a data bus transceiver between the CPU and the ACE (see Typical Interface for a High Capacity Data Bus).

Baud Out (BAUDOUT), Pin 15: This is the $16 \times$ clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAUDOUT may also be used for the receiver section by tying this output to the RCLK input of the chip.

6.0 Pin Descriptions (Continued)

Interrupt (INTR), Pin 30: This goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Line Status; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: This is the composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation or when the transmitter is idle.

6.3 INPUT/OUTPUT SIGNALS

Data (D₇–D₀) Bus, Pins 1–8: This bus is comprised of eight TRI-STATE input/output lines. The bus provides bidirectional communications between the ACE and the CPU. Data, control words, and status information are transferred via the D₇–D₀ Data Bus.

External Clock Input/Output (XIN, XOUT) Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the UART. When a crystal oscillator or a clock signal is provided, it drives the ACE via XIN (see typical oscillator network illustration).

7.0 Connection Diagrams

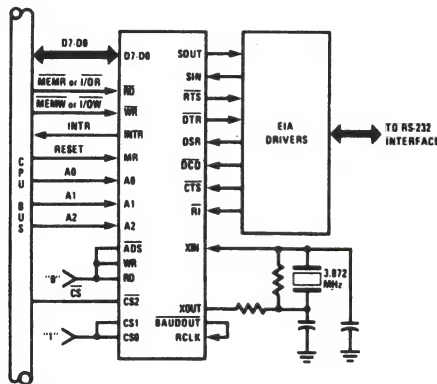


TABLE I. UART Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	0000 0000 (Note 1)
Interrupt Identification Register	Master Reset	0000 0001
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	0000 0000
Line Status Register	Master Reset	0 110 0000
MODEM Status Register	Master Reset	XXXX 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low
INTR (RCVR Data Ready)	Read RBR/MR	Low
INTR (THRE)	Read IIR/Write THR/MR	Low
INTR (Modem Status Changes)	Read MSR/MR	Low
OUT 2	Master Reset	High
RTS	Master Reset	High
DTR	Master Reset	High
OUT 1	Master Reset	High

Note 1: Boldface bits are permanently low.

Note 2: Bits 7–4 are driven by the input signals.

GM16C451

PARALLEL/ASYNCHRONOUS COMMUNICATIONS ELEMENT

DESCRIPTION

The GM16C451 is an universal asynchronous receiver and transmitter with a bidirectional CENTRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56kHz. The GM16C451 fabricated in an advanced 2 μ CMOS process to achieve low power drain and high speed requirements.

The GM16C451 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The GM16C451 also provides the user with a fully bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on board status of the transfer operations being performed. The GM16C451 also has complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The GM16C451 can interface easily to the most popular microprocessors and communications link faults can be detected with internal loopback capability.

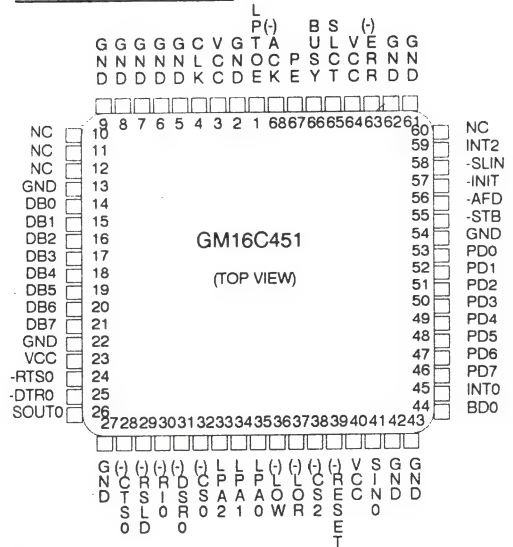
FEATURES

- Pin-to-pin and functionally compatible to VL16C451
- Bidirectional printer port
- Modem control signals (CTS-, RTS-, DSR-, DTR-, RI-, CD-,)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Direct replacement of logic for PC/XT/AT
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Fully compatible with all new bidirectional PS/2 printer port
- High data transfer rate

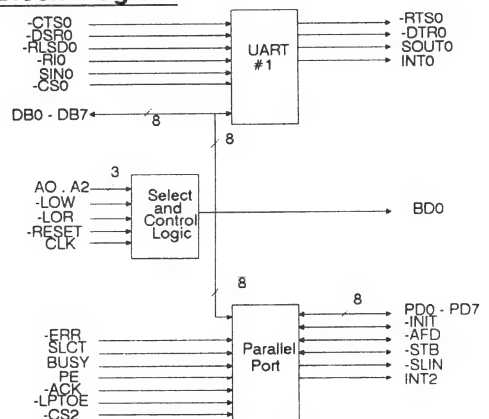
Absolute Maximum Ratings

Ambient Operating Temperature	-10°C ~ + 70°C
Strobe temperature	-65°C + 150°C
Supply Voltage to GND Potential	-0.5V ~ V _{cc} + 0.3V
Applied Output Voltage	-0.5V ~ V _{cc} + 0.3V
Applied Input Voltage	-0.5V ~ 7.0V
Power Dissipation	500mW

Pin Configuration



Block Diagram



SIGNAL DESCRIPTION

Signal Name	Pin No.	Signal Description
IOR	37	Input/Output Read Strobe: This is an active low input which causes the serial channel to output data to the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0,A1,A2. Chip select 0 (-CS0) selects UART and chip select 2 (-CS2) selects the line printer port.
IOW	36	Input/Output Write Strobe: This is an active low input which causes data from the data bus (DB0-DB7) to be input to UART or to the parallel port. The data input depends upon the register selected by the address inputs A0,A1,A2. The chip select inputs (-CS0 and -CS2) enable the UART and the parallel port(respectively).
DB0-DB7	14-12	Data Bits DB0-DB7: The Data Bus provides eight, three state I/O lines for the transfer of data, control and status information between the GM16C451 and the CPU. These lines are normally in a high impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0,A1,A2	35,34,33	Address Lines A0-A2: The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels. Table 11 for the decode of the parallel line printer port.
CLK	4	Clock input: The external clock input to the UART baud rate divisor.
SOUT0	26	Serial Data Output: This line is the serial data outputs from the UART's transmitter circuitry. A mark(1) is a logic "one" (high) and space (0) is a logic "zero"(low). SOUT0 is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
-CTS0	28	Clear to Send Inputs: The logical state of the -CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR(4)] of the UART. A change of state of the -CTS pin, since the previous reading of the MSR causes the setting of DCTS [MSR(0)] to each Modem Status Register. When a -CTS pin is low, the modem is indicating that data on SOUT0 can be transmitted.
DSR0	31	Data Set Ready Inputs: The logical state of the DSR0 pin is reflected in MSR(5) of the Modem Status Register. DDSR[MSR(1)] indicates whether the DSR0 pin has changed state since the previous reading of the MSR. When a DSR0 pin is low, the modem is indicating that it is ready to exchange data with the UART.
DTR0	25	Data Terminal Ready Output: The DTR0 pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of the UART. This signal is cleared (high) by writing a logic 0 to the DTR bit[MCR(0)] or whenever a reset occurs. When active (low), the DTR0 pin indicates to the DCE the UART is ready to receive data.
-RTS0	24	Requests to Send Output: The -RTS0 signal is an output on the UART used to enable the modem. The -RTS0 pin is set low by writing a logic 1 to MCR(1) bit 1 of the UART's Modem Control Register. The -RTS0 pin is reset high by Reset. A low on the -RTS0 indicates to the DCE that the UART has data ready to transmit. In half duplex operations, -RTS0 is used to control the direction of the line.
-R10	30	Ring Indicator Input: When low, -R10 indicates that a telephone ringing signal has been received by the modem or data set. The -R10 signal is a modem control input whose condition is tested by reading MSR(6) (RI) of the UART. The Modem Status Register output TER1[MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER(3) = 1] and -R10 changes from a high to low, an interrupt is generated.

SIGNAL DESCRIPTION(Cont'd)

Signal Name	Pin No.	Signal Description
-LPTOE	1	Parallel Data Output Enable: When low, this signal enables the Write Data Register to the PD0-PD7 lines, putting the PD0-PD7 lines in the high-impedance state. A high allows them to be used as inputs. -LPTOE is usually tied low for line printer operation.
SINO	41	Serial Data Input: The serial data inputs moves information from the communication line or modem to the GM16C451 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
-RLSD0	29	Receive Line Signal Detect: When low, -RLSD output indicates that the data carrier has been detected by the modem or data set. -RLSD is modem input whose condition can be tested by the CPU by reading MSR(7)(RLSD) of the Modem Status Registers. MSR(3)(DRLSD) of the Modem Status Registers indicates whether the -RLSD input has changed since the previous reading of the MSR. -RLSD has no effect on the receiver. If the -RLSD changes state with the modem status interrupt enabled, an interrupt occurs.
-RESET	39	Reset: When low, the reset input forces the GM16C451 into an idle mode in which all serial data activities are suspended. The Modem Control Register(mcr) along with its outputs is cleared. The Line Status Register(LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
INT0	45	Serial Channel Interrupt Output: This three-state output is enabled by the MCR bit 2. The serial channel interrupt goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of the serial channel: Receiver Error flag. Received Data Available. Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset operation.
-CS0, -CS2	32,38	Chip Selects: Each Chip Select input acts as an enable for the write and read signals for its channel. -CS0 enables the serial port, while -CS0 enables the signals to the line printer port.
BD0	44	Bus Buffer Output: The active high output is asserted when this serial channel or the parallel port is read. This output can be used to control the system bus driver device (74LS245)
PD0- PD7	53-46	Parallel Data Bits(0-7): These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when -LPTOE is held in the high state.
-STB	55	Line Printer Strobe: This open-drain line provides communication between the GM16C451 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
-AFD	56	Line Printer Autofeed: This open-drain line provides the line printer with an active low signal when continuous from paper is to be autofeed to the printer.
-INIT	57	Line Printer Initialize: This open-drain line provides the line printer with a signal that allows the line printer initialization routine to be started.

SIGNAL DESCRIPTION(Cont'd)

Signal Name	Pin No.	Signal Description
-SLIN	58	Line Printer Select: This open-drain line selects the printer when it is active low.
INT2	59	Printer Port Interrupt: This signal is an active high, three-state output, generated by the positive transition of ACK. It is enabled by bit 4 of the Write Control Register.
-ERR OR	63	Line Printer Error: This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition.
SLCT	65	Line Printer Selected: This is an input line from the line printer that goes high when the line printer has been selected.
BUSY	66	Line Printer Busy: This is an input line from the line printer that goes high when the line printer is not ready to accept data.
PE	67	Line Printer Paper Empty: This is an input line from the line printer that goes high when the printer runs out of paper.
-ACK	68	Line Printer Acknowledge: This input goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.
VCC	3,23,40 64	Power Supply: The power supply requirement is $5V \pm 5\%$
GND	2,5-9, 13,22,27 42,43,54 61,61	Ground (0 V): All pins must be tied to ground for proper operation.

FUNCTIONAL DESCRIPTION

Serial Channel Register

Three types of internal registers are used in the serial channel of the GM16C451. They are used in the operations of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modem Control Registers, while the status registers are the Line Status Registers and the Modem Status Register. The Data Registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. BIT 0 of a data word is always the first serial data bit received and transmitted. The GM16C451 data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion. The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of

the line characteristics in system memory. The contents of the LCR are described below.

- LCR(0) Word Length Select Bit 0 (WLS0)
- LCR(1) Word Length Select Bit 1 (WLS1)
- LCR(2) Stop Bit Select (STB)
- LSR(3) Parity Enable (PEN)
- LCR(4) Even Parity Select (EPS)
- LCR(5) Stick Parity
- LCR(6) Set Break
- LCR(7) Divisor Latch Access Bit (DLAB)

LCR(0) and LCR(1) word length select Bit 1 : The number of bits in each serial character is programmed as shown in the following chart:

LCR(1)	LCR(0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8 bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When Parity is enable [LCR(3) = 1]; LCR(4) = 0 selects odd parity, And LCR(4) = 1 selects even parity.

LCR(5) Stick Parity: When parity is enable [LCR(3)-1], CLR(5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR(4).

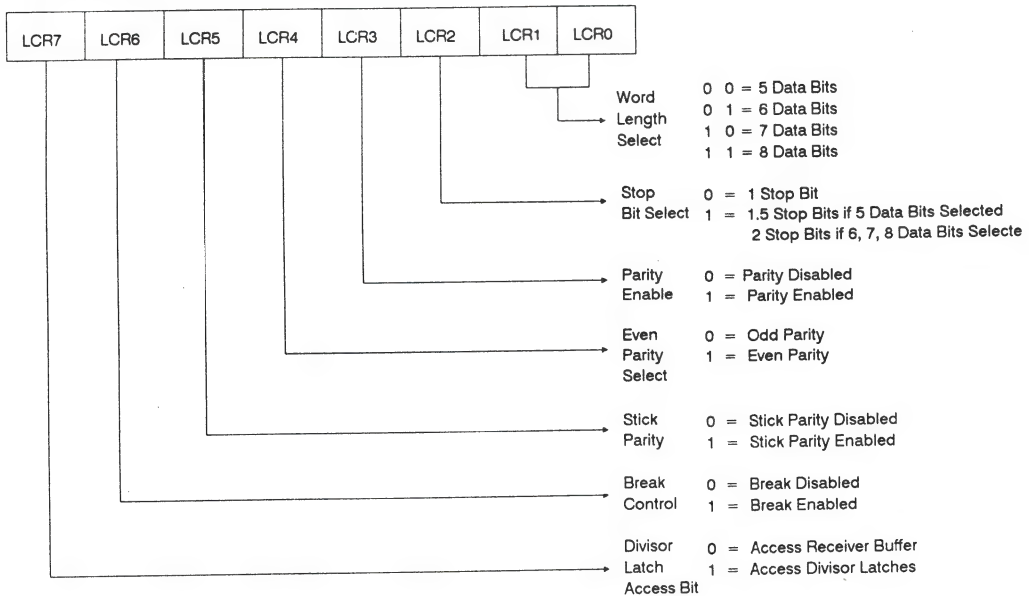
TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care", 0 = Logic Low, 1 = Logic High

Note: The serial channel is accessed when -CS0 is low.

FIGURE 1. LINE CONTROL REGISTER



This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1), and clear break when normal transmission has to be restored.

LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel of the GM16C451.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break

TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	Logic 1	Logic 0
LSR(0) Data Ready(DR)	Ready	Not Ready
LSR(1) Overrun Error(OE)	Error	No Error
LSR(2) Parity Error(PE)	Error	No error
LSR(3) Framing Error(FE)	Error	No Error
LSR(4) Break Interrupt(BI)	Break	No Break
LSR(5) Transmitter Holding Register Empty(THRE)	Empty	Not Empty
LSR(6) Transmitter Empty(TEMY)	Empty	Not Empty
LSR(7) Not Used		

reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU

character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER(1)], an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR(1) - LSR(4). (OE, PE, FE, and BI). The contents of the Line Status Register shown in Table 2 are described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LSR(4)). The PE bit is set high upon detection of a parity error, and is

reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start Bit + Data Bits + Parity + Stop Bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2) = 1 in the Interrupt Enable Register.

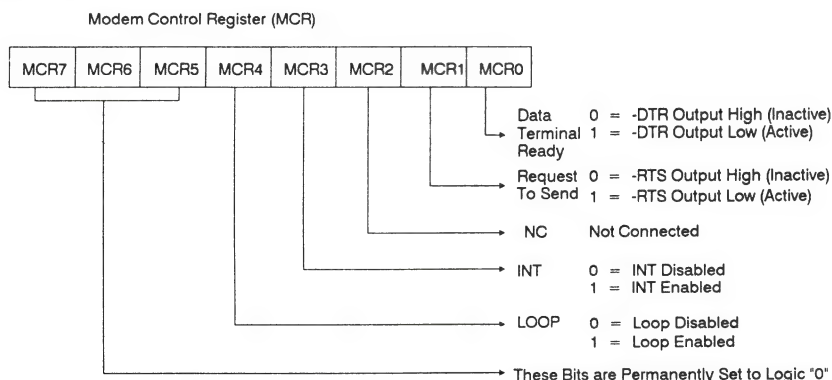
LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the GM16C450 is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enable (IER(1) = 1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the

TABLE 3. MODEM CONTROL REGISTER BITS

MCR BITS	LOGIC 1	LOGIC 0
MCR(0) Data terminal Ready(DCR)	-DTR Output Low	-DTR Output High
MCR(1) Request to Send(RTS)	-RTS Output Low	-Rts Output High
MCR(2) 0		
MCR(3) Interrupt(INT) Enable	INT Enabled	INT Disabled
MCR(4) Loop	Loop Enabled	Loop Disabled
MCR(5) 0		
MCR(6) 0		
MCR(7) 0		

FIGURE 2. MODEM CONTROL REGISTER

Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEND is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3. The MCR can be written and read. The -RTS and -DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0,1,3 and 4 are shown below:

MCR(0): When MCR(0) is set high, the -DTR output is forced low. When MCR(0) is reset low, the -DTR output is forced high. The -DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the RTS output is forced low. When MCR(1) is reset low, the -RTS output is forced high. The -RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(3): When MCR(3) is set high, the INT output is enabled.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the

channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs (-CTS, -DSR, and -RI) are disconnected. The modem control outputs (-DTR and -RTS) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

In the Diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR(5) -MCR(7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the GM16C451. In addition to the current status information, four bits of the MSR indicate whether

TABLE 4. MODEM STATUS REGISTER BITS

MSR BITS	Mnemonic	Description
MSR(0)	DCTS	Delta Clear to Send
MSR(1)	DDSR	Delta Data Set Ready
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(3)	DRLSD	Delta Data Carrier Detect
MSR(4)	-CTS	Clear to Send
MSR(5)	-DSR	Data Set Ready
MSR(6)	-RI	Ring Indicator
MSR(7)	-RLSD	Receiver Line Signal Detect

the modem inputs have changed since the last reading of the MSR. The Delta Status Bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are -CTS, -DSR, -RI and -RLSD. MSR(4) -MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the -CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the -DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the -RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on -RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the -RLSD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the -CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in loop mode [MCR(4) = 1], MSR(4) is equivalent to -RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the -DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR(4) = 1], MSR(5) is equivalent to DTR in the MCR.

MSR(6) Ring Indicator: Indicates the status of the RI input (pin 39). If the channel is in the loop mode

[MCR(4) = 1], MSR(6) is not connected in the MCR.

MSR(7) Receive Line Signal Detect: Receive Line Signal Detect indicates the status of the Receive Line Signal Detect (-RLSD) input. If the channel is in the loop mode [MCR(4) = 1], MSR(4) is equivalent to Out2 of the MCR.

The modem status inputs (-RI, -RLSD, -DSR, and -CTS) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mark control signals. If a DCTS, DDSR, TERI, or DRLSD are true and a state change occurs during a read operation (-DISTR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read -DISTR operations. If a status condition is generated during a read -DISTR operation, the status bit is not set until the trailing edge of the read -DISTR.

If a status bit is set during a read -DISTR operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read -DISTR instead of being set again.

Each GM16C451

serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2 to the power of 16 (see also BRG description). The output frequency of the Baud Generator is $16 \times \text{the data rate}$ [DIVISOR # = Clock / (Baud Rate x 16)]. Two 8 bit divisor latch registers store the divisor in a 16 bit binary format. These Divisor Latch Register must be loaded during initialization. Upon loading either of the Divisor Latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in each serial channel of the GM16C451 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bit are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the

Receiver Shift Register by the 16x clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character results in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 Thru 7:

RBR(0)	DATA BIT 0
RBR(1)	DATA BIT 1
RBR(2)	DATA BIT 2
RBR(3)	DATA BIT 3
RBR(4)	DATA BIT 4
RBR(5)	DATA BIT 5
RBR(6)	DATA BIT 6
RBR(7)	DATA BIT 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused

bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflects the status of the THR. The TEMPTY flag [LSR(5)] indicates if both the THR and TSR are empty.

THR Bits thru 7

THR(0)	DATA BIT 0
THR(1)	DATA BIT 1
THR(2)	DATA BIT 2
THR(3)	DATA BIT 3
THR(4)	DATA BIT 4
THR(5)	DATA BIT 5
THR(6)	DATA BIT 6
THR(7)	DATA BIT 7

Scratchpad Register is an 8 bit Read/Write register that has no effect on any channel in the GM16C451. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR(0)	DATA BIT 0
SCR(1)	DATA BIT 1
SCR(2)	DATA BIT 2
SCR(3)	DATA BIT 3
SCR(4)	DATA BIT 4
SCR(5)	DATA BIT 5
SCR(6)	DATA BIT 6
SCR(7)	DATA BIT 7

TABLE 5. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
Bit2	Bit 1	Bit 0	Priority level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the interrupt Source or THR Write
0	0	0	Fourth	Modem Status	-CTS, -DSR, -RI, -RSLD	MSR Read

x = Not Defined

FIGURE 3. INTERRUPT CONTROL LOGIC

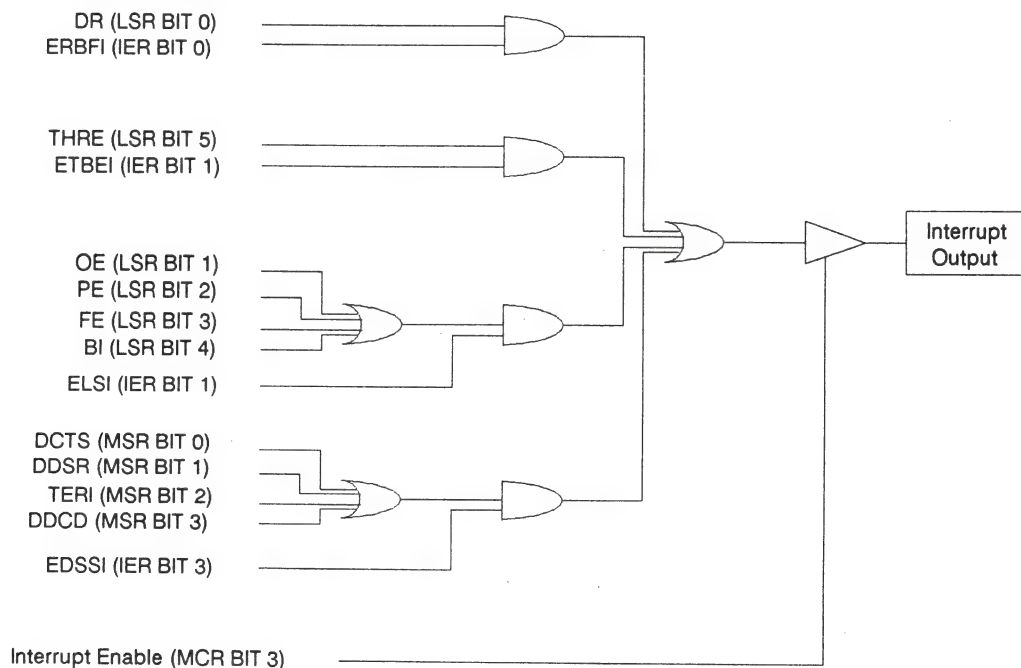


TABLE 6. SERIAL CHANNEL ACCESSIBLE REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit(1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(O/e) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

LSB Data Bit 0 is the first bit transmitted or received.

INTERRUPTS

The Interrupt Identification Register (IIR) in the serial channel of the GM16C451 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, The IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in the Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR(0): IIR(0) can be used in either as hard wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write Register used to independently enable the four serial channel interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in

their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 3 and are described below.

IER(0): When programmed high [IER(0) = LOGIC 1], IER(0) enables Received Data Available Interrupt.

IER(1): When programmed high [IER(1) = LOGIC 1], IER(1) enables the Transmitter Holding Register Empty Interrupt.

IER(2): When programmed high [IER(2) = LOGIC 1] IER(2) enables Receiver Line Status Interrupt.

IER(3): When programmed high [IER(3) = LOGIC 1], IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

TRANSMITTER

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5- to -8 bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, both THRE and TEMT are high. The first word write causes THRE to be reset to 0. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

RECEIVER

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16x clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0),LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status information for the receiver is provided in the Line Status Register to the Receiver Buffer Register, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR(2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3)

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is symmetrical square wave, the center of the data cells will occur within $\pm 3.125\%$ of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16x clock cycle prior to being detected.

BAUD RATE GENERATOR (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers registers DLL and DLM and the external frequency. The bit rate is selected by programming the

two Divisor Latches, Divisor Latch Most Significant Byte and Division Latch Least Significant Byte. Setting DLL = 1 and DLM = 0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432MHz, 2.4576MHz, 3.072MHz. With these frequencies, standard bit rates from 50 to 38.5kbps are available. Tables 7,8,9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

RESET

After power up, the GM16C451 -Reset input (MR) should be held low for 500ns to reset the GM16C451 circuits to an idle mode until initialization. A low on -Reset causes the following

1. Initializes the transmitter and receiver internal clock counters.
2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of The reset condition (Reset high), The GM16C451 remains in the idle mode until programmed.

A hardware reset of the GM16C451 sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the GM16C451 is given in Table 10.

PROGRAMMING

Each serial channel of the GM16C451 is programmed by the control registers LCR, IER, DLL and DLM, MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface. While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the GM16C451 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

CLOCK INPUT OPERATION

The maximum input frequency of the external clock of the GM16C451 is 3.1MHz

TABLE 7. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 8. BAUD RATES (2.4576 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

TABLE 9. BAUD RATES (3.072 MHz CLOCK)

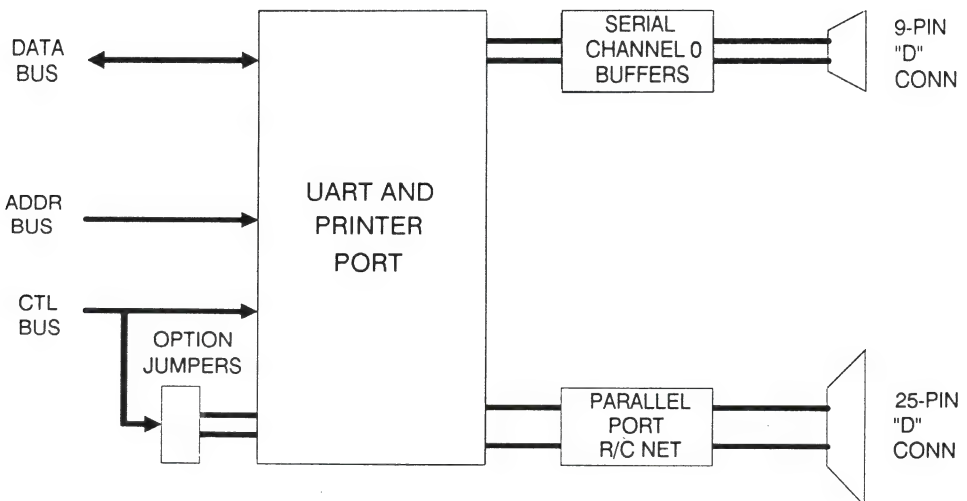
Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

TABLE 10. RESET

Register/Signal	Reset Control	Reset
INTERRUPT ENABLE REGISTER	RESET	ALL BITS LOW (0-3 FORCED AND 4-7 PERMANENT)
INTERRUPT IDENTIFICATION REGISTER	RESET	BIT 0 IS HIGH, BITS 1 AND 2 LOW BITS 3-7 ARE PERMANENTLY LOW
LINE CONTROL REGISTER	RESET	ALL BITS LOW
MODEM CONTROL REGISTER	RESET	ALL BITS LOW
LINE STATUS REGISTER	RESET	ALL BITS LOW, EXCEPT BITS 5 AND 6 HIGH
MODEM STATUS REGISTER	RESET	BITS 0-3 LOW BITS 4-7 INPUT SIGNAL
SOUT	RESET	HIGH
INTRPT(RCVR ERRS)	READ LSR/RESET	LOW
INTRPT(RCVR Data Ready)	READ RBR/RESET	LOW
INTRPT(THRE)	READ IIR/WRITE THR/RESET	LOW
INTRPT(MODEM STATUS CHANGES)	READ MSR/RESET	LOW
-OUT2	RESET	HIGH
-RTS	RESET	HIGH
-DTR	RESET	HIGH
-OUT1	RESET	HIGH

DEVICE APPLICATION

GM16C451



FUNCTIONAL DESCRIPTION

PARALLEL PORT REGISTERS

The GM16C451's parallel port interfaces the device to a Centronics style printer. When Chip Select 2 (-CS2) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (-IOR) and write (-IOW) pin as shown. The Read Data Register allows the microprocessor to read the information on the parallel bus. The Read Status Register allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (-BUSY), Acknowledge (-ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (-ERR)R). The Read Control Register allows the state of the control lines to be read. The Write Control Register sets the state of the control lines. They are Interrupt Enable (IRQ ENB), Select In (SLIN), Initialize the Printer (-INIT), Autofeed the Paper (AUTOFD), Strobe (STROBE), which informs the printer of the presence of a valid byte on the parallel bus. The Write Data Register allows the microprocessor to write a byte to the parallel bus.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

TABLE 11. PARALLEL PORT REGISTERS

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Port	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	PD 0
Read Status	-BUSY	-ACK	PE	SLCT	-ERROR	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	-INIT	AUTOFD	STROBE
Write Data	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	PD 0
Write Control	1	1	1	IRQ ENB	SLIN	-INIT	AUTOFD	STROBE

TABLE 12. PARALLEL PORT REGISTER SELECT

Control Pins					Register Selected
-IOR	-IOW	-CS2	A1	A0	
0	1	0	0	0	Read Data
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5V ± 5% (Note 1,5)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
tDIW	-DISTR STROBE WIDTH	125		ns	
RC	READ CYCLE	360		ns	
tDDD	DELAY FROM -DISTR TO DATA		125	ns	100pF LOAD
tHz	-DISTR TO FLOATING DATA WIDTH	0	100	ns	100pF LOAD, NOTE 4
tDOW	-DOSTR STROBE WIDTH	100		ns	
WC	WRITE CYCLE	360		ns	
tDS	DATA SETUP TIME	40		ns	
tDH	DATA HOLD TIME	40		ns	
tRA	ADDRESS HOLD TIME FROM -DISTR	20		ns	NOTE2
tRCS	CHIP SELECT HOLD TIME FROM DISTR	20		ns	NOTE2
tAR	-DISTR DELAY FROM ADDRESS	60		ns	NOTE2
tCSR	-DISTR DELAY FROM CHIP SELECT	50		ns	NOTE2
tWA	ADDRESS HOLD TIME FROM -DOSTR	20		ns	NOTE2
tWCS	CHIP SELECT HOLD TIME FROM -DOSTR	20		ns	NOTE2
tAW	-DOSTR DELAY FROM ADDRESS	60		ns	NOTE2
tCSW	-DOSTR DELAY FROM SELECT	50		ns	NOTE2
tRW	RESET PULSE WIDTH	5		μs	
tXH	DURATION OF CLOCK HIGH PULSE	140		ns	EXTERNAL CLOCK
tXL	DURATION OF CLOCK LOW PULSE	140		ns	EXTERNAL CLOCK

- NOTES : 1. RCLK IS INTERNALLY DERIVED FROM THE INTERNAL- BAUDOUT SIGNAL.
 2. THE INTERNAL ADDRESS STROBE IS ALWAYS ACTIVE.
 3. RCLK = tXH AND tXL.
 4. CHARGE AND DISCHARGE TIME IS DETERMINED BY VOL, VOH AND THE EXTERNAL LOADING.
 5. ALL TIMING ARE REFERENCED TO VAILD 0 AND 1. (SEE AC TEST POINTS.)

AC CHARACTERISTICS (Cont.) TA = 0°C TO 70°C, VCC = 5V + 5% (Note 1, 5)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
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Transmitter

t _{HR1}	DELAY FROM RISING EDGE OF DOSTR (WR THR) TO RESET INTERRUPT		175	ns	100pF LOAD
t _{IRS}	DELAY FROM INITIAL INTR RESET TO TRANSMIT START	8	24	CLK CYCLES	NOTE2
t _{SI}	DELAY FROM INITIAL WRITE TO INTERRUPT	16	32	CLK CYCLES	NOTE2
t _{STI}	DELAY FROM STOP TO INTERRUPT (THRE)	8	8	CLK CYCLES	NOTE2
t _{IR}	DELAY FROM -DISTR (RD IIR) TO RESET INTERRUPT (THRE)		250	ns	100pF LOAD

Modem Control

t _{MDO}	DELAY FROM -DOSTR (WR MCR) TO OUTPUT		200	ns	100pF LOAD
t _{SIM}	DELAY TO SET INTERRUPT FROM MODEM INPUT		200	ns	100pF LOAD
t _{IRM}	DELAY TO RESET INTERRUPT FROM -DISTR (RS MSR)		250	ns	100pF LOAD

Receiver

t _{SINT}	DELAY FROM STOP TO SET INTERRUPT	1	1	CLK CYCLES	NOTE2
t _{RINT}	DELAY FROM -DISTR (RD RBR/RDLSR) TO RESET INTERRUPT		1	μs	100pF LOAD

Parallel Port

t _{DT}	DATA TIME	1		μs	
t _{SB}	STROBE TIME	1	500	μs	
t _{AD}	ACKNOWLEDGE DELAY (BUSY START TO ACKNOWLEDGE)			μs	DEFINED BY PRINTER
t _{AKD}	ACKNOWLEDGE DELAY (BUSY END TO ACKNOWLEDGE)			μs	DEFINED BY PRINTER
t _{AK}	ACKNOWLEDGE DURATION TIME			μs	DEFINED BY PRINTER
t _{BSY}	BUSY DURATION TIME			μs	DEFINED BY PRINTER
t _{BSD}	BUSY DELAY TIME			μs	DEFINED BY PRINTER

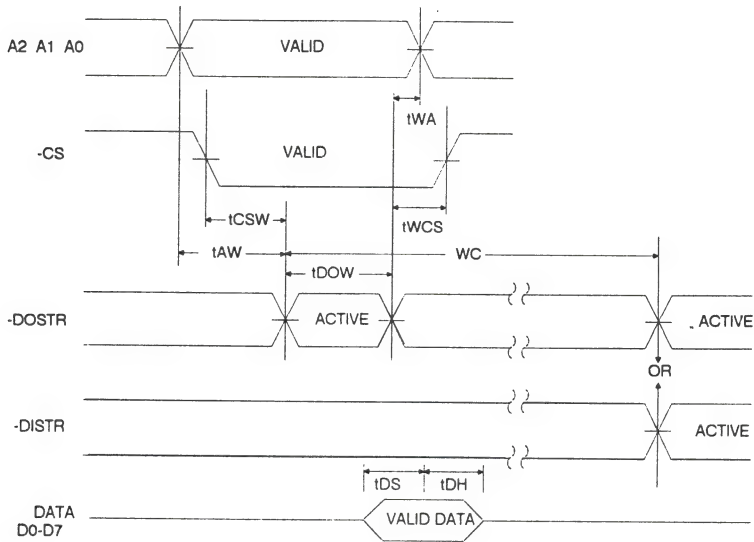
NOTES : 1. THE INTERNAL ADDRESS STROBE IS ALWAYS ACTIVE.

2. RCLK = t_{XH} AND t_{XL}.

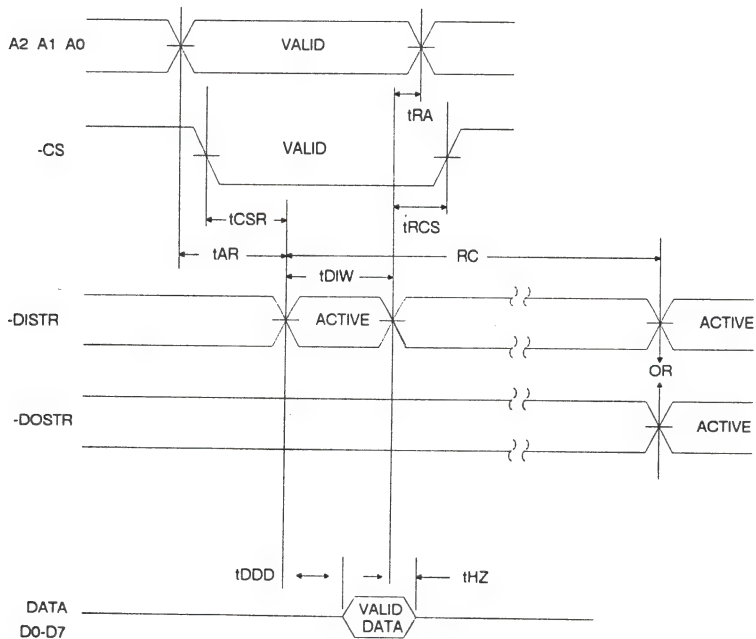
3. CHARGE AND DISCHARGE TIME IS DETERMINED BY VOL,VOH AND THE EXTERNAL LOADING.

4. ALL TIMING ARE REFERENCED TO VALID 0 AND 1. (SEE AC TEST POINTS)

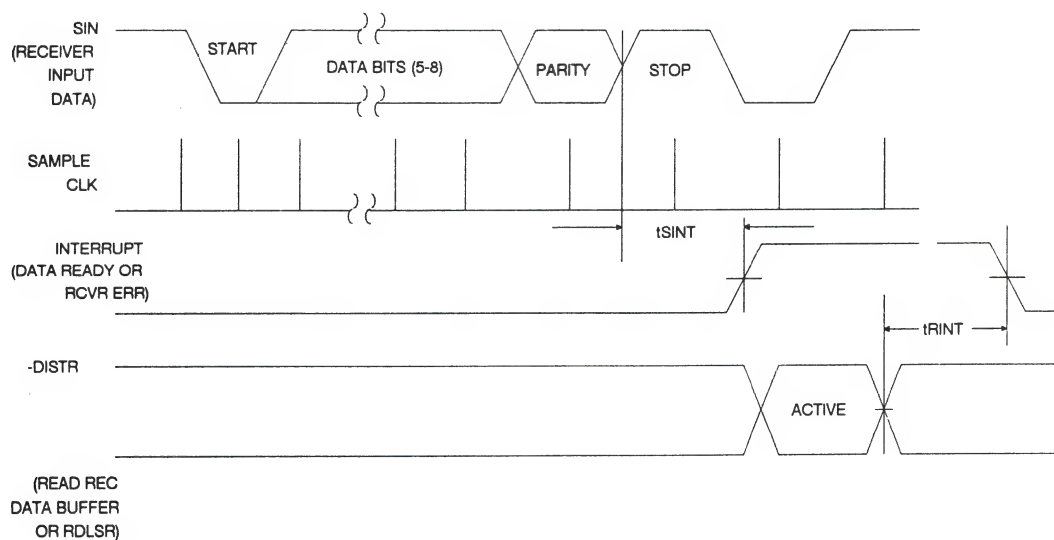
WRITE CYCLE TIMING



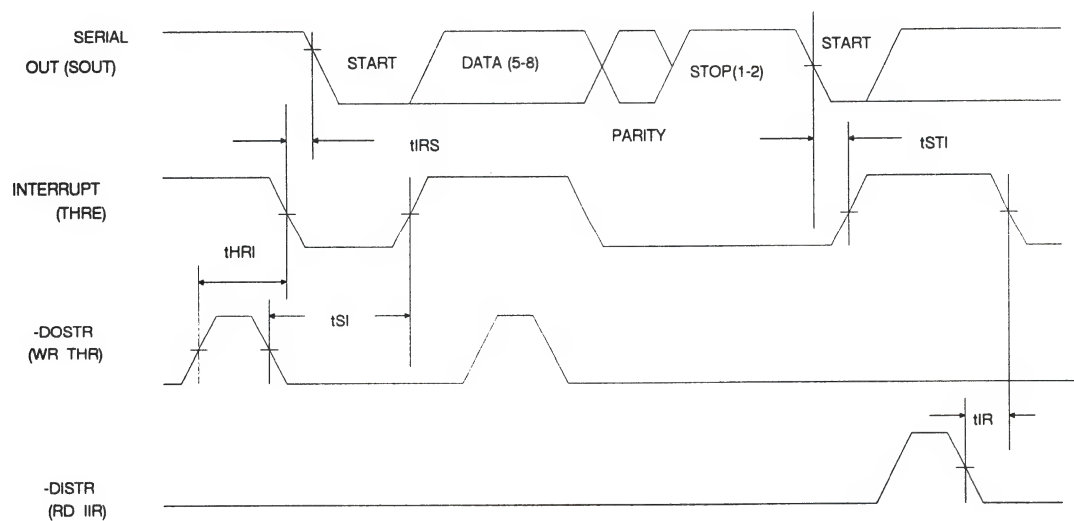
READ CYCLE TIMING



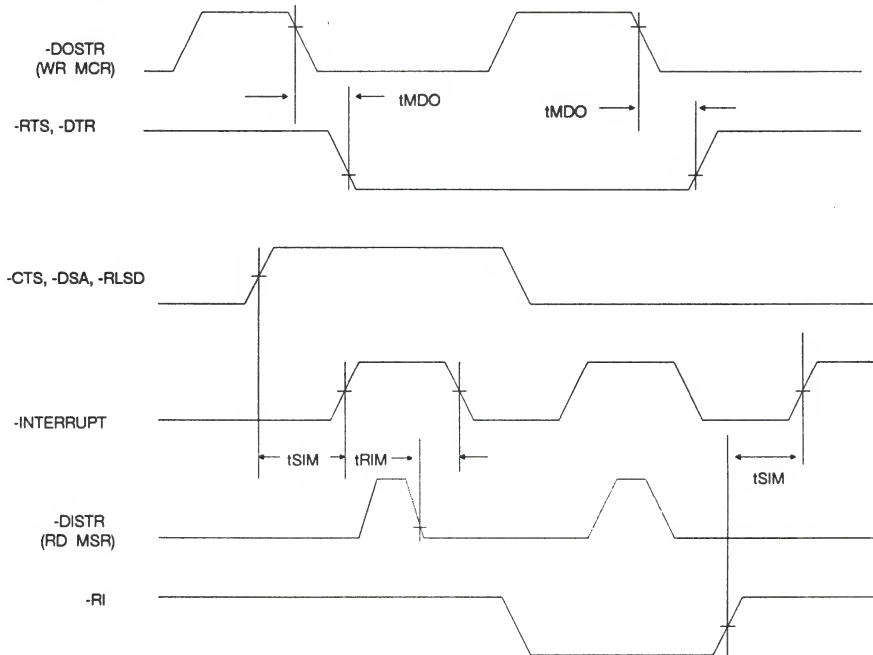
RECEIVER TIMING



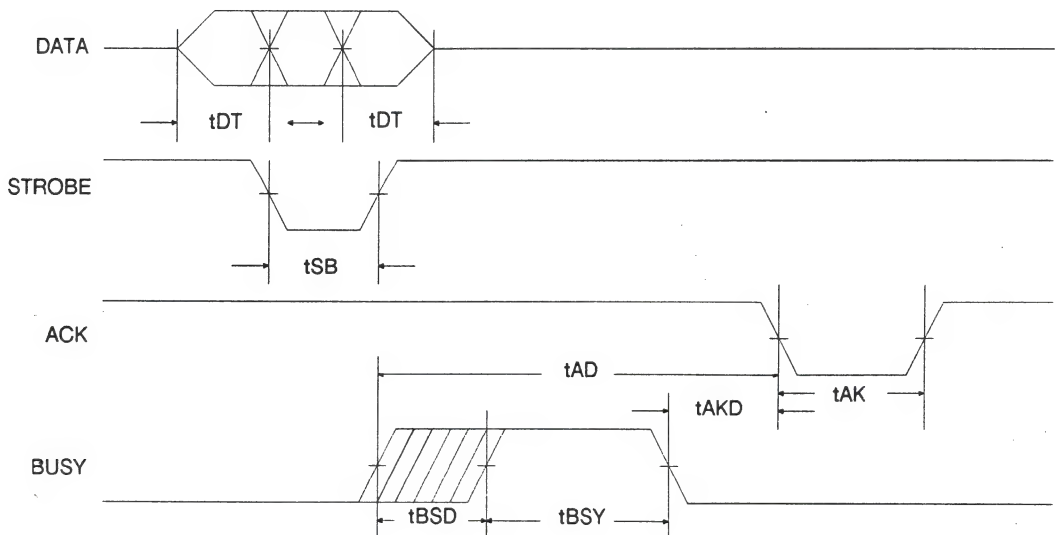
TRANSMITTER TIMING



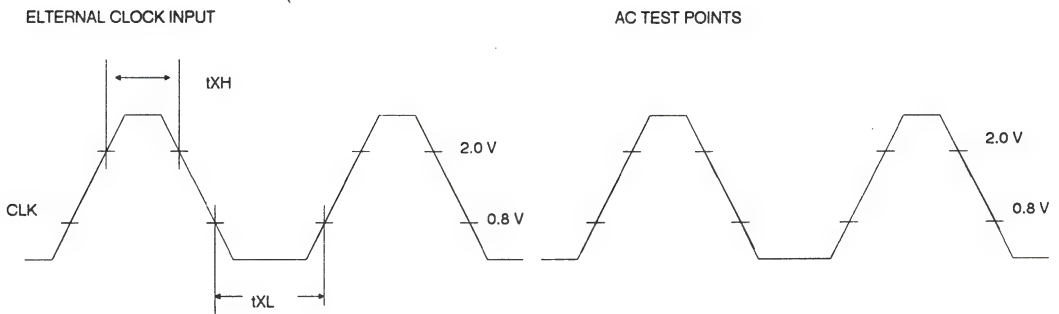
MODEM TIMING



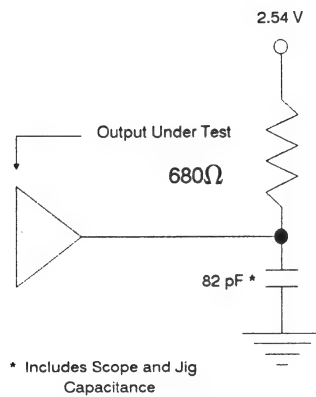
PARALLEL PORT TIMING



AC TESTING INPUT/OUTPUT WAVEFORMS



TEST CIRCUIT



DC CHARACTERISTICS $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{ILX}	CLOCK INPUT LOW VOLTAGE	-0.5	0.8	V	
V_{IHx}	CLOCK INPUT HIGH VOLTAGE	2.0	V_{CC}	V	
V_{IL}	INPUT LOW VOLTAGE	0.5	0.8	V	
V_{IH}	INPUT HIGH VOLTAGE	2.0	V_{CC}	V	
V_{OL}	OUTPUT LOW VOLTAGE		0.4	V	$I_{OL} = 4.0\text{mA}$ ON DB0-DB7 $I_{OL} = 12\text{mA}$ ON PD0-PD7 $I_{OL} = 10\text{mA}$ ON -INIT, -AFD, -STB, AND -SLIN (SEE NOTE 1) $I_{OL} = 2.0\text{mA}$ ON ALL OTHER OUTPUTS
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	$I_{OH} = -0.4\text{mA}$ ON DB0-DB7 $I_{OH} = -2.0\text{mA}$ ON PD0-PD7 $I_{OH} = -0.2\text{mA}$ ON -INIT, -AFD, -STB, AND -SLIN $I_{OH} = -0.2\text{mA}$ ON ALL OTHER OUTPUTS
I_{CC}	POWER SUPPLY CURRENT		50	mA	$V_{CC} = 5.25\text{V}$, NO LOADS ON SINO 1. -DSR0,1; -RLSD0,1; -CTS0,1 -RI0, -RI1 = 2.0V OTHER INPUTS = 0.8V BAUD RATE GENERATOR = 4 MHz BAUD RATE = 56K
I_{IL}	INPUT LEAKAGE		± 10	μA	$V_{CC} = 5.25\text{V}$, GND = 0V ALL OTHER PINS FLOATING.
I_{CL}	CLOCK LEAKAGE		± 10	μA	$V_{IN} = 0\text{V}, 5.25\text{V}$
I_{OZ}	3-STATE LEAKAGE		± 20	μA	$V_{CC} = 5.25\text{V}$, GND = 0V $V_{OUT} = 0\text{V}, 5.25\text{V}$ 1) CHIP DESELECTED 2) CHIP AND WRITE MODE SELECTED
$V_{IL}(\text{RES})$	RESET SCHMITT V_{IL}		0.8	V	
$V_{IH}(\text{RES})$	RESET SCHMITT V_{IH}	2.0		V	

NOTE1: -INIT, -AFD, -STB, AND -SLIN ARE OPEN COLLECTOR OUTPUT PINS THAT EACH HAVE AN INTERNAL PULL-UP RESISTOR ($2.5\text{k}\Omega$ - $3.5\text{k}\Omega$) TO V_{CC} . THIS WILL GENERATE A MAXIMUM OF 2.0mA INTERNAL I_{OL} . IN ADDITION TO THIS INTERNAL CURRENT, EACH PIN WILL SINK AT LEAST 10mA, WHILE MAINTAINING THE V_{OL} SPECIFICATION OF 0.4V MAX.

GM16C452

PARALLEL/ASYNCHRONOUS COMMUNICATIONS ELEMENT

DESCRIPTION

The GM16C452 is a dual universal asynchronous receiver and transmitter with a bidirectional CENTRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 56kHz. The GM16C452 fabricated in an advanced 2μ CMOS process to achieve low power drain and high speed requirements. The GM16C452 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or Modem. The GM16C452 also provides the user with a fully bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on board status of the transfer operations being performed. The GM16C452 also has complete modem control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link. The GM16C452 can interface easily to the most popular microprocessor and communication link faults can be detected with internal loopback capability.

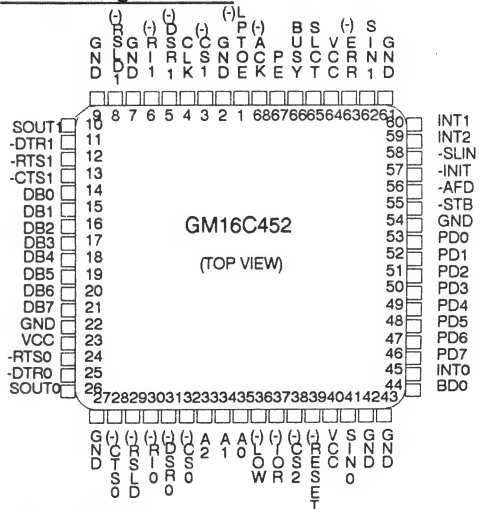
FEATURE

- Pin-to-Pin and functionally compatible to VL16C452
- Bidirectional printer port
- Modem control signals (CTS-, RTS-, DSR-, DRT-, RI-, CD-)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or parity bit generation and detection
- Direct replacement of logic for PC/XT/AT
- Status report register
- Independent transmit and receiver control
- TTL compatible inputs, outputs
- Fully compatible with all new bidirectional PS/2 printer port
- High data transfer rate

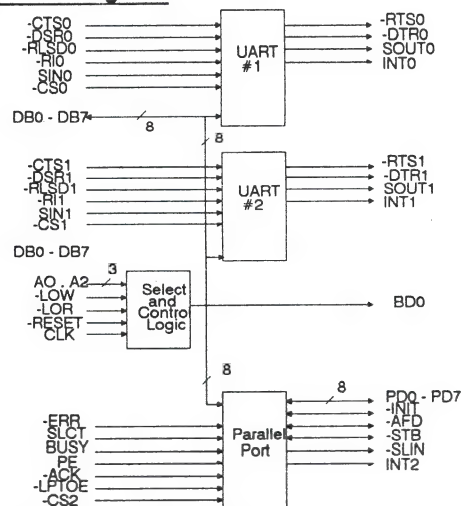
Absolute Maximum Ratings

Ambient Operating Temperature	-10°C ~ + 70°C
Strobe temperature	-65°C + 150°C
Supply Voltage to GND Potential	-0.5V ~ Vcc + 0.3V
Applied Output Voltage	-0.5V ~ Vcc + 0.3V
Applied Input Voltage	-0.5V ~ 7.0V
Power Dissipation	500mW

Pin Configurations



Block Diagram



SIGNAL DESCRIPTION

Signal Name	Pin No.	Signal Description
IOR	37	Input/Output Read Strobe: This is an active low input which causes the selected channel to output data to the data bus (DB0-DB7). The data output depends upon the register selected by the address inputs A0,A1,A2. Chip select 0 (-CS0) selects UART #1, chip select 1 (-CS1) selects UART #2, and chip select 2 (-CS2) selects the line printer port.
IOW	36	Input/Output Write Strobe: This is an active low input which causes data from the data bus (DB0-DB7) to be input to either UART or to the parallel port. The data input depends upon the register selected by the address inputs A0,A1,A2. The chip select inputs (-CS0 -CS1 -CS2) enable the UART#1, UART#2 and the parallel port(respectively).
DB0-DB7	14-12	Data Bits DB0-DB7: The Data Bus provides eight, three state I/O lines for the transfer of data, control and status information between the GM16C452 and the CPU. These lines are normally in a high impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
A0,A1,A2	35,34,33	Address Lines A0-A2: The address lines select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels. Table 11 for the decode of the parallel line printer port.
CLK	4	Clock Input: The external clock input to the UART baud rate divisor.
SOUT0 SOUT1	26, 10	Serial Data Output: These lines are the serial data outputs from the UART's transmitter circuitry. A mark(1) is a logic "one" (high) and space (0) is a logic "zero"(low). Each SOUT0 is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
-CTS0 -CTS1	28, 13	Clear to Send Inputs: The logical state of the -CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR(4)] of each UART. A change of state in either -CTS pin, since the previous reading of the associated MSR causes the setting of DCTS [MSR(0)] to each Modem Status Register. When a -CTS pin is low, the modem is indicating that data on the associated SOUT0 can be transmitted.
DSR0 DSR1	31, 5	Data Set Ready Inputs: The logical state of the DSR pin is reflected in MSR(5) of its associated Modem Status Register. DSR[MSR(1)] indicates whether the associated DSR pin has changed state since the previous reading of the MSR. When a DSR0 pin is low, the modem is indicating that it is ready to exchange data with the associated UART.
DTR0 DTR1	25, 11	Data Terminal Ready Lines: Each DTR pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0 of its associated UART. This signal is cleared (high) by writing a logic 0 to the DTR bit[MCR(0)] or whenever a reset occurs. When active (low), the DTR0 pin indicates to the DCE that its UART is ready to receive data.
-RTS0 -RTS1	24, 12	Requests to Send Output: The -RTS signal is an output on the UART used to enable the modem. An -RTS pin is set low by writing a logic 1 to MCR(1) bit 1 of its UART's Modem Control Register. Both -RTS pins are reset high by Reset. When active, an -RTS pin indicates to the DCE that its UART has data ready to transmit. In half duplex operations, -RTS is used to control the direction of the line.
-R10, -R11	30, 6	Ring Indicator Input: When low, -R1 indicates that a telephone ringing signal has been received by the modem or data set. The -R1 signal is a modem control input whose condition is tested by reading MSR(6) (RI) of the UART. The Modem Status Register output TER1[MSR(2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER(3)=1] and -R1 changes from a high to low, an interrupt is generated.

SIGNAL DESCRIPTION(Cont'd)

Signal Name	Pin No.	Signal Description
-LPTOE	1	Line Printer Output Enable: This input signal enables the parallel line printer when it is low. When this signal is high, the pins of the line printer are held in a high-impedance state. This line may be tied to ground for normal line printer operation.
SINO SIN1	41, 62	Serial Data Input: The serial data inputs moves information from the communication line or modem to the GM16C452 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
-RLSD0 -RLSD1	29, 8	Receive Line Signal Detect: When low, -RLSD output indicates that the data carrier has been detected by the modem or data set. -RLSD is modem input whose condition can be tested by the CPU by reading MSR(7)(RLSD) of the Modem Status Registers. MSR(3)(DRLSD) of the Modem Status Registers indicates whether the -RLSD input has changed since the previous reading of the MSR. -RLSD has no effect on the receiver. If the -RLSD changes state with the modem status interrupt enabled, an interrupt is generated.
-RESET	39	Reset: When low, the reset input forces the GM16C452 into an idle mode in which all serial data activities are suspended. The Modem Control Register(mcr) along with its outputs is cleared. The Line Status Register(LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
INT0 INT1	45, 60	Serial Channel Interrupts: Each serial channel interrupt goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register of its associated channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset operation.
-CS0, -CS1 -CS2	32,3,38	Chip Selects: Each Chip Select input acts as an enable for the write and read signals for the serial channels 0 (-CS0) and 1 (-CS1), -CS2 enables the signals to the line printer port.
BD0	44	Bus Buffer Output: The active high output is asserted when this serial channel or the parallel port is read. This output can be used to control the system bus driver device (74LS245)
PDO- PD7	53-46	Parallel Data Bits(0-7): These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when the port is not selected (-CS2 is high).
-STB	55	Line Printer Strobe: This I/O line provides communication between the GM16C452 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
-AFD	56	Line Printer Autofeed: This I/O line provides the line printer with an active low signal when continuous from paper is to be autofeed to the printer.
-INIT	57	Line Printer Initialize: This I/O line provides the line printer with a signal that allows the line printer initialization routine to be started.

SIGNAL DESCRIPTION(Cont'd)

Signal Name	Pin No.	Signal Description
-SLIN	58	Line Printer Select: This I/O line selects the printer when it is active low.
INT2	59	Interrupt Printer Port: This signal is an input line from the line printer that goes active high when an error signal is received. The interrupt is reset low upon a reset operation.
-ERR OR	63	Line Printer Error: This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition. This causes INT2 to be asserted high.
SLCT	65	Line Printer Selected: This is an input line from the line printer that goes high when the line printer has been selected.
BUSY	66	Line Printer Busy: This is an input line from the line printer that goes high when the line printer has a local operation in progress.
PE	67	Line Printer Paper Empty: This is an input line from the line printer that goes high when the printer runs out of paper, and causes INT2 to be asserted high.
-ACK	68	Line Printer Acknowledge: This input goes low to indicate a successful data transfer has taken place.
VCC	20,40 64	Power Supply: The power supply requirement is $5V \pm 5\%$
GND	2,7,9,22, 27,42,43 ,54,61	Ground (0 V): All pins must be tied to ground for proper operation.

FUNCTIONAL DESCRIPTION

Serial Channel Register

Three types of internal registers are used in the serial channel of the GM16C452. They are used in the operations of the device, and are the control, status, and data registers. The control registers are the Bit Rate Select Register DLL (Divisor Latch LSB) and DLM (Divisor Latch MSB), Line Control Register, Interrupt Enable Register, and the Modern Control Registers, while the status registers are the Line Status Registers and the Modern Status Register. The Data Registers are the Receiver Buffer Register and the Transmitter Holding Register. The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register [LCR(7)] to select the register to be written or read (see Table 1). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. BIT 0 of a data word is always the first serial data bit received and transmitted. The GM16C452 data registers are double-buffered so that read and write operations can be performed at the same time the UART is performing the parallel-to-serial and serial-to-parallel conversion. The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of

the line characteristics in system memory. The contents

of the LCR are described below.

LCR(0) Word Length Select Bit 0 (WLS0)

LCR(1) Word Length Select Bit 1 (WLS1)

LCR(2) Stop Bit Select (STB)

LSR(3) Parity Enable (PEN)

LCR(4) Even Parity Select (EPS)

LCR(5) Stick Parity

LCR(6) Set Break

LCR(7) Divisor Latch Access Bit (DLAB)

LCR(0) and LCR(1) word length select Bit 1 : The number of bits in each serial character is programmed as shown in the following chart:

LCR(1)	LCR(0)	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8 bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR(3) Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When Parity is enable [LCR(3) = 1]; LCR(4) = 0 selects odd parity, And LCR(4) = 1 selects even parity.

LCR(5) Stick Parity: When parity is enable [LCR(3) = 1], LCR(5) = 1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by

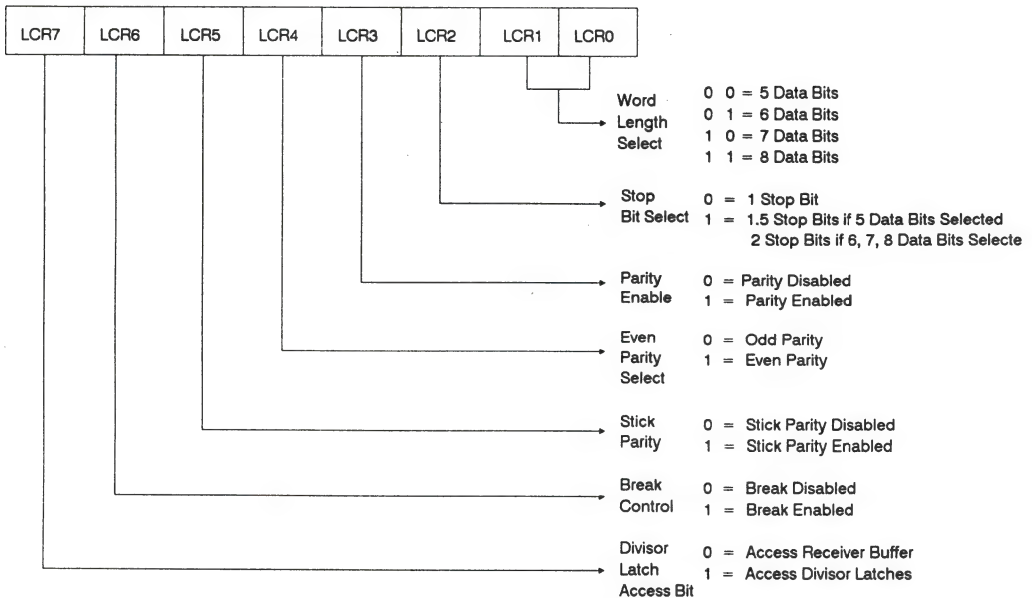
LCR(4).

TABLE 1. SERIAL CHANNEL INTERNAL REGISTERS

DLAB	A2	A1	A0	Mnemonic	Register
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modern Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modern Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care", 0 = Logic Low, 1 = Logic High

Note: Serial Channel 0 is accessed when -CS0 is low; Serial Channel 1 is accessed when -CS1 is low. Selecting both the channels simultaneously is an invalid condition.

FIGURE 1. LINE CONTROL REGISTER

This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to a logic "1", the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic "0". The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all "0"s pad character in response to THRE. 2. Set break in response to the next THRE.
2. Set break in response to the next THRE
3. Wait for the transmitter to be idle (TEMT = 1), and clear break when normal transmission has to be restored.

LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic "1") to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding, or the Interrupt Enable Registers.

The Line Status Register (LSR) is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel of the GM16C452.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is thereby lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received had a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break

TABLE 2. LINE STATUS REGISTER BITS

LSR BITS	Logic 1	Logic 0
LSR(0) Data Ready(DR)	Ready	Not Ready
LSR(1) Overrun Error(OE)	Error	No Error
LSR(2) Parity Error(PE)	Error	No error
LSR(3) Framing Error(FE)	Error	No Error
LSR(4) Break Interrupt(BI)	Break	No Break
LSR(5) Transmitter Holding Register Empty(THRE)	Empty	Not Empty
LSR(6) Transmitter Empty(TEMY)	Empty	Not Empty
LSR(7) Not Used		

reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU

character is an invalid data character. However, it is an entire character, including parity and stop bits.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and may receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the serial channel has completed transmission of the last character to be sent. If the interrupt is enabled [IER(1)], an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR(1) - LSR(4). (OE,PE,FE, and BI). The contents of the Line Status Register shown in Table 2 are described below:

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LSR(4)). The PE bit is set high upon detection of a parity error, and is

reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start Bit + Data Bits + Parity + Stop Bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

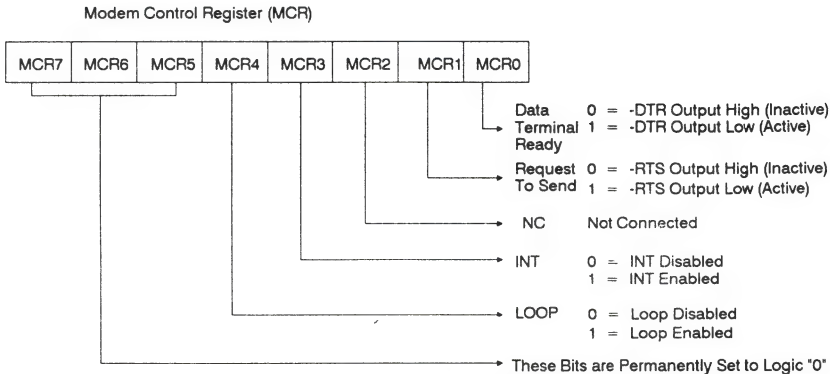
LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2) = 1 in the Interrupt Enable Register. LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the GM16C450 is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enable (IER(1) = 1).THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the

TABLE 3. MODEM CONTROL REGISTER BITS

MCR BITS	LOGIC 1	LOGIC 0
MCR(0) Data terminal Ready(DCR)	-DTR Output Low	-DTR Output High
MCR(1) Request to Send(RTS)	-RTS Output Low	-Rts Output High
MCR(2) 0		
MCR(3) Interrupt(INT) Enable	INT Enabled	INT Disabled
MCR(4) Loop	Loop Enabled	Loop Disabled
MCR(5) 0		
MCR(6) 0		
MCR(7) 0		

FIGURE 2. MODEM CONTROL REGISTER

Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is always 0.

The Modem Control Register (MCR) controls the interface with the modem or data set as described in Table 3. The MCR can be written and read. The -RTS and -DTR outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR Bits 0,1,3 and 4 are shown below:

MCR(0): When MCR(0) is set high, the -DTR output is forced low. When MCR(0) is reset low, the -DTR output is forced high. The -DTR output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the RTS output is forced low. When MCR(1) is reset low, the -RTS output is forced high. The -RTS output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

MCR(3): When MCR(3) is set high, the INT output is enabled.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the

channel. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic "1") state, and the receiver data input Serial Inpit (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The three modem control inputs (-CTS,-DSR, and -RI) are disconnected. The modem control outputs (-DTR and -RTS) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high).

In the Diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Bits MCR(5) -MCR(7) are permanently set to logic 0.

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial channel modem signal inputs by accessing the data bus interface of the GM16C451. In addition to the current status information, four bits of the MSR indicate whether

TABLE 4. MODEM STATUS REGISTER BITS

MSR BITS	Mnemonic	Description
MSR(0)	DCTS	Delta Clear to Send
MSR(1)	DDSR	Delta Data Set Ready
MSR(2)	TERI	Trailing Edge of Ring Indicator
MSR(3)	DRLSD	Delta Data Carrier Detect
MSR(4)	-CTS	Clear to Send
MSR(5)	-DSR	Data Set Ready
MSR(6)	-RI	Ring Indicator
MSR(7)	-RLSD	Receiver Line Signal Detect

the modem inputs have changed since the last reading of the MSR. The Delta Status Bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines for each channel are -CTS, -DSR, -RI and -RLSD. MSR(4) -MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled [IER(3)], a change of state in a modem input signal will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 4. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the -CTS input to the serial channel has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the -DSR input to the serial channel has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the -RI input to the serial channel has changed state from high to low since the last time it was read by the CPU. Low to high transitions on -RI do not activate TERI.

MSR(3) Delta Data Carrier Detect (DRSLD): DRSLD indicates that the -RLSD input to the serial channel has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the -CTS input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in loop mode [MSR(4) = 1], MSR(4) is equivalent to -RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the -DSR input from the modem to the serial channel which indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the channel is in the loop mode [MCR(4) = 1], MSR(5) is equivalent to DTR in the MCR.

MSR(6) Ring Indicator: Indicates the status of the RI input (pin 39). If the channel is in the loop mode

[MCR(4) = 1], MSR(6) is not connected in the MCR.

MSR(7) Receive Line Signal Detect: Receive Line Signal Detect indicates the status of the Receive Line Signal Detect (-RLSD) input. If the channel is in the loop mode [MCR(4) = 1], MSR(4) is equivalent to Out2 of the MCR.

The modem status inputs (-RI, -RLSD, -DSR, and -CTS) reflect the modem input lines with any change of status. Reading the MSR register will clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mark control signals. If a DCTS, DDSR, TERI, or DRLSD are true and a state change occurs during a read operation (-DISTR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DRLSD are false, and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read -DISTR operations. If a status condition is generated during a read -DISTR operation, the status bit is not set until the trailing edge of the read -DISTR.

If a status bit is set during a read -DISTR operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read -DISTR instead of being set again.

Each GM16C452 serial channel contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 3.1 MHz) by any divisor from 1 to 2 to the power of 16-1 (see also BRG description). The output frequency of the Baud Generator is $16 \times$ the data rate [DIVISOR # = Clock / (Baud Rate \times 16)]. Two 8 bit divisor latch registers store the divisor in a 16 bit binary format. These Divisor Latch Register must be loaded during initialization. Upon loading either of the Divisor Latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

The receiver circuitry in each serial channel of the GM16C452 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit LSB = Data Bit 0 [RBR(0)]. Data Bit 0 of a data word [RBR(0)] is the first data bit received. The unused bits in a character less than 8 bit are output low to the parallel output by the serial channel.

Received data at the SIN input pin is shifted into the

Receiver Shift Register by the 16x clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character results in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 Thru 7:

RBR(0) DATA BIT 0
 RBR(1) DATA BIT 1
 RBR(2) DATA BIT 2
 RBR(3) DATA BIT 3
 RBR(4) DATA BIT 4
 RBR(5) DATA BIT 5
 RBR(6) DATA BIT 6
 RBR(7) DATA BIT 7

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused

bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 [THR(0)] is the first serial data bit transmitted. The THRE flag [LSR(5)] reflects the status of the THR. The TEMT flag [LSR(5)] indicates if both the THR and TSR are empty.

THR Bits thru 7

THR(0) DATA BIT 0
 THR(1) DATA BIT 1
 THR(2) DATA BIT 2
 THR(3) DATA BIT 3
 THR(4) DATA BIT 4
 THR(5) DATA BIT 5
 THR(6) DATA BIT 6
 THR(7) DATA BIT 7

Scratchpad Register is an 8 bit Read/Write register that has no effect on any channel in the GM16C452. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR(0) DATA BIT 0
 SCR(1) DATA BIT 1
 SCR(2) DATA BIT 2
 SCR(3) DATA BIT 3
 SCR(4) DATA BIT 4
 SCR(5) DATA BIT 5
 SCR(6) DATA BIT 6
 SCR(7) DATA BIT 7

TABLE 5. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
Bit2	Bit 1	Bit 0	Priority level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Received Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the interrupt Source or THR Write
0	0	0	Fourth	Modem Status	-CTS, -DSR -RI, -RSLD	MSR Read

x = Not Defined

FIGURE 3. INTERRUPT CONTROL LOGIC

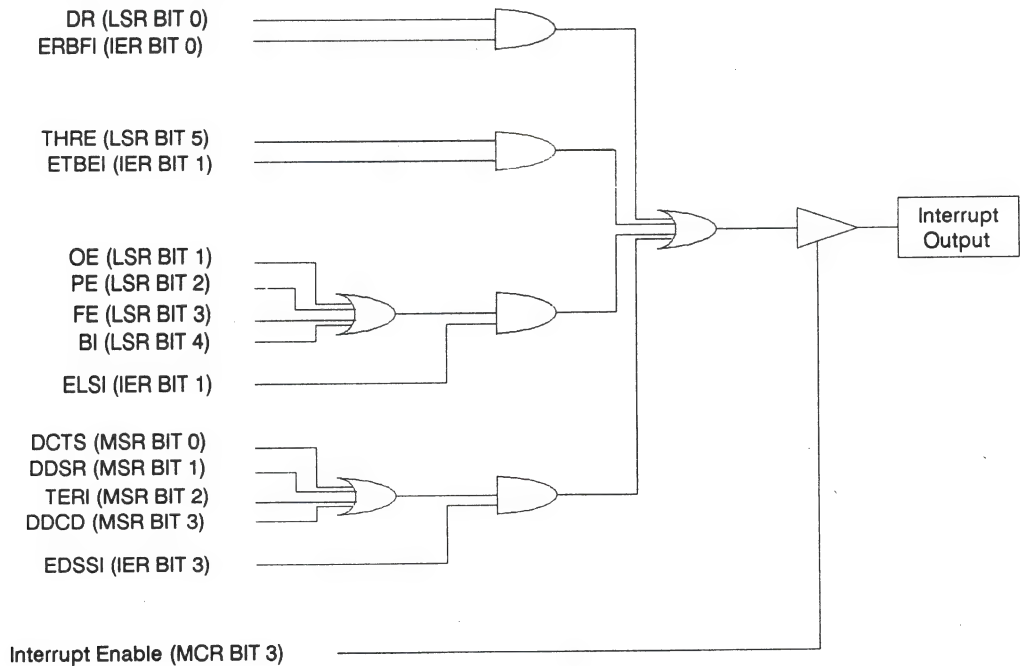


TABLE 6. SERIAL CHANNEL ACCESSIBLE REGISTERS

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit(1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(O/e) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Ready Set	(CTS) Clear to Send	(DRSLD) Delta Receive Line Signal Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

LSB Data Bit 0 is the first bit transmitted or received.

INTERRUPTS

The Interrupt Identification Register (IIR) in the serial channel of the GM16C452 has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, The IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The logic equivalent of the interrupt control circuit is shown in the Figure 3. The contents of the IIR are indicated in Table 5 and are described below.

IIR(0): IIR(0) can be used in either as hard wired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

The Interrupt Enable Register (IER) is a Write Register used to independently enable the four serial channel interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in

their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 3 and are described below.

IER(0): When programmed high [IER(0) = LOGIC 1], IER(0) enables Received Data Available Interrupt.

IER(1): When programmed high [IER(1) = LOGIC 1], IER(1) enables the Transmitter Holding Register Empty Interrupt.

IER(2): When programmed high [IER(2) = LOGIC 1] IER(2) enables Receiver Line Status Interrupt.

IER(3): When programmed high [IER(3) = LOGIC 1], IER(3) enables the Modem Status Interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

TRANSMITTER

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5- to -8 bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, both THRE and TEMT are high. The first word write causes THRE to be reset to 0. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

RECEIVER

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16x clock to $7 \frac{1}{2}$, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0),LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status information for the receiver is provided in the Line Status Register to the Receiver Buffer Register, the Data Received indication in LSR(0) is set high. The CPU reads the Receiver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR(2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3)

The center of the start bit is defined as clock count $7 \frac{1}{2}$. If the data into SIN is symmetrical square wave, the center of the data cells will occur within $\pm 3.125\%$ of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16x clock cycle prior to being detected.

BAUD RATE GENERATOR (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG is provided by an external clock into CLK.

The data rate is determined by the Divisor Latch registers registers DLL and DLM and the external frequency. The bit rate is selected by programming the

two Divisor Latches, Divisor Latch Most Significant Byte and Division Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at the CLK input).

The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432MHz, 2.4576MHz, 3.072MHz. With these frequencies, standard bit rates from 50 to 38.5kbps are available. Tables 7,8,9 illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

RESET

After power up, the GM16C451 -Reset input (MR) should be held low for 500ns to reset the GM16C451 circuits to an idle mode until initialization. A low on -Reset causes the following

- 1.Initializes the transmitter and receiver internal clock counters.
- 2.Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of The reset condition (Reset high), The GM16C451 remains in the idle mode until programmed.

A hardware reset of the GM16C451 sets the THRE and TEMT status bit in the LSR. When Interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a reset on the GM16C451 is given in Table 10.

PROGRAMMING

Each serial channel of the GM16C451 is programmed by the control registers LCR, IER, DLL and DLM, MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface. While the control register can be written in any order, the IER should be written to last because it controls the interrupt enables. Once a serial channel is programmed and operational, these registers can be updated any time the GM16C451 serial channel is not transmitting or receiving data.

The control signals required to access each serial channel's internal registers are shown below.

SOFTWARE RESET

A software reset of the serial channel is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

CLOCK INPUT OPERATION

The maximum input frequency of the external clock of the GM16C452 is 3.1MHz

TABLE 7. BAUD RATES (1.8432 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 8. BAUD RATES (2.4576 MHz CLOCK)

Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

TABLE 9. BAUD RATES (3.072 MHz CLOCK)

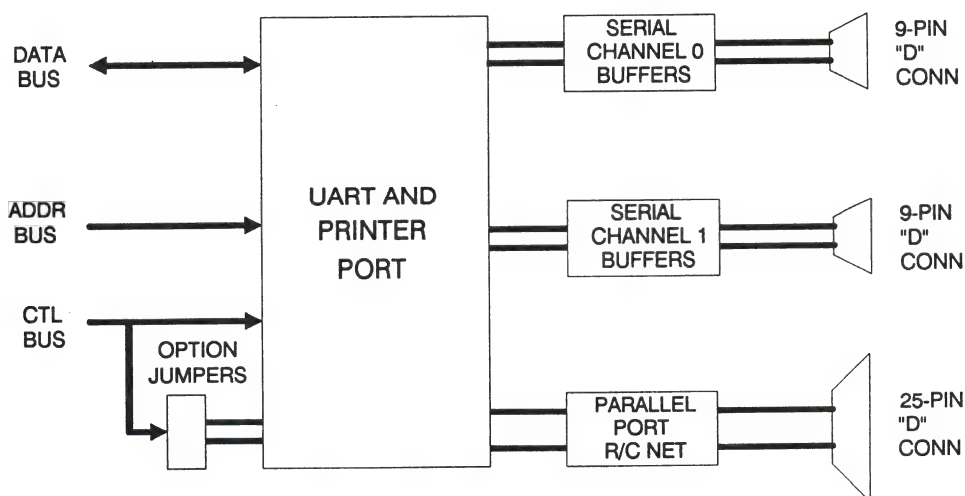
Desired Baud Rate	Divisor Used	Percent Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

TABLE 10. RESET

Register/Signal	Reset Control	Reset
INTERRUPT ENABLE REGISTER	RESET	ALL BITS LOW (0-3 FORCED AND 4-7 PERMANENT)
INTERRUPT IDENTIFICATION REGISTER	RESET	BIT 0 IS HIGH, BITS 1 AND 2 LOW
LINE CONTROL REGISTER	RESET	BITS 3-7 ARE PERMANENTLY LOW
MODEM CONTROL REGISTER	RESET	ALL BITS LOW
LINE STATUS REGISTER	RESET	ALL BITS LOW
MODEM STATUS REGISTER	RESET	ALL BITS LOW, EXCEPT BITS 5 AND 6 HIGH
SOUT	RESET	BITS 0-3 LOW
INTRPT(RCVR ERRS)	READ LSR/RESET	BITS 4-7 INPUT SIGNAL
INTRPT(RCVR Data Ready)	READ RBR/RESET	HIGH
INTRPT(THRE)	READ IIR/WRITE THR/RESET	LOW
INTRPT(MODEM STATUS CHANGES)	READ MSR/RESET	LOW
-OUT2	RESET	HIGH
-RTS	RESET	HIGH
-DTR	RESET	HIGH
-OUT1	RESET	HIGH

DEVICE APPLICATION

GM16C451



FUNCTIONAL DESCRIPTION

PARALLEL PORT REGISTERS

The GM16C452's parallel port interfaces the device to a Centronics style printer. When Chip Select 2 (-CS2) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read (-IOR) and write (-IOW) pin as shown. The top four registers are read-only registers, and the bottom four are write-only registers. Since the parallel port is bidirectional, the first register (READ PORT) allows the microprocessor to read the information on the parallel bus. The second register (READ STATUS) allows the microprocessor to read the status of the printer in the five most significant bits. The status bits are Printer Busy (dBUSY), Acknowledge (ACK) which is a handshake function, Paper Empty (PE), Printer Selected (SLCT), and Error (ERROR). The third register (READ CONTROL) functions are duplicated in the sixth register (WRITE CONTROL). The control bits are found in the five least significant bits of these registers. They are interrupt Enable (IRQ ENB), Select In (SLIN), Initialize the Pprinter (INIT), Autofeed the Paper (AUTOFD), Strobe (STROBE), which informs the printer of the presence of a valid byte on the parallel bus. The fifth register (WRITE PORT) allows the microprocessor to write a byte to the printer.

The parallel port is completely compatible with the parallel port implementation used in the IBM Serial/Parallel Adaptor.

TABLE 11. PARALLEL PORT REGISTERS

Register	Register Bits							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Port	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	PD 0
Read Status	-BUSY	-ACK	PE	SLCT	-ERROR	1	1	1
Read Control	1	1	1	IRQ ENB	SLIN	-INIT	AUTOFD	STROBE
Write Data	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	PD 0
Write Control	1	1	1	IRQ ENB	SLIN	-INIT	AUTOFD	STROBE

TABLE 12. PARALLEL PORT REGISTER SELECT

Control Pins					Register Selected
-IOR	-IOW	-CS2	A1	A0	
0	1	0	0	0	Read Port
0	1	0	0	1	Read Status
0	1	0	1	0	Read Control
0	1	0	1	1	Invalid
1	0	0	0	0	Write Port
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control
1	0	0	1	1	Invalid

AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5V ± 5% (Note 1,5)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
tDIW	-DISTR STROBE WIDTH	125		ns	
RC	READ CYCLE	360		ns	
tDDD	DELAY FROM -DISTR TO DATA		125	ns	100pF LOAD
tHz	-DISTR TO FLOATING DATA WIDTH	0	100	ns	100pF LOAD, NOTE 4
tDOW	-DOSTR STROBE WIDTH	100		ns	
WC	WRITE CYCLE	360		ns	
tDS	DATA SETUP TIME	40		ns	
tDH	DATA HOLD TIME	40		ns	
tRA	ADDRESS HOLD TIME FROM -DISTR	20		ns	NOTE2
tRCS	CHIP SELECT HOLD TIME FROM DISTR	20		ns	NOTE2
tAR	-DISTR DELAY FROM ADDRESS	60		ns	NOTE2
tCSR	-DISTR DELAY FROM CHIP SELECT	50		ns	NOTE2
tWA	ADDRESS HOLD TIME FROM -DOSTR	20		ns	NOTE2
tWCS	CHIP SELECT HOLD TIME FROM -DOSTR	20		ns	NOTE2
tAW	-DOSTR DELAY FROM ADDRESS	60		ns	NOTE2
tCSW	-DOSTR DELAY FROM SELECT	50		ns	NOTE2
tRW	RESET PULSE WIDTH	5		μs	
tXH	DURATION OF CLOCK HIGH PULSE	140		ns	EXTERNAL CLOCK
tXL	DURATION OF CLOCK LOW PULSE	140		ns	EXTERNAL CLOCK

NOTES : 1. RCLK IS INTERNALLY DERIVED FROM THE INTERNAL -BAUDOUT SIGNAL.

2. THE INTERNAL ADDRESS STROBE IS ALWAYS ACTIVE.

3. RCLK = tXH AND tXL.

4. CHARGE AND DISCHARGE TIME IS DETERMINED BY VOL, VOH AND THE EXTERNAL LOADING.

5. ALL TIMING ARE REFERENCED TO VAILD 0 AND 1. (SEE AC TEST POINTS.)

6. ALL TIMING SPECIFICATIONS APPLY TO PINS ON BOTH SERIAL CHANNELS (e.g. Ri REFERS TO BOTH R10 AND R11).

AC CHARACTERISTICS (Cont.) TA = 0°C TO 70°C, VCC = 5V + 5% (Note 1, 5)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
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Transmitter

t _{HR1}	DELAY FROM RISING EDGE OF DOSTR (WR THR) TO RESET INTERRUPT		175	ns	100pF LOAD
t _{IRS}	DELAY FROM INITIAL INTR RESET TO TRANSMIT START	8	24	CLK CYCLES	NOTE3
t _{SI}	DELAY FROM INITIAL WRITE TO INTERRUPT	16	32	CLK CYCLES	NOTE3
t _{STI}	DELAY FROM STOP TO INTERRUPT (THRE)	8	8	CLK CYCLES	NOTE3
t _{IR}	DELAY FROM -DISTR (RD IIR) TO RESET INTERRUPT (THRE)		250	ns	100pF LOAD

Modem Control

t _{MDO}	DELAY FROM -DOSTR (WR MCR) TO OUTPUT		200	ns	100pF LOAD
t _{SIM}	DELAY TO SET INTERRUPT FROM MODEM INPUT		200	ns	100pF LOAD
t _{RIM}	DELAY TO RESET INTERRUPT FROM -DISTR (RS MSR)		250	ns	100pF LOAD

Receiver

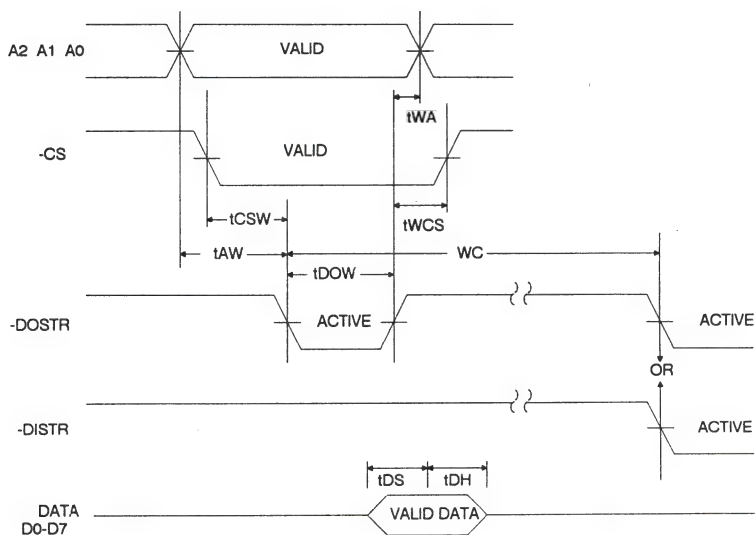
t _{SINT}	DELAY FROM STOP TO SET INTERRUPT	1	1	CLK CYCLES	NOTE3
t _{RINT}	DELAY FROM -DISTR (RD RBR/RDLSR) TO RESET INTERRUPT		1	μs	100pF LOAD

Parallel Port

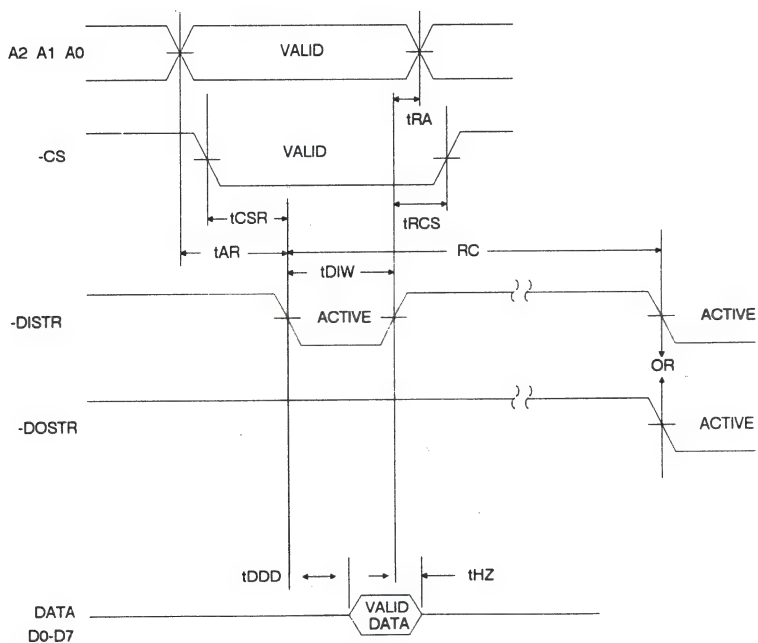
t _{DT}	DATA TIME	1		μs	
t _{SB}	STROBE TIME	1	500	μs	
t _{AD}	ACKNOWLEDGE DELAY (BUSY START TO ACKNOWLEDGE)			μs	DEFINED BY PRINTER
t _{AKD}	ACKNOWLEDGE DELAY (BUSY END TO ACKNOWLEDGE)			μs	DEFINED BY PRINTER
t _{AK}	ACKNOWLEDGE DURATION TIME			μs	DEFINED BY PRINTER
t _{BSY}	BUSY DURATION TIME			μs	DEFINED BY PRINTER
t _{BSD}	BUSY DELAY TIME			μs	DEFINED BY PRINTER

- NOTES : 1. ALL TIMING SPECIFICATIONS APPLY TO PINS ON BOTH SERIAL CHANNELS (e.g. RI REFERS TO BOTH R10 AND R11).
 2. THE INTERNAL ADDRESS STROBE IS ALWAYS ACTIVE.
 3. RCLK = t_{xH} AND t_{xL}.
 4. CHARGE AND DISCHARGE TIME IS DETERMINED BY VOL,VOH AND THE EXTERNAL LOADING.
 5. ALL TIMING ARE REFERENCED TO VALID 0 AND 1. (SEE AC TEST POINTS)

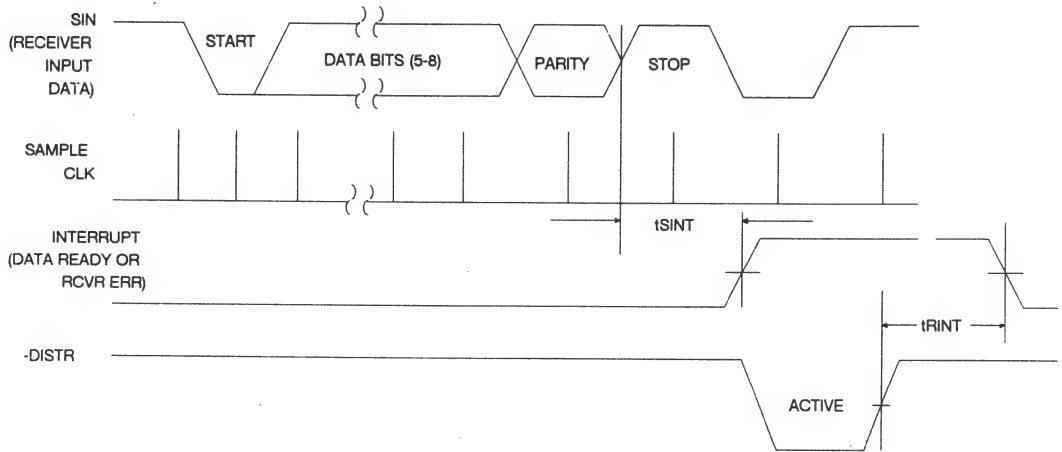
WRITE CYCLE TIMING



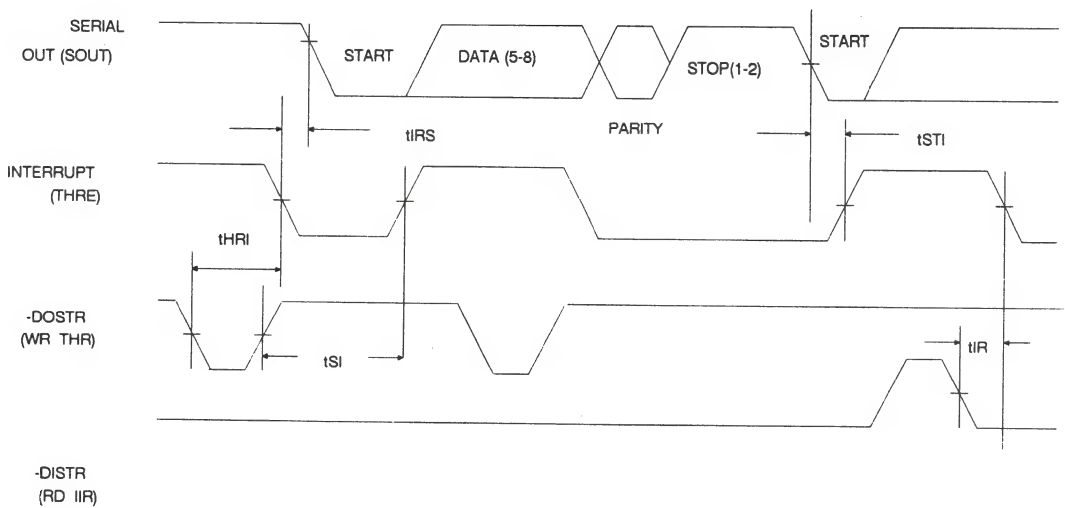
READ CYCLE TIMING



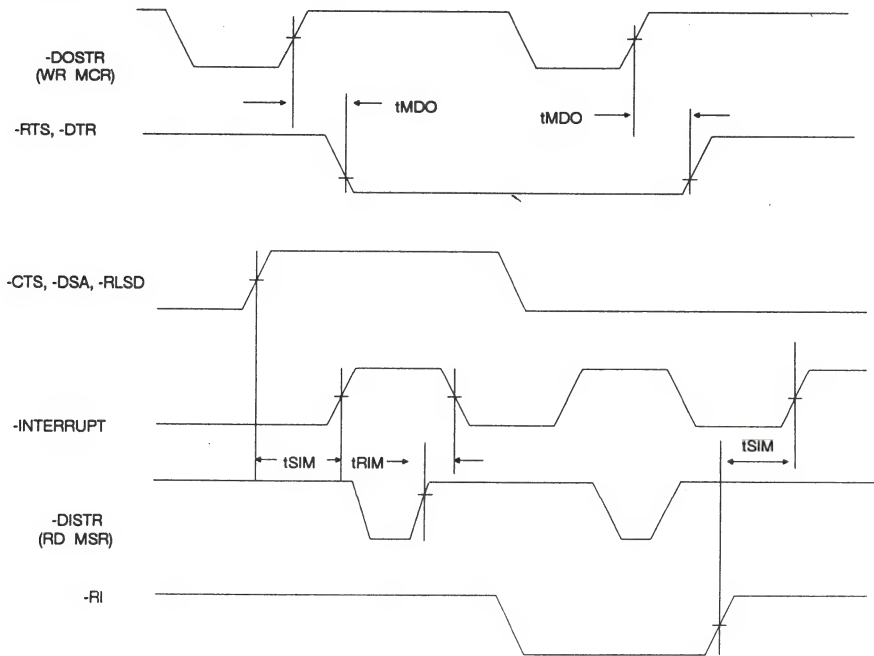
RECEIVER TIMING



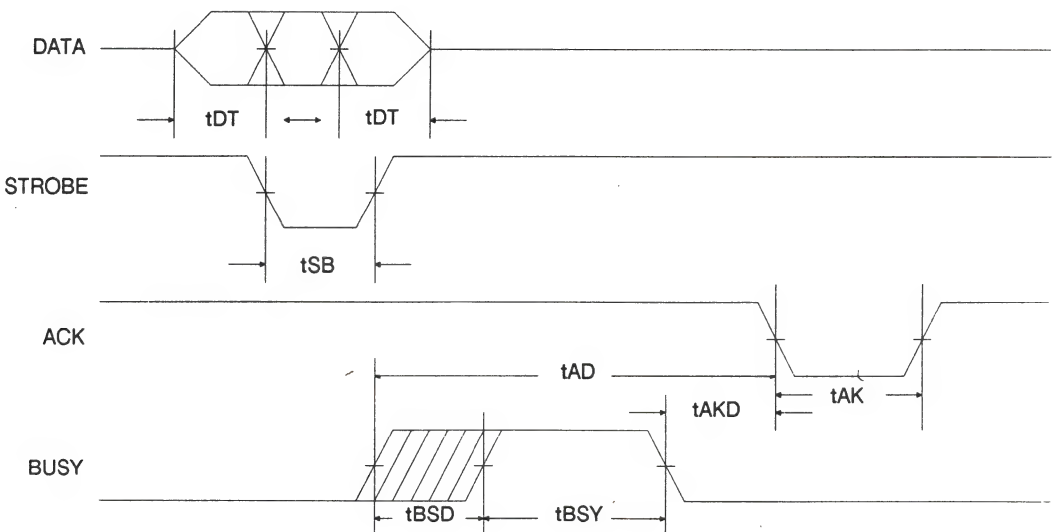
TRANSMITTER TIMING



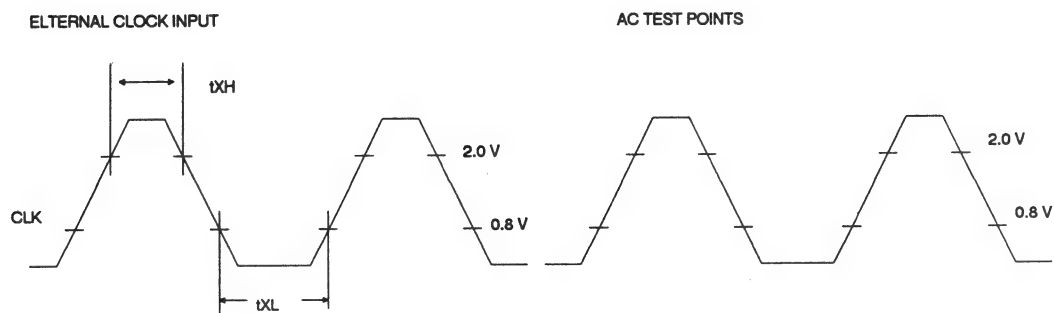
MODEM TIMING



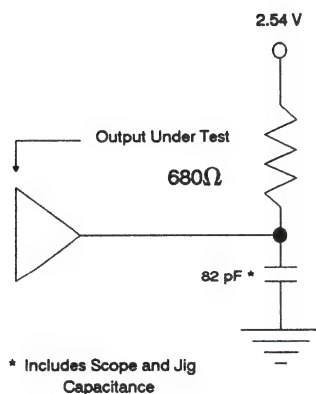
PARALLEL PORT TIMING



AC TESTING INPUT/OUTPUT WAVEFORMS



TEST CIRCUIT



DC CHARACTERISTICS $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{ILX}	CLOCK INPUT LOW VOLTAGE	-0.5	0.8	V	
V_{IHx}	CLOCK INPUT HIGH VOLTAGE	2.0	V_{CC}	V	
V_{IL}	INPUT LOW VOLTAGE	0.5	0.8	V	
V_{IH}	INPUT HIGH VOLTAGE	2.0	V_{CC}	V	
V_{OL}	OUTPUT LOW VOLTAGE		0.4	V	$I_{OL} = 4.0\text{mA}$ ON DB0-DB7 $I_{OL} = 12\text{mA}$ ON PD0-PD7 $I_{OL} = 10\text{mA}$ ON -INIT, -AFD, -STB, AND -SLIN (SEE NOTE 1) $I_{OL} = 2.0\text{mA}$ ON ALL OTHER OUTPUTS
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	$I_{OH} = -0.4\text{mA}$ ON DB0-DB7 $I_{OH} = -2.0\text{mA}$ ON PD0-PD7 $I_{OH} = -0.2\text{mA}$ ON -INIT, -AFD, -STB, AND -SLIN $I_{OH} = -0.2\text{mA}$ ON ALL OTHER OUTPUTS
I_{CC}	POWER SUPPLY CURRENT		50	mA	$V_{CC} = 5.25\text{V}$, NO LOADS ON SINO 1. -DSR0,1; -RLSD0,1;-CTS0,1 -RI0,-RI1 = 2.0V OTHER INPUTS = 0.8V BAUD RATE GENERATOR = 4 MHz BAUD RATE = 56K
I_{IL}	INPUT LEAKAGE		± 10	μA	$V_{CC} = 5.25\text{V}$, GND = 0V ALL OTHER PINS FLOATING.
I_{CL}	CLOCK LEAKAGE		± 10	μA	VIN = 0V, 5.25V
I_{OZ}	3-STATE LEAKAGE		± 20	μA	$V_{CC} = 5.25\text{V}$, GND = 0V VOUT = 0V, 5.25V 1) CHIP DESELECTED 2) CHIP AND WRITE MODE SELECTED
$V_{IL}(\text{RES})$	RESET SCHMITT V_{IL}		0.8	V	
$V_{IH}(\text{RES})$	RESET SCHMITT V_{IH}	2.0		V	

NOTE1: -INIT, -AFD, -STB, AND -SLIN ARE OPEN COLLECTOR OUTPUT PINS THAT EACH HAVE AN INTERNAL PULL-UP RESISTOR ($2.5\text{k}\Omega$ - $3.5\text{k}\Omega$) TO V_{CC} . THIS WILL GENERATE A MAXIMUM OF 2.0mA INTERNAL I_{OL} . IN ADDITION TO THIS INTERNAL CURRENT, EACH PIN WILL SINK AT LEAST 10mA, WHILE MAINTAINING THE V_{OL} SPECIFICATION OF 0.4V MAX.

GM3054 / 3057

SERIAL INTERFACE CMOS CODEC/FILTER

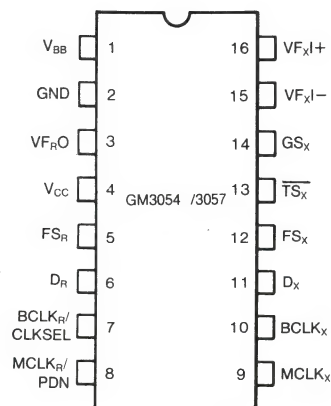
Description

The GM3054, GM3057 family consists of μ -law and A-law monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in Figure 1, and a serial PCM interface. The devices are fabricated using GoldStar's advanced double Polysilicon Gate CMOS process.

The transmit portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are autozero circuitry and a compressing coder which samples the filtered signal and encodes it in the compressed μ -law or A-law PCM format. The receive portion of each device consists of an expanding decoder, which reconstructs the analog signal from the compressed μ -law or A-law code, a low-pass filter which corrects for the $\sin x/x$ response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks, which may vary from 64 KHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Pin Configuration

(Top View)



Features

- **Complete Codec and Filtering System Including:**
 - Transmit High-Pass and Low-Pass Filtering
 - Receive Low-Pass Filter With $\sin x/x$ Correction
 - Active RC Noise Filter
 - μ -Law or A-Law Compatible Coder and Decoder
 - Internal Precision Voltage Reference
 - Serial I/O Interface
 - Internal Auto-Zero Circuitry
- **μ -Law, 16 Pin—GM3054 (PDIP · CERDIP)**
- **A-Law, 16 Pin—GM3057 (PDIP · CERDIP)**
- **Meets or Exceeds All D3/D4 and CCITT Specifications**
- **$\pm 5.0V$ Operation**
- **Low Operating Power—Typically 60 mW**
- **Power-Down Standby Mode—Typically 3.0 mW**
- **Automatic Power-Down**
- **TTL or CMOS Compatible Digital Interfaces**
- **Maximizes Line Interface Card Circuit Density**

Block Diagram

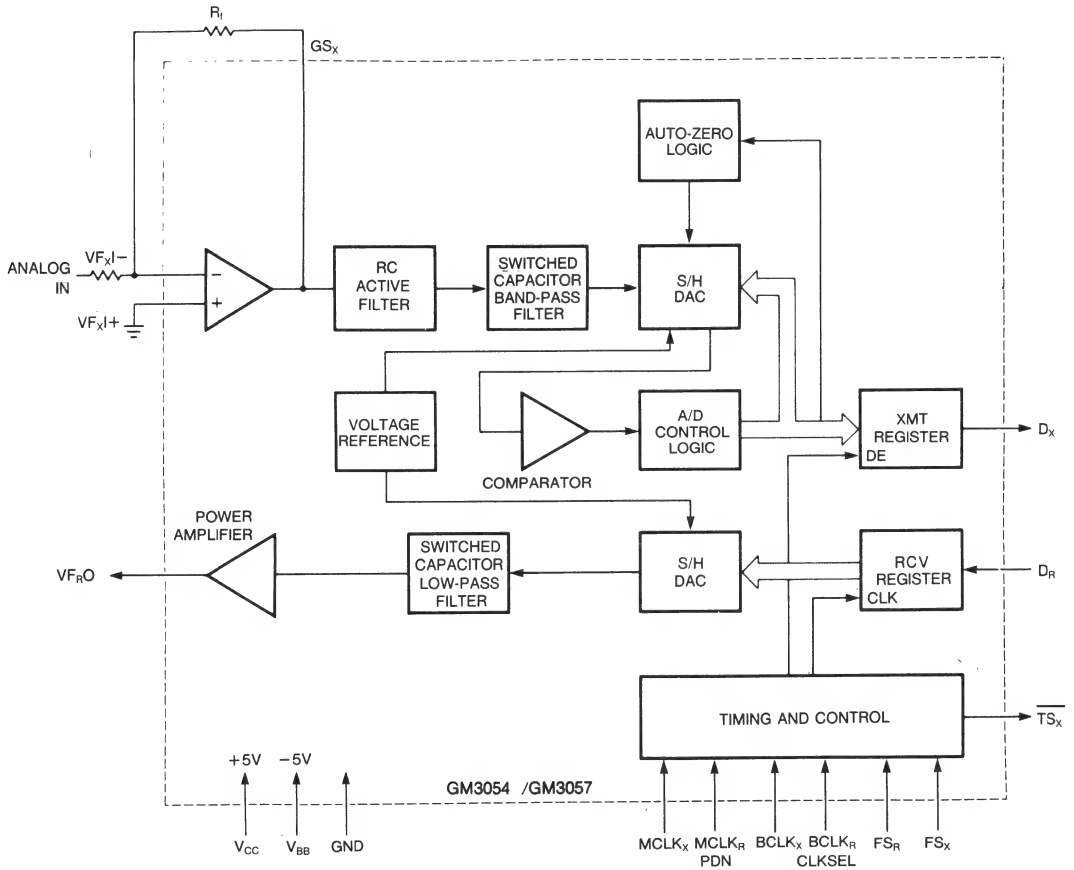


Figure 1

Pin Description

Pin NO.	Name	Function
1	V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$
2	GND	Ground. All signals are referenced to this pin.
3	V_{FRO}	Analog output of the receive filter.
4	V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
5	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R . FS_R is an 8 KHz pulse train. See Figures 2 and 3 for timing details.
6	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R/CLKSEL$	The bit clock which shifts data into D_R after FS_R leading edge. May vary from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_R$. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (See Table 1).
8	$MCLK_R/PDN$	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
9	$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
10	$BCLK_X$	The bit clock which shifts out the PCM data on D_X . May vary from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
11	D_X	The 3-State PCM data output which is enabled by FS_X .
12	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X . FS_X is an 8 KHz pulse train; see Figures 2 and 3 for timing details.
13	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
15	$VF_X -$	Inverting input of the transmit input amplifier.
16	$VF_X +$	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the device and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and V_{FRO} outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R/PDN$ pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R/PDN$ pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The 3-State PCM data output, D_X , will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R/PDN$ pin can be used as a power-down control. A low level on $MCLK_R/PDN$ powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R/CLKSEL$ can be also be applied to $BCLK_X$ and the $BCLK_R/CLKSEL$ can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

Functional Description (Continued)

With a fixed level on the BCLK_R/CLKSEL pin, BCLK_X will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of BCLK_R CLKSEL. In this synchronous mode, the bit clock, BCLK_X, may be from 64 KHz to 2.048 MHz, but must be synchronous with MCLK_X.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of BCLK_X. After 8 bit clock periods, the 3-State D_X output is returned to a high impedance state. with an FS_R pulse, PCM data is latched via the D_R input on the negative edge of BCLK_X (or BCLK_R if running). FS_X and FS_R must be synchronous with MCLK_{X/R}.

Table I. Selection Of Master Clock Frequencies

BCLK _R /CLKSEL	Master Clock Frequency Selected	
	GM3057	GM3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. MCLK_X and MCLK_R must be 2.048 MHz for the GM3057, and 1.536 MHz or 1.544 MHz for the GM3054 and need not be synchronous. For best transmission performance, however, MCLK_R should be synchronous with MCLK_X, which is easily achieved by applying only static logic levels to the MCLK_R/PDN pin. This will automatically connect MCLK_X to all internal MCLK_R functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with MCLK_X and BCLK_X. FSR starts each decoding cycle and must be synchronous with BCLK_R which must be a clock. The logic levels shown in Table 1 are not valid for asynchronous operation. BCLK_X and BCLK_R may operate from 64 KHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both

frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in Figure 2. With FS_X high during a falling edge of BCLK_X the next rising edge of BCLK_X enables the D_X 3-State output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of BCLK_R (BCLK_X in synchronous mode), the next falling edge of BCLK_R latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

The use the long frame sync mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in Figure 3. Based on the transmit frame sync, FS_X, the device will sense whether short or long frame sync pulses are being used. For 64 KHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of BCLK_X, whichever comes later, and the first bit clocked out is the sign bit. The following seven BCLK_X rising edges clock out the remaining seven bits. The D_X output is disabled by the falling BCLK_X edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edge of BCLK_R (BCLK_X in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see Figure 4. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 KHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of compressing type according to μ -law (GM3054) or A-law (GM3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) or nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μ s (due to the transmit filter) plus 125 μ s (due to encoding delay), which total 290 μ s. Any

offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive station consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 KHz. The decoder is A-law (GM3057) or μ -law (GM3054A) and the 5th order low pass filter corrects for sin x/x attenuation due to the 8 KHz sample/hold. The filter

is then followed by a power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight BCLK_R (BCLK_X) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μ s later the decoder DAC output is updated. The total decoder delay is 10 μ s (decoder update) plus 110 μ s (filter delay) plus 62.5 μ s d(1/2 frame), which gives approxiamtely 180 μ s.

Absolute Maximum Ratings

V_{CC} to GND 7V
V_{SS} to GND -7V
Voltage at any Analog Input or Output V_{CC}+0.3V to V_{SS}-0.3V

Voltage at any Digital Input or Output V_{CC}+0.3V to GND -0.3V
Operating Temperature Range -25°C to +125°C
Storage Temperature Range -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) 300°C

Electrical Characteristics

Unless otherwise noted: V_{CC}=5.0V \pm 5%, V_{BB}=-5V \pm 5%, GND=0V, T_A=0°C to 70°C; typical characteristics specified at V_{CC}=5.0V, V_{BB}=-5.0V, T_A=25°C; all signals are referenced to GND.

Operating Current

I _{CC0}	Power-Down Current			0.5	1.5	mA
I _{BB0}	Power-Down Current			0.05	0.3	mA
I _{CC1}	Active Current			6.0	9.0	mA
I _{BB1}	Active Current			6.0	9.0	mA

Digital Interface

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	$D_X, I_L = -3.2\text{mA}$ $\overline{TS}_X, I_L = 3.2\text{mA}, \text{Open Drain}$			0.4 0.4	V V
V_{OH}	Output High Voltage	$D_X, I_H = -3.2\text{mA}$	2.4			V
I_{IL}	Input Low Current	$GND \leq V_{IN} \leq V_{IL}$, All Digital Inputs	-10		10	μA
I_{IH}	Input High Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	-10		10	μA
I_{OZ}	Output Current in High Impedance State	$D_X, GND \leq V_O \leq V_{CC}$	-10		10	μA

Analog Interface With Transmit Input Amplifier

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IXA}	Input Leakage Current	$-2.5\text{V} \leq V \leq +2.5\text{V}$, $VF_X I^+$ or $VF_X I^-$	-200		200	nA
R_{IXA}	Input Resistance	$-2.5\text{V} \leq V \leq +2.5\text{V}$, $VF_X I^+$ or $VF_X I^-$	10			$\text{M}\Omega$
R_{OXA}	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_{LXA}	Load Resistance	GS_X	10			$\text{K}\Omega$
C_{LXA}	Load Capacitance	GS_X			50	pF
V_{OXA}	Output Dynamic Range	$GS_X, R_L \leq 10\text{K}\Omega$	± 2.8			V
A_{VXA}	Voltage Gain	$VF_X I^+$ to GS_X	5000			V/V
F_{UXA}	Unity Gain Bandwidth		1	2		MHz
V_{OSXA}	Offset Voltage		-20		20	mV
V_{CMXA}	Common-Mode Voltage		-2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB

Analog Interface With Receive Output

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R_{ORF}	Output Resistance	Pin VF_{RO}		1	3	Ω
R_{LRF}	Load Resistance	$VF_{RO} = \pm 2.5\text{V}$	600			Ω
C_{LRF}	Load Capacitance				500	pF
V_{OSRO}	Output DC Offset Voltage		-200		200	mV

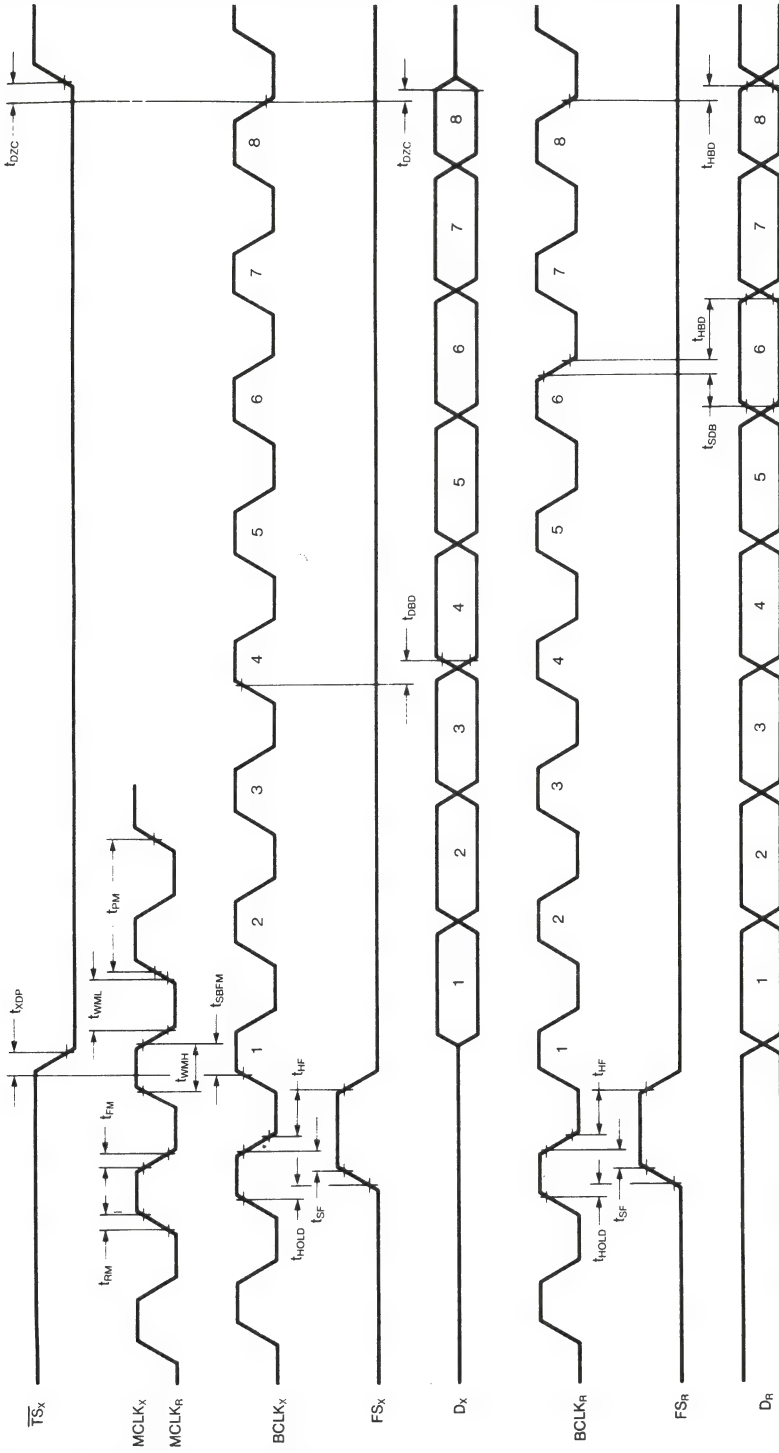
Timing Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the BCLK _R /CLKSEL Pin		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	MCLK _X and MCLK _R	160			ns
t_{WML}	Width of Master Clock Low	MCLK _X and MCLK _R	160			ns
t_{RM}	Rise Time of Master Clock	MCLK _X and MCLK _R			50	ns
t_{FM}	Fall Time of Master Clock	MCLK _X and MCLK _R			50	ns
t_{SBFM}	Set-Up Time from BCLK _X High (and FS _X in Long Frame Sync Mode) to MCLK _X Falling Edge	First Bit Clock after the Leading Edge of FS _X	100			ns
t_{PB}	Period of Bit Clock		485	488	15,725	ns
t_{WBH}	Width of Bit Clock High	V _{IH} =2.2V	160			ns
t_{WBL}	Width of Bit Clock Low	V _{IL} =0.6V	160			ns
t_{RB}	Rise Time of Bit Clock	t _{PS} =488 ns			50	ns
t_{FB}	Fall Time of Bit Clock	t _{PB} =488 ns			50	ns
t_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Bit clock High to Frame Sync	Short Frame Only	0			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from BCLK _X High to Data Valid	Load=150 pF plus 2 LSTTL Loads	0		180	ns
t_{XDP}	Delay Time to TS _X Low	Load=150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from BCLK _X Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS _X or BCLK _X , Whichever Comes Later	C _L =0 pF to 150 pF	20		165	ns
t_{SDB}	Set-Up Time from D _R Valid to BCLK _{R/X} Low		50			ns
t_{HBD}	Hold Time from BCLK _{R/X} Low to D _R Invalid		50			ns
t_{SF}	Set-Up time from FS _{X/R} to BCLK _{X/R} Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50			ns
t_{HF}	Hold Time from BCLK _{X/R} Low to FS _{X/R}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100			ns
t_{HBF1}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS _X or FS _R)	Long Frame Sync Pulse (from 3 to 8 Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	160			ns

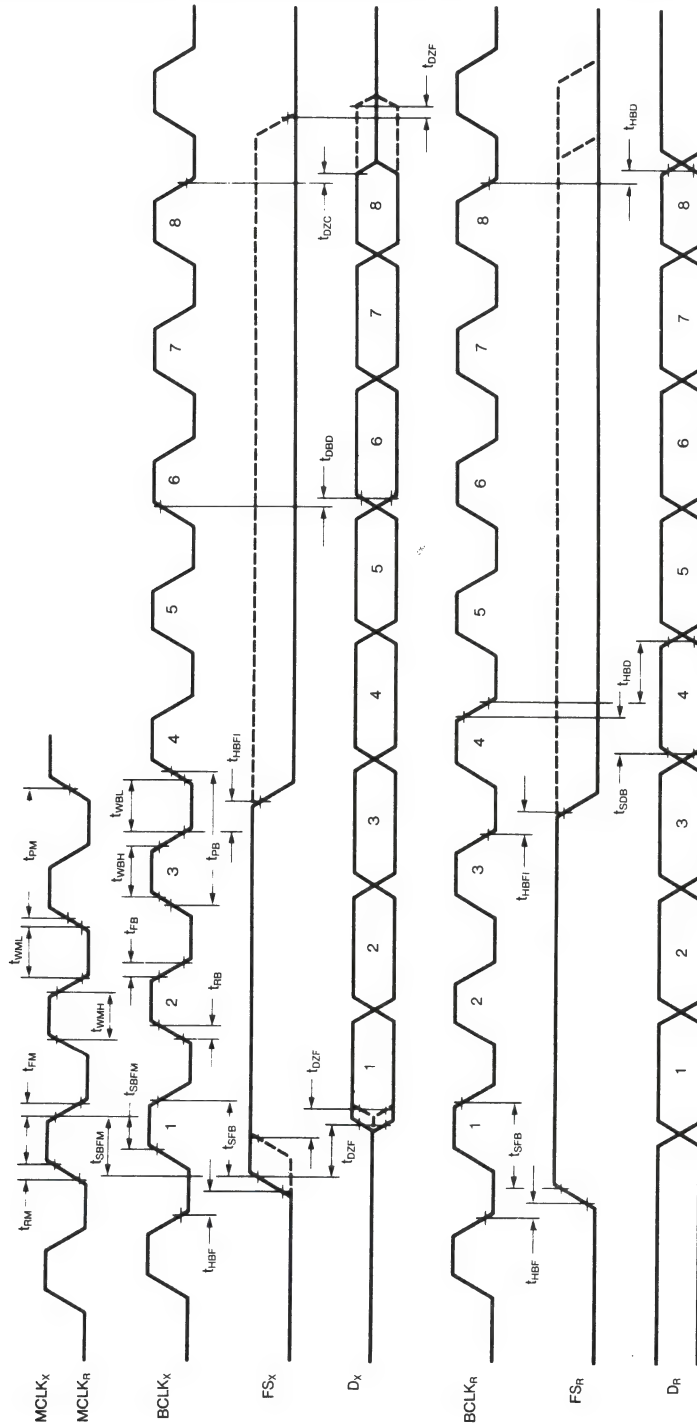
Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

Timing Diagrams

Figure 2. Short Frame Sync Timing



Timing Diagrams (Continued)
Figure 3. Long Frame Sync Timing



Transmission Characteristics

Unless otherwise specified: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $GND = 0V$, $f = 1.02\text{ KHz}$, $V_{IN} = 0\text{ dBm}$, transmit input amplifier connected for unity-gain non-inverting.

Amplitude Response

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{MAX}	Absolute Levels	Nominal 0 dBm0 Level is 4dBm (600 Ω)				
		0 dBm0				
		GM3054A		1.2276		Vrms
		GM3057		1.2276		Vrms
G_{XA}	Transmit Gain, Absolute	Max Overload Level				
		GM3054A (3.17 dBm0)		2.501		V _{PK}
G_{XR}	Transmit Gain, Relative to G_{XA}	GM3057 (3.14 dBm0)		2.492		V _{PK}
		$T_A = 25^\circ\text{C}$, $V_{CC} = 5V$, $V_{BB} = -5V$	-0.15		0.15	dB
		Input at $GS_X = 0\text{ dBm0}$ at 1020 Hz				
		$f = 16\text{ Hz}$			-40	dB
		$f = 50\text{ Hz}$			-30	dB
		$f = 60\text{ Hz}$			-26	dB
		$f = 200\text{ Hz}$	-1.8		-0.1	dB
		$f = 300\text{ Hz}$ -3000 Hz	-0.15		0.15	dB
		$f = 3300\text{ Hz}$	0.35		0.05	dB
		$f = 3400\text{ Hz}$	-0.7		0	dB
		$f = 4000\text{ Hz}$			-14	dB
		$f = 4600\text{ Hz}$ and Up, Measure Response from 0 Hz to 4000 Hz			-32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T_A = 0^\circ\text{C}$ to 70°C			± 0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			± 0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test method				
		Reference Level = -10 dBm0				
		$VF_{XL} = -40\text{ dBm0}$ to $+3\text{ dBm0}$	-0.2		0.2	dB
		$VF_{XL} = -50\text{ dBm0}$ to -40 dBm0	-0.4		0.4	dB
G_{RA}	Receive Gain, Absolute	$VF_{XL} = -55\text{ dBm0}$ to -50 dBm0	-1.2		1.2	dB
		$T_A = 25^\circ\text{C}$, $V_{CC} = 5V$, $V_{BB} = -5V$	-0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz				
		$f = 0\text{ Hz}$ to 3000 Hz	-0.15		0.15	dB
		$f = 3300\text{ Hz}$	-0.35		0.05	dB
		$f = 3400\text{ Hz}$	-0.7		0	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$f = 4000\text{ Hz}$			-14	dB
		$T_A = 0^\circ\text{C}$ to 70°C			± 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			± 0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference				
		Input PCM Code Corresponds to an Ideally Encoded -10 dBm0 Signal				
		PCM Level = -40 dBm0 to $+3\text{ dBm0}$	-0.2		0.2	dB
		PCM Level = -50 dBm0 to -40 dBm0	-0.4		0.4	dB
V_{RO}	Receive Output Drive Level	PCM Level = -55 dBm0 to -50 dBm0	-1.2		1.2	dB
		$R_L = 600\Omega$	-2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise specified: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $GND = 0V$, $f = 1.02\text{ KHz}$, $V_{IN} = 0\text{ dBm}$, transmit input amplifier connected for unity-gain noninverting.

Envelope Delay Distortion With Frequency

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
D_{XA}	Transmit Delay, Absolute	$f = 1600\text{ Hz}$		290	315	μS
D_{XR}	Transmit Delay, Relative to D_{XA}	$f = 500\text{ Hz}-600\text{ Hz}$		195	220	μS
		$f = 600\text{ Hz}-800\text{ Hz}$		120	145	μS
		$f = 800\text{ Hz}-1000\text{ Hz}$		50	75	μS
		$f = 1000\text{ Hz}-1600\text{ Hz}$		20	40	μS
		$f = 1600\text{ Hz}-2600\text{ Hz}$		55	75	μS
		$f = 2600\text{ Hz}-2800\text{ Hz}$		80	105	μS
		$f = 2800\text{ Hz}-3000\text{ Hz}$		130	155	μS
D_{RA}	Receive Delay, Absolute	$f = 1600\text{ Hz}$		180	200	μS
D_{RR}	Receive Delay, Relative to D_{RA}	$f = 500\text{ Hz}-1000\text{ Hz}$	-40	-25		μS
		$f = 1000\text{ Hz}-1600\text{ Hz}$	-30	-20		μS
		$f = 1600\text{ Hz}-2600\text{ Hz}$		70	90	μS
		$f = 2600\text{ Hz}-2800\text{ Hz}$		100	125	μS
		$f = 2800\text{ Hz}-3000\text{ Hz}$		145	175	μS

Noise

N_{XC}	Transmit Noise, C Message Weighted	GM3054A $VF_X I^* = 0$		12	15	dBmC0
N_{XP}	Transmit Noise, P Message Weighted	GM3057 $VF_X I^* = 0V$		-74	-69	dBmOp
N_{RC}	Receive Noise, C Message Weighted	GM3054A PCM Code Equals Alternating Positive and Negative Zero		8	11	dBmC0
N_{RP}	Receive Noise, P Message Weighted	GM3057 PCM Code Equals Positive Zero		-82	-79	dBmOp
N_{RS}	Noise, Single Frequency	$f = 0\text{ KHz}$ to 100 KHz , Loop Around Measurement, $VF_X I^* = 0 V_{rms}$			-53	dBmO
$PPSR_X$	Positive Power Supply Rejection, Transmit	$VF_X I^* = 0 V_{rms}$ $V_{CC} = 5.0 V_{DC} + 100\text{ mVrms}$ $f = 0\text{ KHz}-50\text{ KHz}$	40			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	$VF_X I^* = 0 V_{rms}$ $V_{BB} = -5.0V V_{DC} + 100\text{ mVrms}$ $f = 0\text{ KHz}-50\text{ KHz}$	40			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{CC} = 5.0 V_{DC} + 100\text{ mVrms}$ $f = 0\text{ Hz}-4000\text{ Hz}$ $f = 4\text{ KHz}-25\text{ KHz}$ $f = 25\text{ KHz}-50\text{ KHz}$	40 40 36			dBC dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{BB} = -5.0 V_{DC} + 100\text{ mVrms}$ $f = 0\text{ Hz}-4000\text{ Hz}$ $f = 4\text{ KHz}-25\text{ KHz}$ $f = 25\text{ KHz}-50\text{ KHz}$	40 40 36			dBC dB dB

Transmission Characteristics (Continued)

Unless otherwise specified: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $GND = 0V$, $f = 1.02\text{ KHz}$, $V_{IN} = 0\text{ dBm0}$, transmit input amplifier connected for unity-gain noninverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SOS	Spurious Out-of Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz-3400 Hz Input Applied to VF_XI^* , Measure Individual Image Signals at VF_{RO} 4600 Hz-7600 Hz 7600 Hz-8400 Hz 8400 Hz-100,000 Hz			-32 -40 -32	dB dB dB

Distortion

STD _X STD _R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method Level = 3.0 dBm0 = 0 dBm0 to -30 dBm0 = -40 dBm0 XMT RCV = -55 dBm0 XMT RCV	33 36 29 30 14 15			.dBC dBC dBC dBC dBC dBC
SFD _X	Single Frequency Distortion, Transmit				-46	dB
SFD _R	Single Frequency Distortion, Receive				-46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, $VF_X^* = -4\text{ dBm0}$ to -21 dBm0 , Two Frequencies in the Range 300 Hz-3400 Hz			-41	dB

Crosstalk

CT _{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	$f = 300\text{ Hz}-3400\text{ Hz}$ $D_R = \text{Steady PCM Code}$		-90	-75	dB
CT _{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	$f = 300\text{ Hz}-3400\text{ Hz}$, $VF_XI = 0V$		-90	-70 (Note 2)	dB

Note 1: Measured by extrapolation from the distortion test result.

Note 2: CT_{R-X} is measured with a -40dBm0 activating signal applied at $VF_XI = 0V$

Encoding Format At D_x

	GM3054A μ -Law	GM3057 A-Law (Includes Even Bit Inversion)
V_{IN} (at GS_X) = +Full-Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} (at GS_X) = 0V	<div style="display: flex; align-items: center;"> <div style="font-size: 2em; margin-right: 5px;">{</div> <div> 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 </div> </div>	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} (at GS_X) = -Full-Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

Application Information

POWER SUPPLIES

While the pins of the GM3054A family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

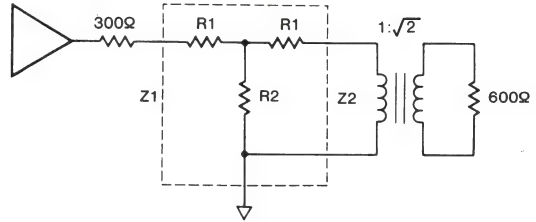
All ground connections to each device should meet at a common point as close as possible to the GND pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μ F supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} .

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μ F capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a GM3054A family CODEC/FILTER receive output must drive a 600 Ω load, but a peak swing lower than ± 2.5 V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π -pad at the output. Table II lists the required resistor values for 600 Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600 Ω is obtained if the output impedance of the attenuator is in the range 282 Ω to 319 Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1 \left(\frac{N^2 + 1}{N^2 - 1} \right) - 2 \sqrt{Z1, Z2} \left(\frac{N}{N^2 - 1} \right)$$

$$R2 = 2 \sqrt{Z1, Z2} \left(\frac{N}{N^2 - 1} \right)$$

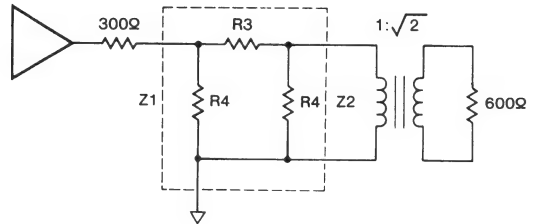
$$\text{Where } N = \sqrt{\frac{\text{Power In}}{\text{Power Out}}}$$

$$\text{and } S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{sc} \cdot Z_{oc}}$$

Where Z_{sc} = Impedance with short circuit termination
and Z_{oc} = Impedance with open circuit termination

π -Pad Attenuator



$$R3 = \sqrt{\frac{Z1, Z2}{2}} \left(\frac{N^2 - 1}{N} \right)$$

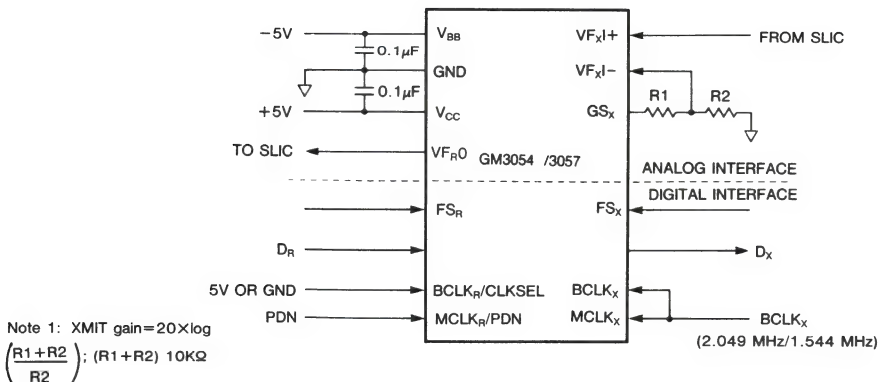
$$R3 = Z1 \left(\frac{N^2 - 1}{N^2 - 2NS + 1} \right)$$

Applications Information (Continued)

Table II. Attenuator Tables For $Z_1=Z_2=300\Omega$ (All Values In Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	6.7k	10.4	17.4k
0.4	6.9	6.5k	18.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.2	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	616	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



GM6388

15 MEMORY TONE/PULSE SWITCHABLE DIALER

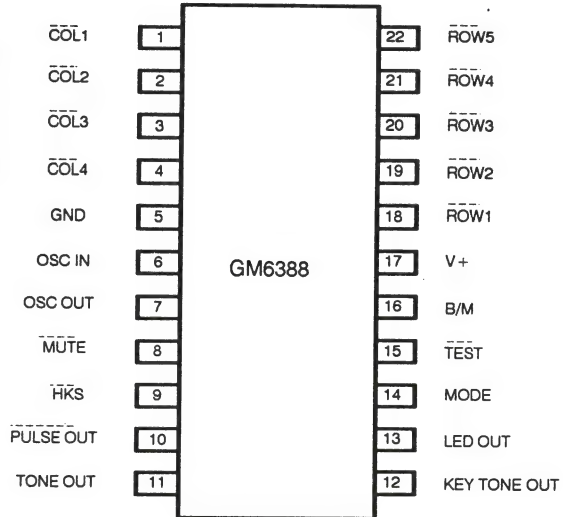
DESCRIPTION

The GM6388 is a monolithic integrated circuit which performs 15-Memory Tone/Pulse switchable dialing functions for modern telephone set design. It is fabricated in CMOS technology, thus has good performance in low voltage, low power operations. Four 16-digits direct dialing memories are added for convenient emergency calls (such as fire, police, doctor) and Long Distance Service Company (such as MCI, SPRINT) access codes operations. Wide operating voltage range and low memory retention current facilitate this chip excellent for battery-free direct line powered operation.

FEATURES

- DTMF/Pulse Switchable Dialer
- Stores Ten 16-Digits Numbers for Repertory Dialing
- Additional Four 16-Digits Numbers for Emergency Calling and Long Distance Service Company Access code Memory
- One 31-Digits for Last Number Redial Memory.
- Auto Pause Access for PBX and Toll Service Operations : 3.1 sec. per pause
- Easy Operation with Redial, Store, Auto & Pause Keypads
- Key-Tone Output for valid keypad Entry recognition
- Uses Form A Keyboard or the Standard 2-of-9 Matrix Keyboard
- Electronic Keypad Input is Available; low Action
- Uses Inexpensive 3,579545 MHz Television Color-Burst Crystal
- Pin Selectable for Break/Make Ratio
- Memory Retention Current <0.6uA
- Wide operation voltage range; 2.5V ~ 5.5V
- Automatic switching from PULSE mode to TONE mode in Long Distance memory
- 22-pin Dual-in-Line Package

PIN CONFIGURATION



KEYBOARD FUNCTION

COL1	COL2	COL3	COL4	
1	2	3	EM1	ROW1
4	5	6	EM2	ROW2
7	8	9	EM3	ROW3
*	0	#	LDC	ROW4
R	S	A	P	ROW5

R : Redial
 S : Store
 A : Auto Dialing
 P : Pause
 EM1-EM3 : Emergency 1-3
 LDC : Long Distance Company

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V^+	6.0 Volts
Any Input Relative to V^+	+ 0.5 Volts
Any Input Relative to V^-	- 0.5 Volts
Operating Temperature	- 40°C to + 85°C
Storage Temperature	- 65°C to + 150°C
Power Dissipation Per Package	500 (for $T_A = -40^\circ\text{C}$ to + 60°C) mA

ELECTRICAL CHARACTERISTICS

DC Characteristics ($V^+ = 2.5\text{V}$, $T_A = 25^\circ\text{C}$, Unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT	NOTES
Operating Voltage	V^+	Tone	2.0	-	5.5	V	
		Pulse	2.0	-	5.5		
		Memory	1.0	-	5.5		
Operating Current	I_{op}	Tone	-	0.6	2	mA	1,4,6
		Pulse	-	0.2	0.5		
Memory Retention Current	IMR	HKS = 1 $T_A = 45^\circ\text{C}$ $V^+ = 1.0\text{V}$	-	0.1	0.2	μA	
Standby Current	I_s		-	0.1	5	μA	1,2,3,5,6
Tone Output Voltage	V_{TO}	Row Group $R_L = 10\text{k}\Omega$	130	150	170	mVrms	
Pre - Emphasis		Column Group / Row Group	-	-	3	dB	
DTMF Distortion	THD	$R_L = 10\text{k}\Omega$		-30	-23	dB	7, 8
Tone Output External Load Impedance	R_L	THD < 20dB	10	-	-	$\text{k}\Omega$	
Tone Output DC Level	V_{DC}	$V^+ = 2.5\text{--}5.5\text{V}$	0.5V^+	-	0.6V^+	-	
Tone Output Sink Current	I_{TL}	$V_{TO} = 0.5\text{V}$	0.2	-	-	mA	
Pulse Output Drive Current	I_{PH}	$V_{PO} = 2.0\text{V}$	-0.2	-	-	mA	

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT	NOTES
Sink Current	I_{PL}	$V_{PO} = 0.5V$	0.2			mA	
Mute Output Drive Current	I_{MH}	$V_{MO} = 2.0V$	-0.2			mA	
Sink Current	I_{ML}	$V_{MO} = 0.5V$	2			mA	
Key Tone Output Drive Current	I_{KH}	$V_{KO} = 2.0V$	-0.5			mA	
Sink Current	I_{KL}	$V_{KO} = 0.5V$	0.5			mA	
LED Output Drive Current	I_{LH}	$V_{LO} = 2.0V$	-0.2			mA	
Sink Current	I_{LL}	$V_{LO} = 0.5V$	0.2			mA	

NOTES :

1. HKS = 0
2. In DTMF Mode
3. In Pulse Mode
4. Keyboard Entry, Including Auto Dialing
5. No Keyboard Entry
6. All Output Unloaded
7. Dual Tone Multi-Frequency Distortion is measured in terms of total Out-of-band power related to sum of row & column fundamental power.
8. Crystal parameters defined as $R_S < 100\Omega$, $L_m = 96mH$, $C_m = 0.25pF$, $C_h = 5pF$, $F = 3.5795MHz$ & $C_L = 18pF$

(II)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT	NOTES
Key-In Debounce	t_{KD}	Test = 1		20		ms	1, 2, 3
Pulse mute delay	t_{MD}	Test = 1 $\frac{B/M=1}{B/M=0}$		40		ms	2
				33.3			1.2
Pre-digit Pause	t_{PDP}	Test = 1 $\frac{B/M=1}{B/M=0}$		40		ms	
				33.3			1.2
Pulse Rate	f_{PR}	Test = 1 Test = 0		10		pps	1
				600			
Inter Digit Pause	t_{IDP}	Test = 1 Test = 0		800		ms	
				13.3			
Break/Make Ratio	B:M	$\frac{B/M=1}{B/M=0}$		60:40		%	1
				66.6:33.3			
Tone Duration	t_{TD}	Auto Dialing	100			ms	1
Inter Tone Pause	t_{ITP}	Auto Dialing		105		ms	1
Row Group Frequency	f_1	Row 1		699		Hz	1
	f_2	Row 2		766			
	f_3	Row 3		848			
	f_4	Row 4		948			
Column Group Frequency	f_5	col 1		1216		Hz	1
	f_6	col 2		1332			
	f_7	col 3		1472			
Key Tone Frequency	f_K			1.2		kHz	1
Input Voltage Low	V_{IL}	Pins : 1, 2, 3, 4, 9, 14,	GND		0.3V ⁺		
Input Voltage High	V_{IH}	15, 17, 18, 19, 20, 21, 22	0.7V ⁺		V ⁺		
Keypad Input Drive Current	I_{KD}	$V_I = 0V$	4	10	30	μA	
Sink Current	I_{KS}	$V_I = 2.5V$	200	400		μA	
Control Pin Input Leakage Current	I_{IN}	Pins : 9, 14, 15, 17		$\pm 10^{-5}$	± 0.1	μA	

NOTES : 1. Crystal parameters defined as $R_s < 100\Omega$, $L_m = 96mH$, $C_m = 0.25pF$, $C_h = 5pF$, $F = 3.579545MHz$ & $C_L = 18pF$

2. Refer to Pulse Mode Time Diagram

3. Refer to DTMF Mode Time Diagram

FUNCTIONAL DESCRIPTION

ROW - COLUMN INPUTS (Pins 1-4 & 18-22)

The keypads input is compatible with the standard 2-of-9 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic input. Figure 1 shows how to connect to the two keyboard types and Figure 2 shows wave forms for electronic inputs. In normal operation any single button is pushed to produce dual tone, pulses or function. Activation of two or more buttons will result in no response, except for single tone. TABLE I illustrates the address keypads function, in detail.

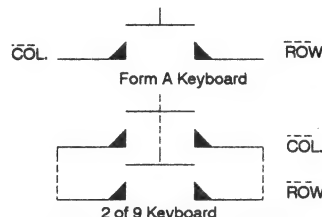
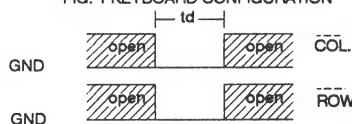


FIG. 1 KEYBOARD CONFIGURATION



td is min. tone duration plus keypad debounce time

FIG. 2 ELECTRONIC INPUT

TABLE I: ADDRESS KEYPADS TRUTH TABLE

OUTPUT		ACTIVE LOW INPUTS		OUTPUT
		ROW (Pin 18~22)	COLUMN (Pin 1~3)	TONE (Pin 11) PULSE (Pin 10)
TONE (Pin 14=0)	Normal (Pin 15=1)	One Two or More One Two or More	One One Two or More Two or More	Dual Tone Pin 11=0 Pin 11=0 Pin 11=0
	Single Tone (Pin 15=0)	One Two or More One Two or More	One One Two or More Two or More	Dual Tone Column Tone Row Tone Pin 11=0
PULSE (Pin 14=1)	10 pps (Pin 15=1)	One Two or More One Two or More	One One Two or More Two or More	10 pps Pin 10=1 Pin 10=1 Pin 10=1
	600 pps (Pin 15=0)	One Two or More One Two or More	One One Two or More Two or More	600 pps Pin 10=1 Pin 10=1 Pin 10=1

Note 1 : In pulse mode, Pin 10=1 for * & # buttons

Note 2 : In pulse mode, always Pin 11=0, In DTMF mode, always Pin 10=1

Note 3 : Pin 10=1, Pin 11=0 for any button in Row5 & Column4, regardless of mode.

* OSC. IN (Pin 6), OSC. OUT (Pin 7)

A built-in inverter provides oscillation with an inexpensive 2.579545MHz television color-burst crystal. The oscillator ceases when a keypad input is not sensed. An on-board counter is used to decrease the frequency of oscillator, and creates keypad debounce, mute delay, pre-digit pause, pulse rate, inter rate, inter digit pause, Break/Make ratio, inter-tone Pause, tone duration, row group & column group frequency, & key tone frequency etc. Any crystal frequency deviation from 3.579545MHz will be reflected in the time parameter above. Most crystals do not vary more than +0.02%.

* MUTE (Pin 8)

The mute output is a conventional CMOS inverter that pulls to V⁺ with no Keyboard input and pulls to GND when an address keypads entry is sensed (excluding the * & # Keypads, in pulse mode), that is, and keypad in row 5 & column 4 is pushed, then mute out keeps high level still. The mute output is used to cut out the current biased in type-2500 telephone circuit or GM6388, that is required to actuate on address keypads input.

* TONE OUT (PIN 11)

In pulse mode, the tone output keeps low state regardless of keypads input. In DTMF mode, the pin outputs dual tone or single tone, referred to TABLE I.

The tone duration equals to the period of button pushed minus the keypad debounce time in manual dialing. The tone duration and inter-tone-pause are internal set to be 100ms and 105ms respectively in auto dialing.

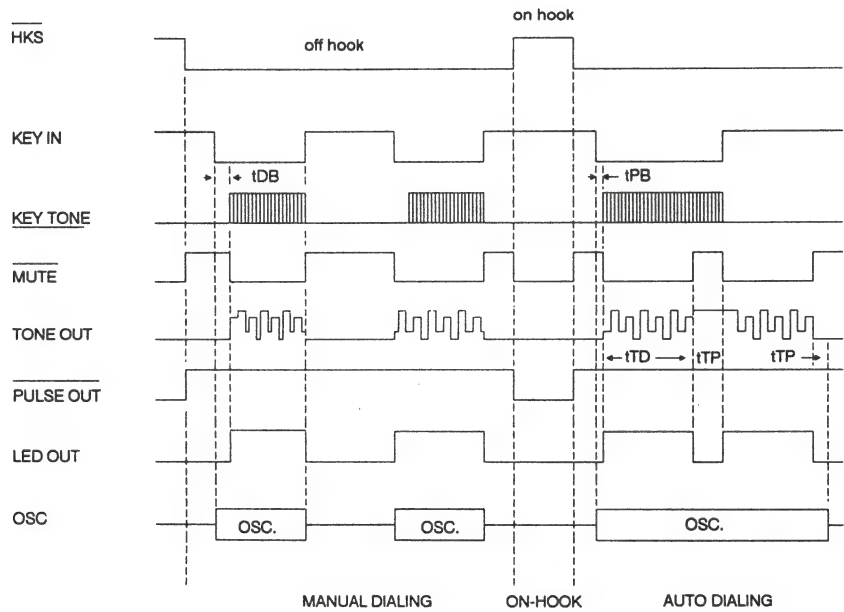


FIG. 3-1 TIME DIAGRAM (TONE MODE)

*** HKS (Pin 9)**

The HKS (Hook Switch) input is used to sense the state of handset in ON-HOOK or OFF-HOOK. In ON-HOOK state, HKS = 1, the keyboard input is disabled, there is not any operation for any keyboard entry, to avoid the energy lose stored in capacitor. In OFF-HOOK state, HKS = 0, all of the function work.

*** PULSE OUT (Pin 10)**

In DTMF mode, the pulse out keeps high level regardless of keyboard entry. In pulse mode, this output sends a chain of pulses to correspond the address keypad input, but keeps high level for * & # entry. Figure 3-2 shows the time diagram in pulse mode. The pulse rate and inter digit pause are fixed, in normal condition Pin 15 = 1, to be 10 pps and 800ms respectively. The Break/Make ratio is pin selectable depends on the state of B/M Pin. It is 60:40 for B/M = 1, and 66.6:33.3 for B/M = 0.

*** KEY TONE OUT (Pin 12)**

The key tone output is a conventional CMOS inverter. A NPN transistor is needed to drive a piezo. The output frequency is 1.2KHz. In spite of DTMF or Pulse mode, the key tone actuate, after any keypad (including row 5 and column 4) entry has been detected, and ceases at the time of button released. There is not key tone output, whenever two or more keyboard button are pushed simultaneously.

*** LED OUT (Pin 13)**

The LED OUT is a conventional CMOS inverter. A NPN transistor is used to turn off LED. In DTMF mode, the output actuates in the duration of DTMF signal is sending. But the output always keeps low in pulse mode. With the exception of controlling LED for indication, it can be used for muting operation in Tone mode also.

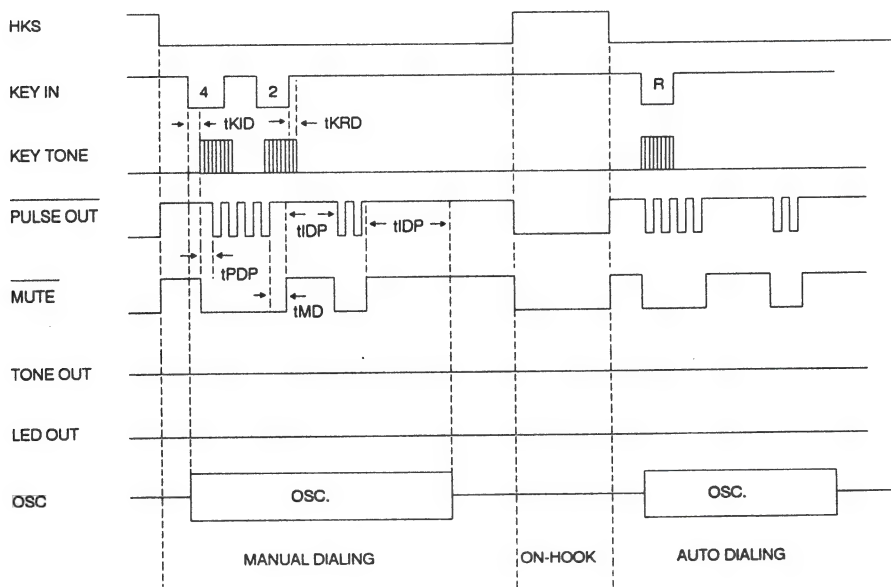


FIG. 3-2 PULSE MODE TIME DIAGRAM

GM6388

* MODE (Pin 14)

Pulls pin 14 to V⁺, the dialer is in pulse mode.

On the contrary, it is in DTMF mode.

* TEST (Pin 15)

In normal operation, ties the TEST Pin to V⁺, the single tone is inhibited & pulse rate is 10pps. In testing operation, ties the TEST pin to GND, single tone can be created with the method shown in TABLE I, and all of the time parameter in pulse dialing is faster by 60 times.

* B/M (Pin 16)

The Break/Make ratio is 60:40, if B/M = 1, and is 66.6:33.3 if B/M=0. This pin influences nothing in DTMF mode.

KEYBOARD OPERATIONS

Note : All the keyboard operations should be under OFF-HOOK condition.

I. NORMAL DIALING

Select Pulse or Tone mode.

Push **[D1]** , **[D2]** **[Dn]**
D1 ~ Dn : 0 ~ 9, *, #

Then the number D1, D2,Dn will be dialed out in Pulse or Tone mode as selected.

II. REDIALING

Select Pulse or Tone mode.

Push **[D1]** , **[D2]** Dn, busy, ON-HOOK.
Come OFF-HOOK, push **[REDIAL]** , the last number D1, D2 Dn will be automatically dialed out in pulse or Tone mode as selected.

III. NUMBER STORING

Don't care Pulse or Tone mode

Push **[S]** **[D2]** , **[D2]** **[Dn]** , **[S]** , **[Ln]**
Ln : 0 ~ 9

then the number D1, D2 Dn will be stored in location **[Ln]**

IV. MEMORY DIALING

Select Pulse or Tone mode.

Push **[A]** , **[Ln]** , then the number stored in location **[Ln]** will be automatically dialed out in Pulse to Tone mode as selected.

V. PAUSE KEY OPERATION

In some cases, such as PABX or long distance service, pauses should be inserted in dialing sequence. The GM6388 provides stackable pause function (3.1 sec/pause) which facilitates flexible applications.

For examples :

1. Storing with Pause

Don't Care Pulse or Tone Mode. Push **[S]** , **[D1]** , **[P]** , **[D2]** ... **[Dn]** , **[S]** , **[Ln]**
then the number D1, P D2 Dn will be stored in **[Ln]**

2. Dialing with Pause

Select pulse or Tone mode. Push **[A]** **[Ln]** , then the output signal will be dialed as following sequence. D1, wait for 3.1 seconds, D2 Dn.

Note : The pause duration is 3.1 sec/pause, it can be continuously stored for longer pause duration. But every pause will occupy one digit of memory size.

VI. EMERGENCY DIALING

The GM6388 provides three memories for storing emergency numbers such as fire, police and doctor. Convenient one-key dialing operation is designed for these emergency memories which is important in easy operation :

1. Storing Emergency Numbers

Don't care Pulse or Tone Mode.

Push **[S]** **[D1]** **[D2]** ... **[Dn]** **[S]** **[EMn]**
EMn : EM1 ~ EM3

2. Emergency Dialing

Select Pulse or Tone mode.

Push **[EMn]** , then the number stored in EMn will be automatically dialed out in Pulse or Tone mode as selected.

VII. LONG DISTANCE SERVICE MEMORY DIALING

The GM6388 provides one special memory location for storing the long distance service company access code, it also provides automatic switching function from Pulse mode to Tone mode after the pause duration. This function facilitates the subscriber to utilize the long distance service company (such as MCI, SPRINT) without confusing the Pulse/Tone switching operations.

1. Storing the Long Distance Service Company Code to LDC memory. Don't care Pulse or Tone mode

[S], [D1], [D2], [Dn], [P], [P]

LDC NUMBER

[D'1], [D'2] [D'n], [S], [LDC]

AUTHORIZED ACCESS CODE

2. LDC Memory Auto dialing

When a LDC number & access code were stored ad above described procedure, the number can be automatically dialed as following sequence :

- 2-1. If the mode switch was set in Pulse mode, Push

[LDC] the output signals will be

D1 Dn, pause for 6.2 sec..

LDC NO. (PULSE)

D'1, D'1 D'n

Access Code (Tone)

Note : The chip will be automatically switched to Tone mode after the pause duration until an ON-HOOK state is detected.

- 2-2. If the mode switch was set in

Tone mode Push [LDC]

then the output signals will be D1 Dn, pause for 6.2 sec.

LDC NO. (Tone)

D'1, D'2D'n

Access Code (Tone)

Note : After completing anyone operation I-VII above, another can be operated continuously without ON-HOOK once.

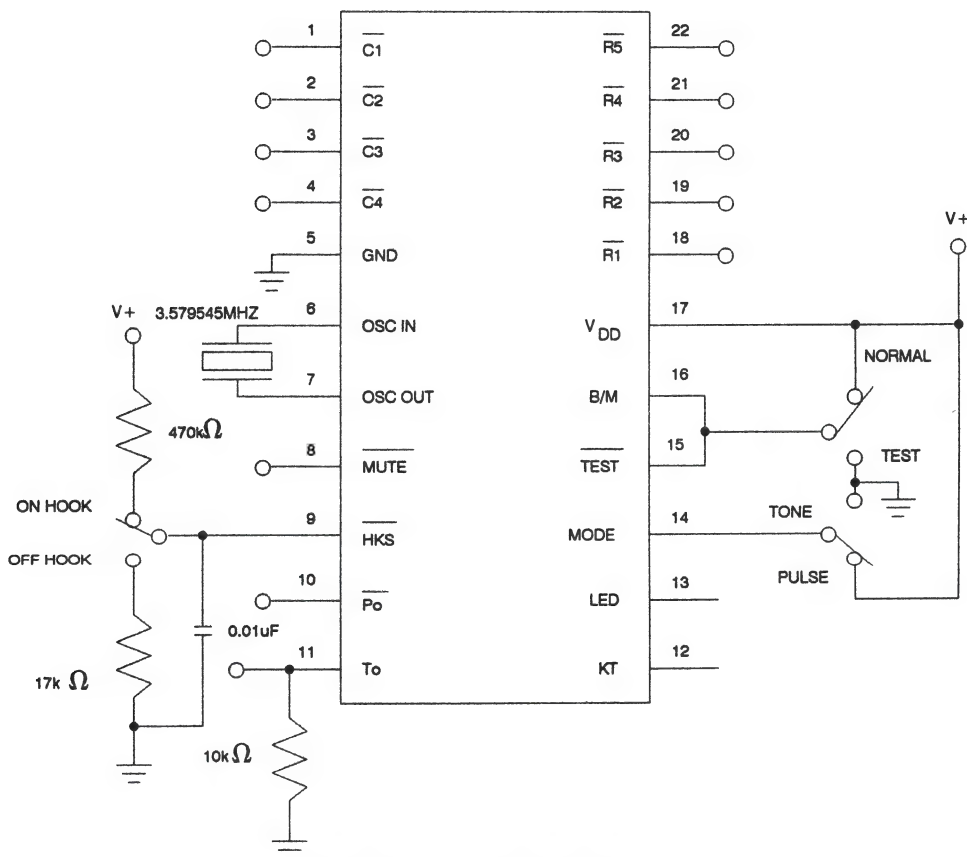


FIGURE 4. GM6388 GENERAL TEST CIRCUIT

GM6390

TONE/PULSE SWITCHABLE DIALER WITH REDIAL

Description

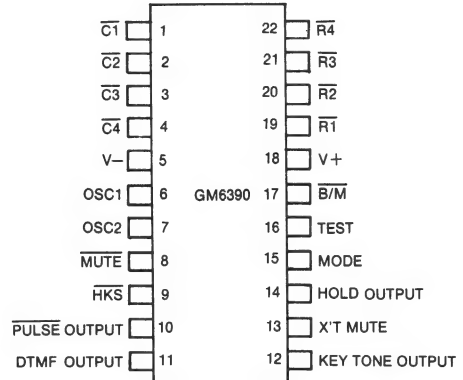
The GM6390 is a monolithic, integrated circuit manufactured using GS silicon Gate CMOS process. The device is TONE/PULSE switchable dialer with the last number redial memory and designed for low cost, high stability TONE/PULSE switchable telephone application.

The pause key and the pulse to tone key are provided for PBX and Long Distance company operation. The wide operating voltage range and low memory retention current facilitate this chip excellent for battery-free direct telephon-line operation.

Features

- DTMF/PULSE Switchable Dialer
- One 31-Digits for Last Number Redial Memory
- Auto Pause Access for PBX Operation; 3.1sec. per pause
- Pulse to Tone Key(P→T) for Toll Service Operation
- Key-Tone Output for Valid Keypad Entry Recognition.
- Electronic Keypad Input is Available; Low Action
- Uses Form A Keyboard or The Standard 2 of 8 Matrix Keyboard
- Uses Inexpensive 3.579545MHz Television Color-Burst Crystal.
- Pin Selectable for Break/Make Ratio
- Low Memory Retention Current;
 $\leq 0.2 \mu A$ at $V_+ = 1.0V$, $\overline{HKS} = 1$
- Low Operating Voltage; 2.0V for Both Tone and Pulse Mode
- Switching from Pulse Mode to Tone Mode in LDC Operation
- 22-Pin Dual-In-Line Package

Pin Connection



Keyboard Function

	C1	C2	C3	C4
R1	1	2	3	P→T
R2	4	5	6	H
R3	7	8	9	P
R4	*	0	#	R

P→T : Pulse to Tone Switch

H : Hold

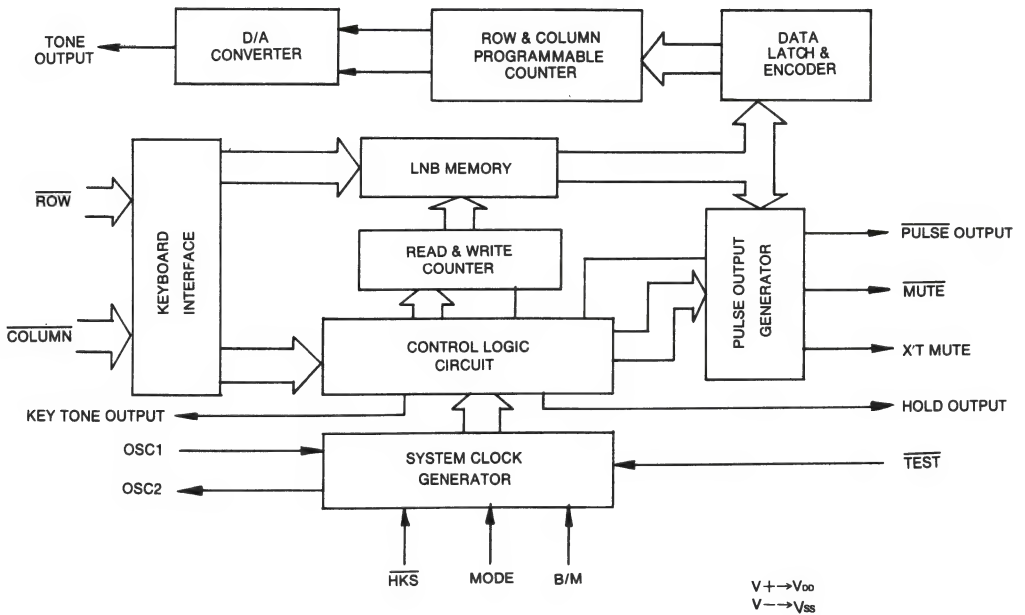
P : Pause

R : Redial

Absolute Maximum Ratings

DC Supply Voltage $V+$	6.0V
Any Input Relative to $V+$	+0.3V
Any Input Relative to $V-$	-0.5V
Power Dissipation P_D	500mW ($T_a = -25^\circ\text{C}$ to $+60^\circ\text{C}$)
Operating Temperature T_{opr}	-25°C to $+85^\circ\text{C}$
Storage Temperature T_{stg}	-65°C to $+150^\circ\text{C}$

Functional Block Diagram



Electrical Characteristics(Unless otherwise specified, $V_+ = 2.5V$, $T_a = 25^\circ C$)**DC Characteristics**

SYMBOL	PARAMETER	TEST CIRCUIT	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V+	DC Operating Voltage		2.0	—	5.5	V	Tone
			2.0	—	5.5	V	Pulse
			1.0	—	5.5	V	Memory
I _T	Operating Current(Tone)	1	—	0.6	2	mA	Unloaded and Keypad Entry
I _P	Operating Current(Pulse)		—	0.2	0.5	mA	
I _S	Standby Current	1	—	0.1	5	μA	$\overline{HKS}=0$, Unloaded and No Keypad Entry
I _{MR}	Memory Retention Current	2	—	0.1	0.2	μA	$\overline{HKS}=1$, $V_+ = 1V$
V _{TO}	Tone Output Voltage	3	120	150	180	mVrms	Row Group, $R_L = 10K\Omega$
THD	*DTMF Distortion	4	—	-30	-23	dB	$V_+ = 2.0 \sim 5.5V$, $R_L = 10K\Omega$
PE	Pre Emphasis	4	1	2	3	dB	$V_+ = 2.0 \sim 5.5V$, $R_L = 10K\Omega$
V _{TDC}	Tone Output DC Level	4	0.5V+	—	0.6V+	V	$V_+ = 2.0 \sim 5.5V$ Keypad Entry
R _L	Tone Output Load Impedance	—	10	—	—	KΩ	THD ≤ -23dB
I _{TOS}	Tone Output Sink Current	5	0.2	—	—	mA	$V_{T0} = 0.5V$, No Keypad Entry
I _{POL}	Pulse Output Leakage Current	5	—	—	0.1	μA	$V_{PO} = 5V$
			—	—	1.0	μA	$V_{PO} = 12V$
I _{POS}	Pulse Output Sink Current	6	1.0	3.0	—	mA	$V_{PO} = 0.5V$
I _{MOD}	Mute Output Drive Current	5	-0.5	—	—	mA	$V_{MO} = 2.0V$
I _{MOS}	Mute Output Sink Current	5	2.0	—	—	mA	$V_{MO} = 0.5V$
I _{KOD}	Key Tone Output Drive Current	5	-0.5	—	—	mA	$V_{KO} = 2.0V$
I _{KOS}	Key Tone Output Sink Current	5	0.5	—	—	mA	$V_{KO} = 0.5V$

(Continued)

SYMBOL	PARAMETER	TEST CIRCUIT	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I _{XMD}	X'T Mute Drive Current	5	−0.5	—	—	mA	V _{XO} =2.0V
I _{XMS}	X'T Mute Sink Current	5	0.5	—	—	mA	V _{XO} =0.5V
I _{HOD}	HOLD OUTPUT Drive Current	5	−0.5	—	—	mA	V _{HO} =2.0V
I _{HOS}	HOLD OUTPUT Sink Current	5	0.5	—	—	mA	V _{HO} =0.5V
I _{KID}	Keypad Input Drive Current	8	4	10	30	μA	V _{KI} =0V
I _{KIS}	Keypad Input Sink Current	5,7	200	400	—	μA	V _{KI} =2.5V
I _{IN}	Control Pin Input Leakage Current	—	—	±10 ^{−5}	±0.1	μA	HKS, MODE

* Dual Tone Multi-Frequency distortion is measured in term of total out-of-band power related to sum of row and column fundamental power.

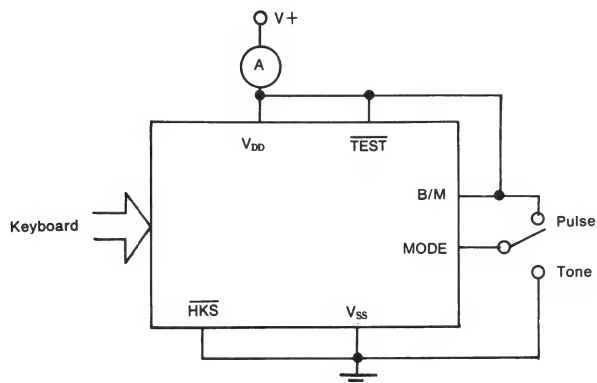
AC Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t _{KD}	Keypad Debounce Time	—	10	—	mS	$\overline{\text{TEST}}=1$
t _{PMD}	Pulse Mute Delay Time	—	40	—	mS	$\overline{\text{TEST}}=1$, B/M=60:40
		—	33.3	—	mS	$\overline{\text{TEST}}=1$, B/M=60:33
t _{PDP}	Pre-Dight Pause Time	—	40	—	mS	$\overline{\text{TEST}}=1$, B/M=60:40
		—	33.3	—	mS	$\overline{\text{TEST}}=1$, B/M=60:33
t _{TD}	Tone Duration Time	—	100	—	mS	Redial
t _{ITP}	Inter Tone Pause Time	—	106	—	mS	Redial
P _R	Pulse Rate	—	10	—	PPS	$\overline{\text{TEST}}=1$
		—	600	—	PPS	$\overline{\text{TEST}}=0$
R _{B/M}	Break/Make Ratio	—	60:40	—		B/M=1
		—	60:33	—		B/M=0
f _{R1}	Row1 Frequency	—	699	—	Hz	**ROW1
f _{R2}	Row2 Frequency	—	766	—	Hz	**ROW2
f _{R3}	Row3 Frequency	—	848	—	Hz	**ROW3
f _{R4}	Row4 Frequency	—	948	—	Hz	**ROW4
f _{C1}	Column 1 Frequency	—	1216	—	Hz	**COLUMN1
f _{C2}	Column 2 Frequency	—	1332	—	Hz	**COLUMN2
f _{C3}	Column 3 Frequency	—	1472	—	Hz	**COLUMN3
f _K	Key Tone Frequency	—	1.2	—	KHz	—

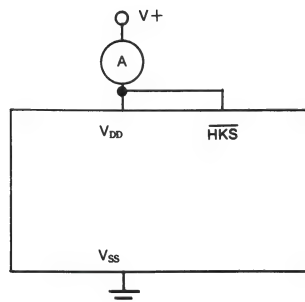
** Use 3.579545 MHz Crystal ($R_s \leq 100 \Omega$, $L_m = 96 \text{mH}$,
 $C_m = 0.25 \text{pF}$, $C_h = 5 \text{pF}$, $C_L = 18 \text{pF}$ and $\Delta F \leq \pm 200 \text{ppm}$)

Test Circuit ($V+ \rightarrow V_{DD}$, $V- \rightarrow V_{SS}$)

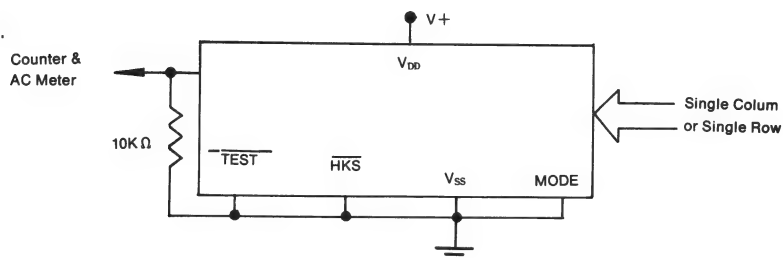
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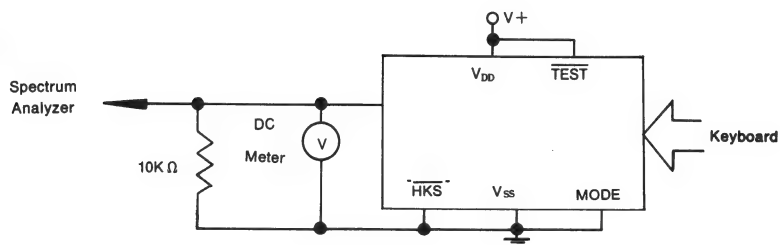
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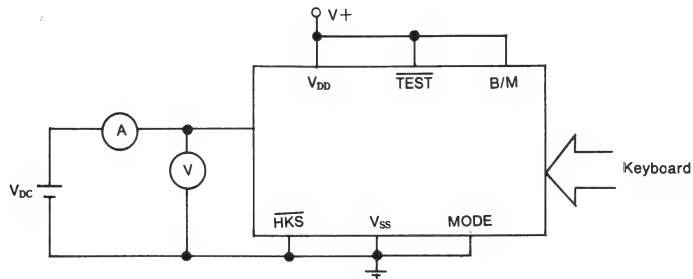


$$THD = 20 \log \frac{\sqrt{(V_1)^2 + (V_2)^2 + \dots + (V_n)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

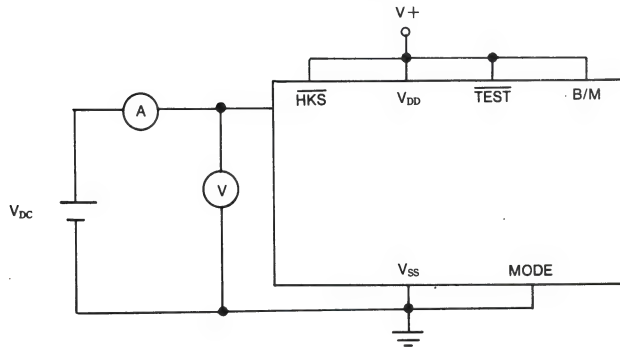
* V_1, \dots, V_n are harmonic frequency components in the 500Hz to 3400Hz band.

* V_L, V_H are the individual frequency components of the DTMF signal.

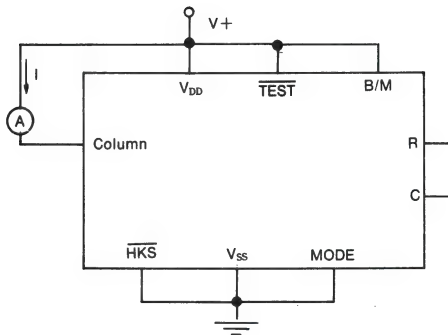
5.



6.

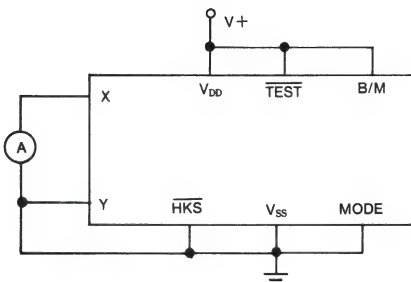


7.



- * R: Anyone of R1~R4
- * C: Anyone of C1~C4
- * $I_{KD} = I / (1 - \text{Duty Cycle})$
- * Current(I) is the dc current measured from ampere meter.

8.



- * When column drive current is tested, the X is Column and Y is Row. When row drive current is tested, they are changed.
- * $I_{KD} = I / \text{Duty Cycle}$
- * Current(I) is the dc current measured from ampere meter.

Functional Pin Description

* V+ (Pin 18)

Pin 18 is the positive supply for the circuit and must meet the maximum and minimum voltage requirements.

* V- (Pin 5)

Pin 5 is the negative supply input to the device. This is voltage reference for all specifications.

* $\overline{C1}$, $\overline{C2}$, $\overline{C3}$, $\overline{C4}$, $\overline{R1}$, $\overline{R2}$, $\overline{R3}$, $\overline{R4}$

The Keypad input interface with either the standard 2 of 8 keyboard or the inexpensive single contact (Form A) keyboard. Figure 1. shows how to connect to the two keyboard types and Figure 2 shows waveform electronic inputs.

In normal operation, a valid keypad entry is a single Row connected to a single Column. Activation of two or more buttons will result in no response except for single tone, TABLE1 illustrates address keypads function in detail.

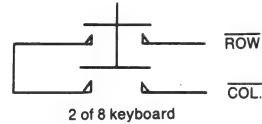
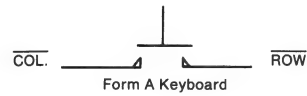
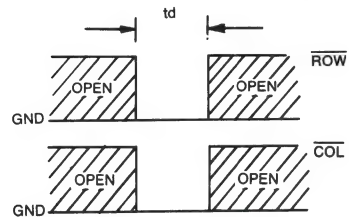


Figure 1. Keyboard Configuration



td is minimum tone duration plus keypad debounce time.

Figure 2. Electronic Input

TABLE 1. Address Keypads Truth Table

		Active Low Input		Output	
		\overline{ROW}	\overline{COLUMN}	Tone	Pulse
Tone (MODE=0) Pulse (MODE=1)	Normal ($\overline{TEST}=1$)	One	One	Dual Tone	10pps
		Two or More	One	V—	Open
		One	Two or More		
		Two or More	Two or More		
	Under Test ($\overline{TEST}=0$)	One	One	Dual Tone	600pps
		Two or More	One	Column Tone	Open
		One	Two or More	Row Tone	
		Two or More	Two or More	V—	

* OSC1, OSC2

Input/Output, Pin 6,7, OSC1 and OSC2 and inputs to an on-chip inverter used as the timing reference for the circuit. It has sufficient loop gain to oscillate when used with a low cost 3.579545MHz television color-burst crystal. The oscillator is disabled when no keypad input been sensed.

An on-board counter is used to decrease the frequency of oscillator, and creates keypad debounce, mute delay, pre-digit pause, Break-Make ratio, tone duration, Row group and Column group frequency and key tone frequency etc. Any deviation from the nominal crystal frequency is directly reflected in the time parameters above.

* MUTE

The **MUTE** Output, pin 8, is a conventional CMOS inverter which is pulled to high normally during standby, but pulled

low in the transmitting period of the address code.

* HKS

The **HKS**, hookswitch, input is used to detect the state of hand set in ON-HOOK or OFF-HOOK. This is a high impedance input and must be switched high for ON-HOOK operation or low for OFF-HOOK operation.

* PULSE Output

The **PULSE** Output, pin 10, is consisted of an open drain N-channel device. In OFF-HOOK state, this NMOS transistor keeps in ON-state only in break duration, but OFF-state in make or normal duration, in order to send the pulses train of the address codes in pulse mode. Figure 3. shows this timing.

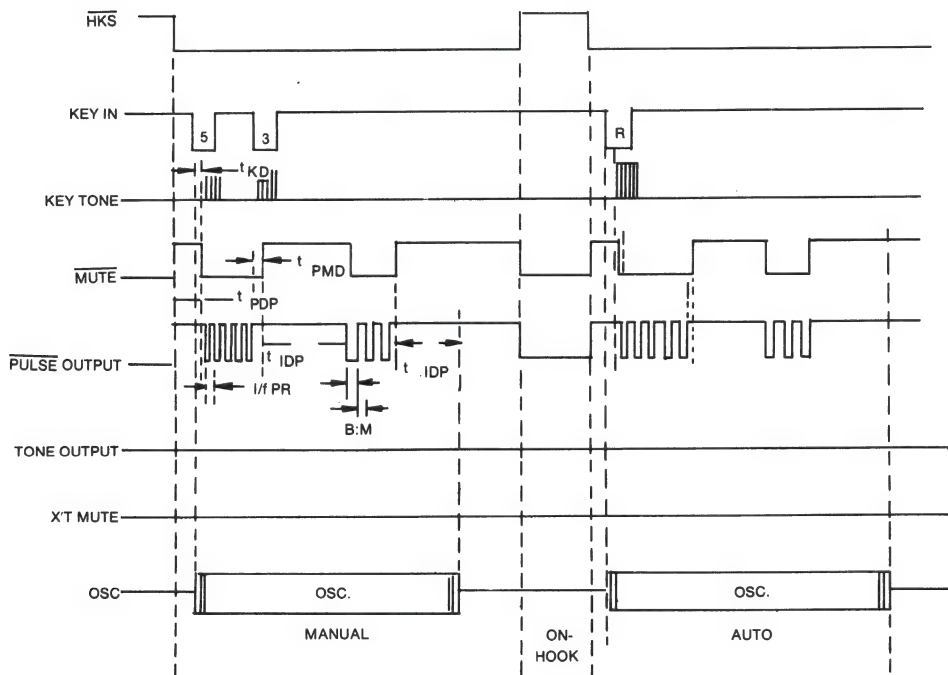


Figure 3. Pulse Mode Timing

* DTMF Output

The DTMF Output, pin 11, keeps low state regardless of keypad input in pulse mode but this pin outputs dual or single tone using the method illustrated in TABLE1 in DTMF mode. In manual dialing, the tone duration equals to the period of button pushed minus the keypad debounce time. In auto dialing, the tone duration and inter-tone-pause is internally set to be 100ms and 106ms respectively.

Figure 4. shows tone mode timing.

two or more keyboard button are pushed simultaneously.

* X'T MUTE

The X'T MUTE is a conventional CMOS inverter. In pulse mode, the X'T MUTE always keeps low level. In tone mode, it is also at low level with no keypad entry, but goes to high state when keyboard is pushed. Figure 3 and 4 show the waveform in detail. With the exception of controlling LED for indication, it can be used for muting operation in Tone mode also.

* HOLD Output

The Hold out is a conventional flip-flop. It is reset to low level by picking up the handset, and set to high level responding to push the "H" button, and go down if push the "H" button again. The "H" key is disabled and reset to low level when dialing. The Hold out is used to drive a melody IC for hold line application.

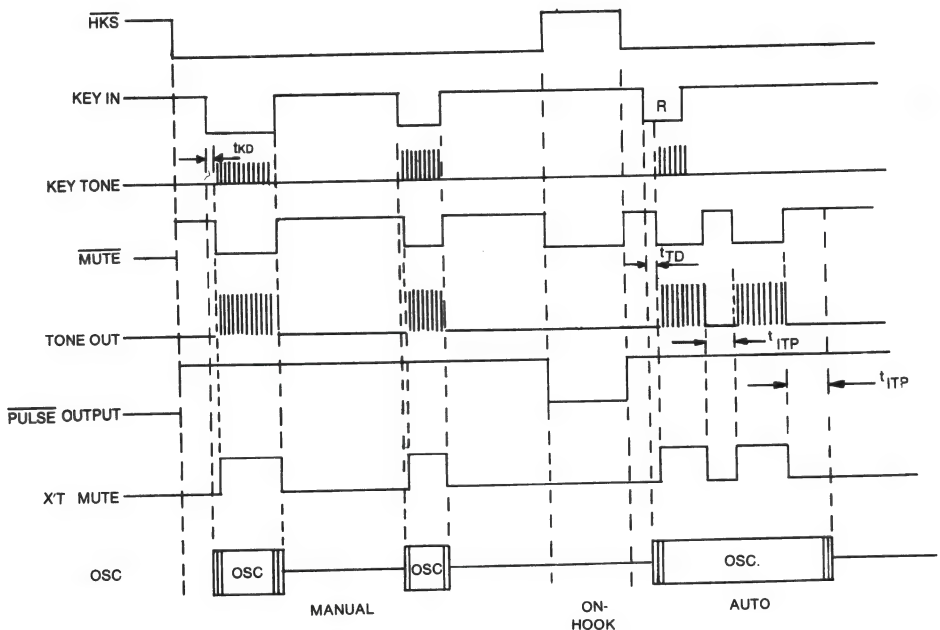


Figure 4. Tone Mode Timing

* MODE

There are two methods of switching the IC to be pulse or tone dialer. One is MODE Selection pin, pull it to high, the dialer is in pulse mode. On the contrary, the dialer is in tone mode. The other is "P→T", pulse to tone keypad, when MODE is tied to high (in pulse mode), it is changed to tone mode after pushing "P→T" button. And reset to pulse mode by putting the handset back. In tone made (MODE=0), the "P→T" button actuates nothing.

In auto redialing, the "P→T" button is not only changing mode but also providing 3.1 sec. pause if it was stored in memory previously.

* TEST

If $\overline{\text{TEST}}$ pin is tied to high, the IC is in normal operation. the pulse rate is 10pps and single tone is inhibited. If $\overline{\text{TEST}}$ pin is tied to GND, the IC is under test, single tone can be created with the operation shown in TABLE 1, and all of pulse time parameter are divided by rate of 60.

* B/M

In pulse mode, the Break/Make ratio is 60:40, if B/M=1; the ratio is 66 $\frac{2}{3}$:33 $\frac{1}{3}$, if B/M=0, the B/M pin influences nothing, in DTMF mode.

* KEYBOARD OPERATIONS

Note: All the keyboard operations should be under off-hook condition.

1. Normal Dialing

Select Pulse or Tone mode

Push $\overline{\text{D1}}, \overline{\text{D2}}, \dots, \overline{\text{Dn}}$; D1~Dn: 0~9, *, #; n is unlimited.

Then the number D1, D2, ..., Dn will be dialed out in pulse or Tone mode as selected. (Excluding of *, # in Pulse mode)

2. Redialing

Select Pulse or Tone mode

Push $\overline{\text{D1}}, \overline{\text{D2}}, \dots, \overline{\text{Dn}}$; n≤31; If busy, after ON-HOOK, Come OFF-HOOK, push $\overline{\text{R}}$, the last number D1, D2, ..., Dn will be automatically dialed out in Pulse or Tone mode as selected again.

3. Mix-Dialing

$\overline{\text{REDIALING}} + \overline{\text{MANUAL DIALING}}$ is allowable.

4. Pause and Pulse to Tone Keys Operation

In some case, such as PABX or LDC service, pause should

be inserted in dialing sequence and different dialing mode, Pulse or Tone mode, is needed. The chip provides user with pause function and Pulse/Tone switchable, which facilitate flexible application.

(a) Dialing with Pause

Select pulse or Tone mode

Push $\overline{\text{D1}}, \overline{\text{P}}, \overline{\text{D2}}, \dots, \overline{\text{Dn}}$; D1~Dn: 0~9, *, #

Then the number will be dialed out as following sequence: D1, D2, ..., Dn; without pause.

(b) Redialing with Pause

When the dialing, operation as above has done, but busy, then ON-HOOK. Come OFF-HOOK, push $\overline{\text{R}}$, then the signal will be dialed out automatically as following sequence: D1, pause 3.1 sec., D2, ..., Dn.

(c) Dialing with Pulse to Tone Key

Select the Pulse or Tone mode

Push $\overline{\text{D1}}, \overline{\text{D2}}, \dots, \overline{\text{Dn}}, \overline{\text{P} \rightarrow \text{T}}, \overline{\text{D1}}, \overline{\text{D2}}, \dots, \overline{\text{Dn}}$

Then the number will be dialed out as following sequence:

1) If the mode switch is set in pulse mode, then the output signal will be:

D1, D2, ..., Dn, D'1, D'2, ..., D'n; without pause
(Pulse mode) (Tone mode)

2) If the mode switch is set in Tone mode, then the output signal will be:

D1, D2, ..., Dn, D'1, D'2, ..., D'n; without pause
(Tone mode) (Tone mode)

(d) Redialing with Pulse to Tone Key

When the dialing operation as above has done, but busy, then ON-HOOK. Come OFF-HOOK.

push $\overline{\text{R}}$, then the signal will be dialed out automatically as same sequence of dialing with Pulse to Tone key, but has a 3.1 sec. pause during changing mode.

5. Hold Line

OFF-HOOK when the telephone is ringing. If need hold line then:

Push $\overline{\text{H}}$, and melody will be sent. After a moment, if want to talk:

Push $\overline{\text{H}}$, again, then melody will be stopped.

Note:

- 1) The pause can be continuously stored for longer pause duration, but every pause will occupy one digit of memory size.
- 2) The Pulse to Tone Key also can be stored for longer pause but always change state from pulse to tone mode. It can be reset to pulse mode only in the operation of ON-HOOK.
- 3) Hold line is not ON-HOOK state.

GL6801

DTMF GENERATOR

Description

GL 6801 is a monolithic integrated DTMF - generator intended for use in a telephone set in parallel with an electronic speech circuit. The DC characteristic to the line is set by the speech circuit. GL 6801 gives a mute signal when sending. Optional signal levels -6 and -8 dBm are available. The circuit operates with a single contact or matrix keyboard.

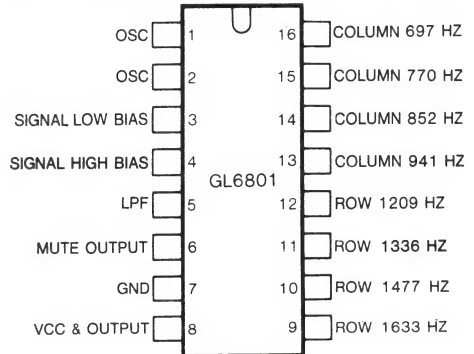
Features

- Operates with a Standard Crystal at 3.58MHz
- Wide Operating Line Voltage and Current Range
- Separately Adjusted Level from the High and Low Frequency Group
- Stabilized Signal Level Against Variations (Temperature/Line Voltage)
- Short Start-up Time
- Minimized External Components
- Easy PC Board Layout
- Internal Protection of All Inputs

Functions

- Two Tone Generation from High and Low Frequency Group
- Generated Unvalid Signals, if Two or More Keys are Pressed Simultaneously.
- All Tones can be Generated Separately.
- The Absolute Signal Level Adjusted with R_L and R_H .
- The Stabilizing Signal Level Against Variation In Temperature and Line Current.
- Pause Time and Signal Time Determined Externally from Keyboard.
- Allowed Leakage in Keyboard 1 M Ω . Typically Threshold 100K.
- Worked with Electronic Speecher, GL 6901.

Pin Configuration



Maximum Ratings

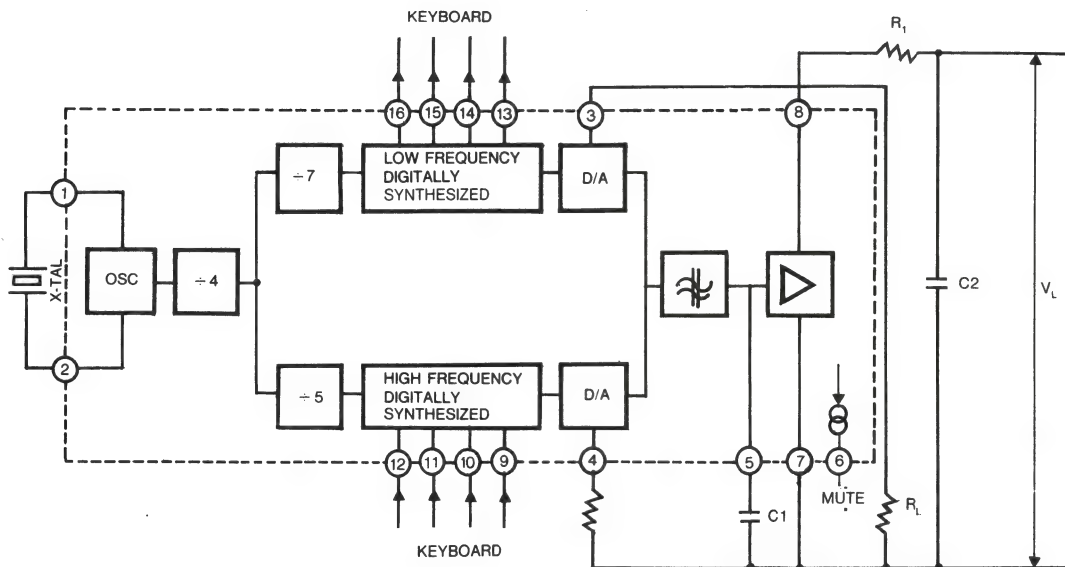
Max. Continuous Line Voltage	$V_{L(max.)}$	15 V
Peak Line Voltage($t_p=2S$)	$V_{L(max.)}$	20 V
	($t_p=20mS$)	22 V
Operating Temperature Range	T_{OPR}	-20 to $+70$ °C
Storage Temperature Range	T_{STG}	-55 to $+125$ °C

Electrical Characteristics: ($T_A = -20^{\circ}\text{C} \sim +50^{\circ}\text{C}$, $V_L = 4.3\text{V} \sim 9\text{V}$)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Line Voltage		V _L	Tone Generation DC Level 1.3V _{PP} Signal	4.3		9	V
			Stand by DC Level 2.0V _{PP} Signal	4.3		9	V
Line Current		I _L	Stand by no Key Pressed V _L =4.3V			250	μA
			Operating Current V _L =4.3V			10	mA
Mute Current		I _M	One or More Keys Pressed	125			μA
Key Resistance		R _C	Key Circuit Closed			1	KΩ
Frequency							
Low	f _{osc} =3579545Hz	Δf					
	f1=697Hz	f _{L1}		-1	-0.32	+1	%
	f2=770Hz	f _{L2}		-1	+0.02	+1	%
	f3=852Hz	f _{L3}		-1	+0.03	+1	%
	f4=941Hz	f _{L4}		-1	-0.11	+1	%
High	f5=1209Hz	f _{H1}		-1	-0.03	+1	%
	f6=1336Hz	f _{H2}		-1	-0.03	+1	%
	f7=1477Hz	f _{H3}		-1	-0.68	+1	%
	f8=1633Hz	f _{H4}		-1	-0.36	+1	%
Signal Level	High	V _H	R _H =46.4 KΩ	-11	-9	-7	dBm
			R _H =33.2 KΩ		-6		dBm
			R _H =26.1 KΩ		-4		dBm
	Low	V _L	R _L =69.3KΩ	-13	-11	-9	dBm
			R _L =48.7KΩ		-8		dBm
			R _L =39.0KΩ		-6		dBm
Ratio Signal Level High freq/Low freq		V _H /V _L		1	2	3	dB
Impedance to Line		Z _L	At Standby or Tone Generation	6			KΩ
Total Harmonic Distortion		THD	Normal Operating			-31	dBm
			Standby			-80	dBm
Harmonics			300~3400Hz			-33	dBm
			3.4~50KHz*			-33~80	dBm
			50KHz			-80	dBm
Start up Time			Output Level Within 1dB from Final Levels		3	5	mS

* Single tone distortion is less than $(-33 - 12 \log \frac{f}{3400}) \text{dBm}$

Typical Application



Generation Frequency

PIN 9	→ 1633Hz
PIN 10	→ 1477Hz
PIN 11	→ 1336Hz
PIN 12	→ 1209Hz
PIN 13	→ 941Hz
PIN 14	→ 852Hz
PIN 15	→ 770Hz
PIN 16	→ 697Hz

X-RAL = 3.5795MHz

R_1	= 33Ω
R_L	= 69.8KΩ
R_H	= 46.4KΩ
C_1	= 3.3nF
C_2	= 4.6nF

GL6840

ELECTRONIC TWO TONE RINGER

Description

The GL6840 is a monolithic integrated circuit designed to replace the mechanical bell in telephone sets, in connection with an electro acoustical converter. The device can drive either directly a piezo ceramic converter (buzzer) or a small loudspeaker. In this case a transformer is needed. The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across output amplifiers in the transducer; both tone frequencies and the switching frequency can be externally adjusted.

The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variations of the ringing signal cannot affect the correct operation of the devices.

The output bridge allows to use a high impedance transducer with acoustical results much better than in a single ended configuration.

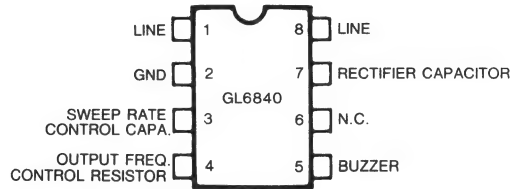
The two outputs can also be connected independently to different converters or actuators (acoustical, opto, logic).

Feature

- Low Current Consumption, in Order to Allow the Parallel Operation of 4 Devices
- Integrated Rectifier Bridge with Zener Diodes to Protect Against Overvoltages
- Little External Circuitry
- Tone and Switching Frequencies Adjustable by External Components
- Integrated Voltage and Current Hysteresis
- Bridge Output Configuration

Pin Configuration

(Top View)



Absolute Maximum Ratings

Calling Voltage (f=50Hz) continuous	120	V _{rms}
Calling Voltage (f=50Hz) 5s ON/10s OFF	200	V _{rms}
Supply Current	30	mA
Operating Temperature	-20 to 75	°C
Storage Temperature	-65 to 150	°C

Test Circuit

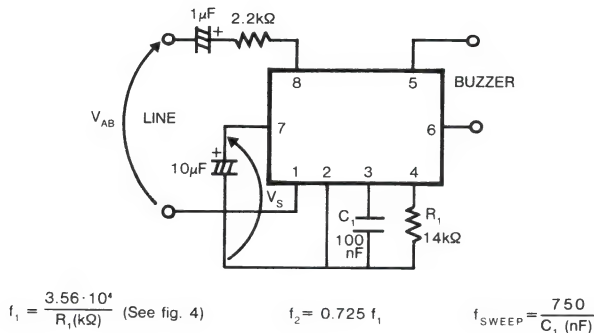


FIG. 1

Electrical Characteristics: T_A = 25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _S				26	V
Current consumption without load (Pins 1-8)	I _B	V _S =16.5 to 29.5V		1.5	1.8	mA
Activation voltage	V _{ON}		12		13.5	V
Sustaining voltage	V _{OFF}		7.8		9.3	V
Differential resistance in OFF condition	R _D		6.4			KΩ
Output voltage swing	V _{OUT}			V _S -5		V
Short circuit current (Pins 5-6)	I _{OUT}	V _S =20V		35		mA
Voltage drop between Pin 8-1 and Pin 7-2	V _S			3		V
Output frequencies f _{OUT 1} f _{OUT 2}		V _S =26V R ₁ =14KΩ V _S =0V V _S =6V	2 1.4		2.66 2	KHz
$\frac{f_{OUT 1}}{f_{OUT 2}}$			1.33		1.43	
Programming resistor range			8		56	KΩ
Sweep frequency		R ₁ =14KΩ C ₁ =100nF		10		Hz

Typical Application

TYPICAL APPLICATION WITH
BALANCED OUTPUT

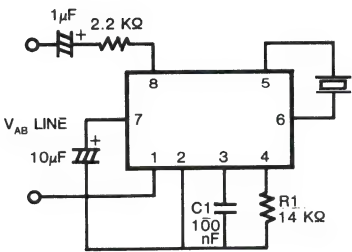


FIG. 2

F_{1OUT} VS R₁

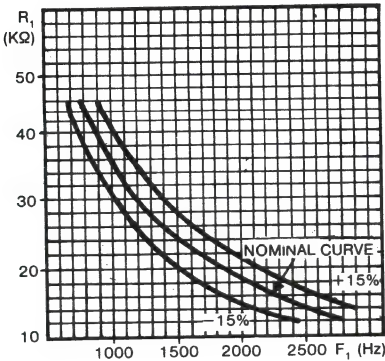


FIG. 3

GL6901

SPEECH CIRCUIT FOR USE IN ELECTRONIC TELEPHONE

Description

GL 6901 is monolithic integrated speech circuit for use in electronic telephones. It is designed for use with a low impedance microphone and to form a part of the transmission function in a telephone set. Sending and receiving gain is regulated with line length.

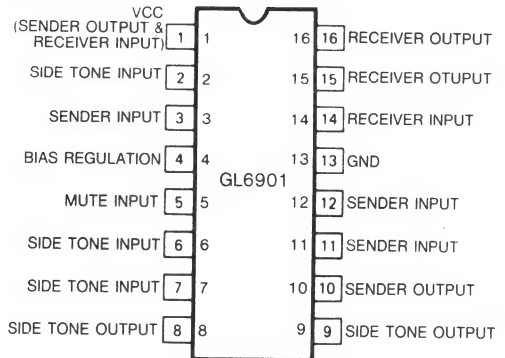
Features

- Low Voltage Operation (Down to 3.5V)
- High Output Swing on Long Lines, OdBm Down to 10mA
- Cut Off of Sending Amplifier with External Contact
- Very Short Start-up Time
- Minimum Number of External Components
- Receiving Gain Determined with Only Resistive Elements
- 20 dB Extra Gain with Volume Control for the Receiving Amplifier
- No Interaction Between the External Components

Functions

- Line Balance, Side Tone and Frequency Response Adjusted
- Mute Function for Parallel Operation with DTMF or Pulse Sending Device
- Pushbutton Controlled Cut-off of the Sending Amplifier
- Line Length Compensation of Side Tone Level
- Setting of the Gain and Frequency Response for Sending and Receiving
- Sending and Receiving Gain Regulated with Line Length
- Radio Interference Suppression

Pin Configuration



Maximum Ratings

Line Voltage ($t_D=2S$)	V_{DC}	22	V
Continuous Operating Line Current	I_{DC}	100	mA
Operating Temperature Range	T_{OPR}	$-40 \sim +70$	$^{\circ}C$
Storage Temperature Range	T_{STG}	$-55 \sim +125$	$^{\circ}C$

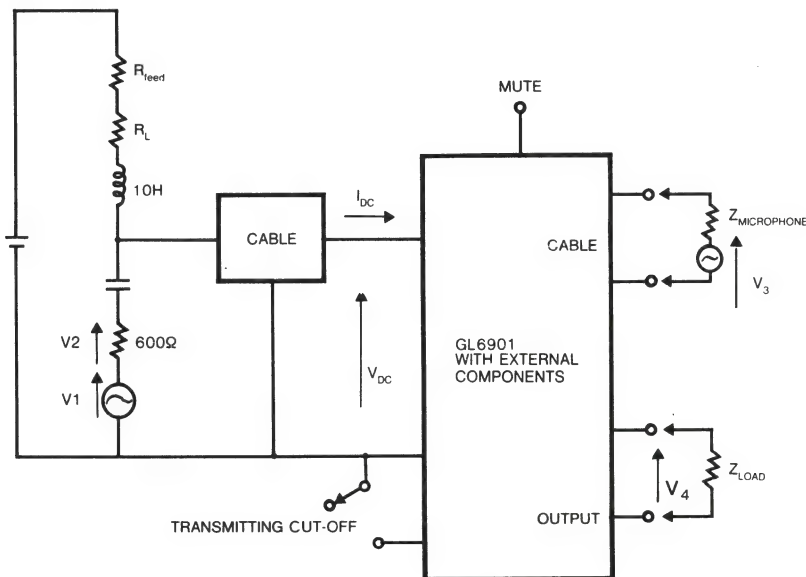
Electrical Characteristics (At $T_A = 25^\circ\text{C}$, No cable and no line rectifier unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Terminal Voltage	$I_{DC} = 10\text{mA}$		3.5		V
	$I_{DC} = 100\text{mA}$		12		V
Transmitting Amplification	$20 \cdot \log_{10} \left(\frac{V_2}{V_3} \right)$ short line		44*		dB
Transmitting Range of Regulation	Short line to long line		5		dB
Receiving Amplification	$20 \cdot \log_{10} \left(\frac{V_4}{V_1} \right)$ short line		-16.5*		dB
Receiving Range of Regulation	Short line to long line		5		dB
Transmitter Input Impedance			1		K Ω
Transmitter Dynamic Output			1.5		V
Transmitter Max Output			3		V
Receiver Output Impedance			Low**		Ω
Receiver Dynamic Output			1.1**		V
Receiver Max Output	Measured with line rectifier		1.7**		V
Transmitter Output Noise	P_s of-weighting, R_{el} . 1V short line		-70		dB
Receiver Output Noise	A-weighting, Rel. 1V $R_L = 0$ with cable		-80		dB _A

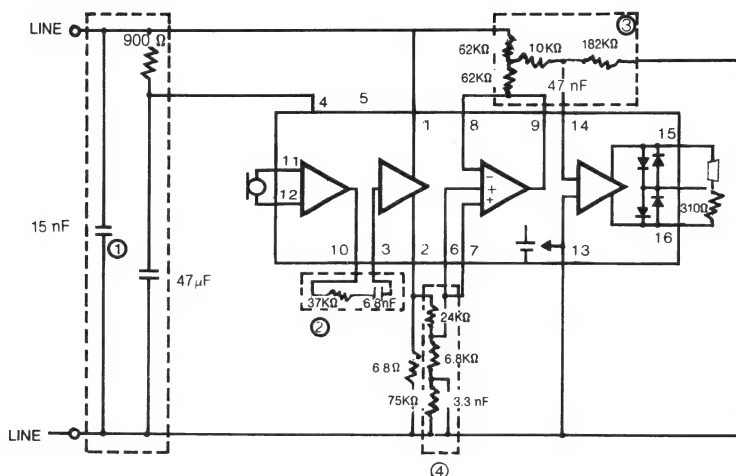
* Adjustable to both higher and lower values with external components.

** The output impedance can be adjusted with an external resistor. This gives a corresponding change in the output swing.

Test Set Up



Typical Application



External RC-networks

- ① Line impedance and radio interference suppression
- ② Sender amplifier, gain set and frequency adjustment
- ③ Receiver amplifier, gain set and frequency adjustment
- ④ Side tone adjustment

GL6981

LOW VOLTAGE SPEECH CIRCUIT

Descriptions

The GL6981 is a bipolar integrated speech circuit for use in electronic telephones. The circuit is designed to operate at low supply voltages down to 1.3V making it usable when connected in parallel with other telephones.

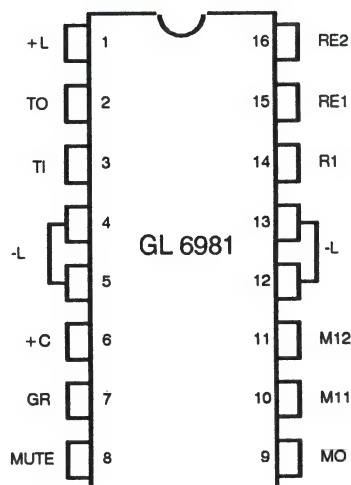
A differential-input microphone amplifier permits the use of a dynamic microphone. Electret microphones (with built-in FET buffer amplifiers) may also be used.

Gain regulation circuitry provides compensation for loop losses in both the transmit and receiver amplifiers.

The receiver amplifier has a balanced push-pull output stage for good driving capabilities even at low supply voltage.

A straight-forward design procedure simplifies adaptation of the circuit to suit different transducers and battery feeding systems.

Pin Configurations



Features

- Low voltage operation down to 1.3V DC.
- AC voltage swing down to 0.4V.
- Transmit and receive gain compensation.
- Differential microphone input for dynamic microphone.
- Current generator output powers electret buffer amplifier or pulse dialer.
- Balanced receiver output stage.
- 16 pin "batwing" DIP handles 1.5W power dissipation.

Absolute Ratings

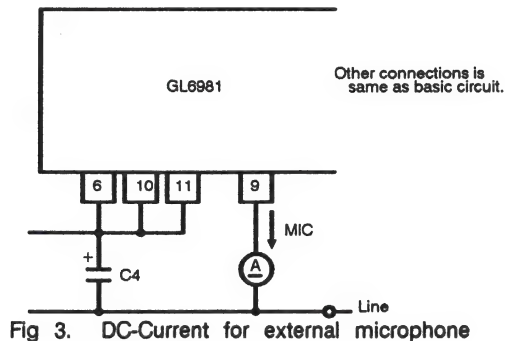
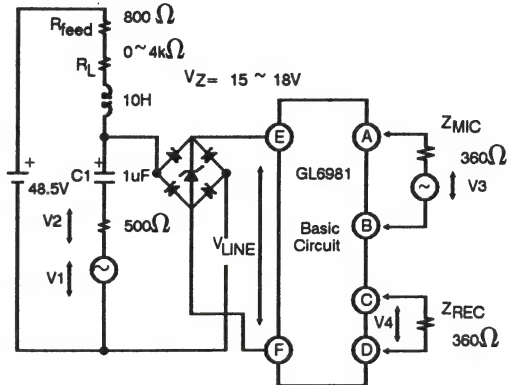
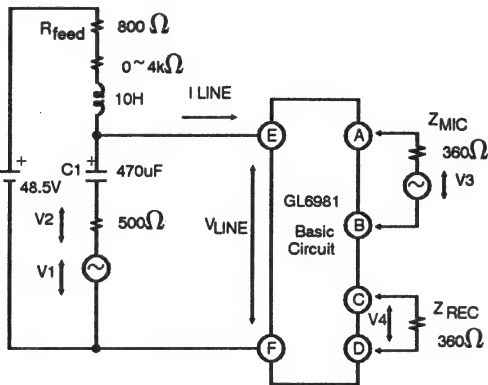
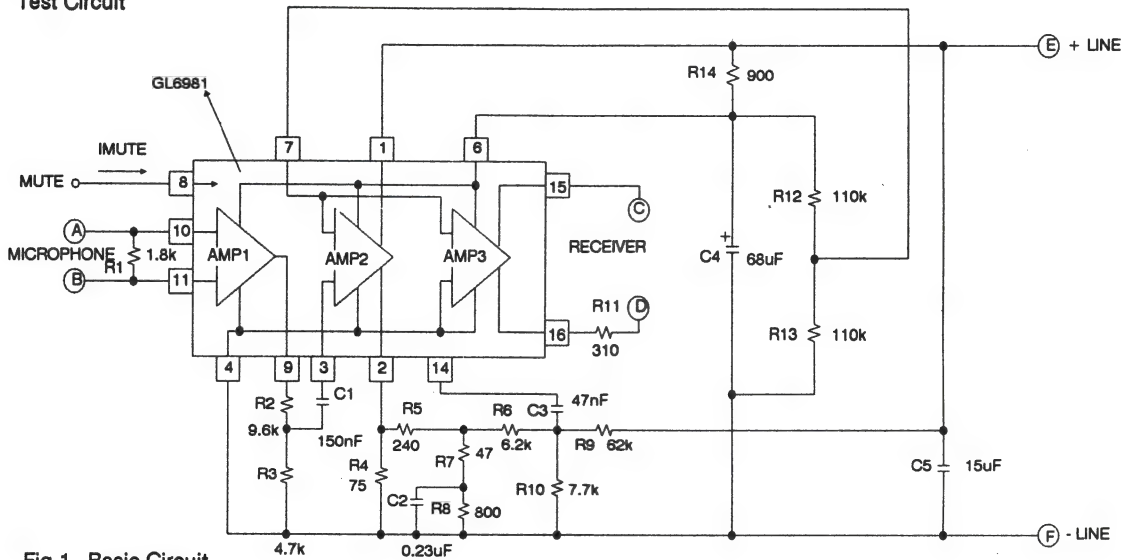
Line Current I_L	150 mA
Line Voltage V_L	Continuous 15 V
$t_P = 2s$	20 V
$t_P = 10ms$	22 V
Power Dissipation	1.5W
Operating Temperature	-20°C + 70°C
range T_{amb}	
Storage Temperature	-55 to + 125°C
range T_{stg}	

Electrical Characteristics DC Characteristics :

Tamb -25°C. Measured using test circuits of fig. 1 and 2 without artificial cable, unless otherwise noted.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Line Voltage	V_L V_L V_L $I_L = 2.5 \text{ mA}$ $I_L = 10 \text{ mA}$ $I_L = 100 \text{ mA}$ $R_A = 47\Omega$		1.4 3.5 8.5		V V V
	V_L V_L V_L $I_L = 2.5 \text{ mA}$ $I_L = 10 \text{ mA}$ $I_L = 100 \text{ mA}$ $R_A = 75\Omega$		1.5 3.7 11.3		V V V
Transmitting gain	V_2 , V_3 $20 \log (V_2/V_3)$ $f_m = 1 \text{ kHz}$ (Adjustable with R2 and R3) $R_L = 0\Omega$ $R_L = 400\Omega$ $R_L = 900 \text{ to } 2200 \Omega$	41 43.5 46	43 45.5 48	45 47.5 50	dB dB dB
Transmitting gain, Range of regulation	$f = 1 \text{ kHz}$, $R_L = 0$ to $R_L = 900\Omega$	3	5	7	dB
Transmitting frequency response	200-3400 Hz	-1		+1	dB
Receiving gain	V_4 , V_1 $20 \log (V_4/V_1)$ $f = 1 \text{ kHz}$ (Adjustable with R10) $R_L = 0\Omega$ $R_L = 400\Omega$ $R_L = 900 \text{ to } 2200\Omega$	-18.5 -16 -13.5	-16.5 -14 -11.5	-14.5 -12 -9.5	dB dB dB
Receiving gain, range of regulation	$f = 1 \text{ kHz}$, $R_L = 0$ to $R_L = 900\Omega$	3	5	7	dB
Receiving frequency response	200-3400 Hz	-1		+1	dB
Input impedance, microphone amplifier	$f = 1 \text{ kHz}$		2.5/1.8		k Ω
Transmitter dynamic output level	V_2 200-3400 Hz, THD $\leq 2\%$ $I_L = 20\text{-}100 \text{ mA}$		1.5		V _{peak}
Transmitter maximum output level	V_2 200-3400 Hz $I_L = 0\text{-}100 \text{ mA}$ $V_3 = 0\text{-}1\text{V}$		3.5		V _{peak}
Receiver output impedance	$f = 1 \text{ kHz}$		310+6		Ω
Receiver dynamic output level	V_4 200-3400Hz, THD $\leq 2\%$ $I_L = 20\text{-}100 \text{ mA}$		0.5		V _{peak}
Receiver maximum output level	V_4 200-3400 Hz $I_L = 0\text{-}100 \text{ mA}$ $V_1 = 0\text{-}50\text{V}$		1		V _{peak}
Transmitter noise level	V_2 Psophometric weighted relative to $1V_{rms}$, $R_L = 0$		-70		dB
Receiver noise level	V_4 A-weighted, relative to $1V_{rms}$, with artificial cable: 0-5 km, $\phi = 0.5 \text{ mm}$ 0-3 km, $\phi = 0.4 \text{ mm}$		-80		dB
DC current to external microphone amplifier	Imic Pins to and 11 to pin 6 $I_L = 0\text{-}150 \text{ mA}$ DC-current at pin 9	300			μA
Mute current	Imute $I_L = 10\text{-}150 \text{ mA}$	100			μA

Test Circuit



Pin Descriptions.

PIN	NAME	FUNCTION
1	+L	Output of the DC-regulator and transmit amplifier. This pin is connected to the line through a polarity guard diode bridge.
2	TO	Output of the transmit amplifier. This pin is connected to a resistor R4 of 47Ω to 100Ω to -L, which in practice sets the DC series-resistance of the circuit. The output has a low AC output impedance, and the signal is used to drive a sidetone balancing network R5, R7, R8 and C2.
3	TI	Input of the transmit amplifier.
4, 5 12, 13	-L	The negative power terminal, connected to the line through a polarity guard diode bridge.
6	+C	This pin is the positive power supply terminal for most of the circuitry inside the GL6981 (about 1 mA current consumption). The majority of the line current however, passes through the TO and +L pins (see above). The +C pin shall be connected to a decoupling capacitor, C4, of 47 to 150 μF .
7	GR	This pin is control input for the gain regulation circuitry.
8	MUTE	The MUTE input which requires min. 100 μA to mute the microphone and receiver amplifiers.
9	MO	Output of the microphone amplifier. When electret microphones are used this pin can be connected as a current generator output. See functional description for pins 10 and 11 below.
10, 11	M11, M12	Inputs of the microphone amplifier. The input impedance at these pins is approx. 2.5k Ω . Connecting pins 10 and 11 to pin 6, (+C) switches pin 9 (MO) to a current generator output, that sources about 300 μA for an external electret buffer amplifier.
14	R1	Input of receiver amplifier. Input impedance is approx. 35k Ω .
15, 16	RE1, RE2	Receiver amplifier output. The output is intended to drive low impedance receivers.

Functional description

The GL6981 contains a DC-regulator, a microphone amplifier, a transmit amplifier and a receiver amplifier.

The DC-regulator determines the voltage/current characteristics of the circuit looking from the line, the circuit acts as a reference voltage of approx.

3 Volts in series with a resistor (externally set). The voltage reference is derived from a bandgap reference, which provides for temperature-stable DC-characteristics. To maintain operation even when the line voltage (inside polarity guard diode bridge) drops below 3 Volts, the circuit automatically switches to a lower reference voltage.

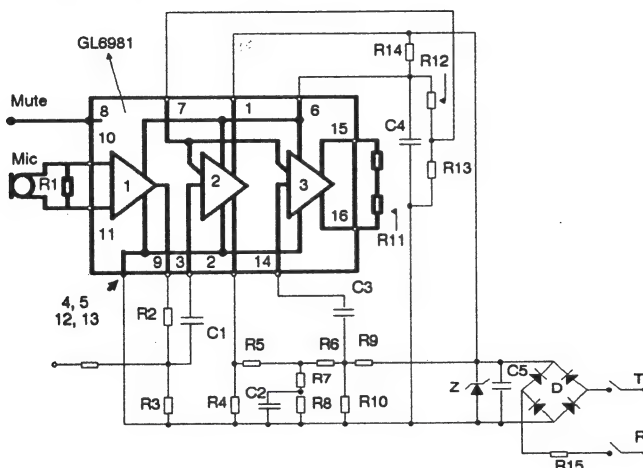
A microphone amplifier with a differential input stage, and hence good common mode rejection, is provided for low-sensitivity magnetic or dynamic microphones.

The transmit amplifier receives its input signal either from the microphone amplifier or from a separate electret buffer amplifier (that can be powered directly

from the circuit). The transmit output stage contains the previously described DC-regulator. The AC-gain is regulated with the line length (selectable) and the output level is amplitude limited to eliminate sidetone distortion at high transmitting levels.

The sidetone cancellation (or hybrid function) works as follows: A signal on the line is taken from the transmit amplifier and fed through a sidetone balancing network into the summing junction of the receiver amplifier. The (inverted) signal from the line is added, and sidetone cancellation occurs. Only the receive signal, together with a much weaker sidetone signal is left at the input of the receiver amplifier.

The AC-gain of the receiver amplifier is also regulated with the line length. The output from the receiver amplifier is intended to drive low-impedance (down to 150ohms) receivers. An internal clipping network limits the signal to the receiver and prevents acoustic shocks.



R1 = 1.8 k Ω R6 = 6.2 k Ω
 R2 = 9.6 k Ω R7 = 62 Ω
 R3 = 4.7 k Ω R8 = 2.1 k Ω
 R4 = 47 Ω R9 = 68 k Ω
 R5 = 130 Ω R10 = 3.3 k Ω to 10 k Ω

R11 = 310 Ω
 R12 = 43 k Ω
 R13 = 30 k Ω
 R14 = 910 Ω
 R15 = 5 to 10 k Ω

R16 = Adjust for DTMF levels C5 = 15 nF
 C1 = 68 nF Z = 15V Zenerdiode 5 W
 C2 = 0.22 μ F
 C3 = 47 nF
 C4 = 100 μ F

Fig 4. Basic application of GL6981 or 48V 2x200 Ω battery feeding system and dynamic or magnetic microphone and receiver.

Applications information

The GL6981 is a flexible circuit designed to meet specifications from telephone administrations all over the world. Adaptation to different battery feeding systems and transducers is made by selecting the values of a few external components. Figure 4 above shows the GL6981 and associated components in a basic telephone speech network. To complete an electronic telephone, the circuit needs to be supplemented by a tone Ringing and a DTMF or pulse dialer circuit.

Then proceeding through a design, some of the circuit adjustments will interact with each other. It is therefore recommended to adjust the parameters in the following order.

1. Impedance to the line.
2. DC-characteristics.
3. Microphone selection, transmitting gain and frequency response
4. Gain regulation.
5. Side-tone level, receiving gain and frequency response.

Impedance to the line

The output impedance of the circuit is determined by R14 in parallel with C5. R14 is normally set to a value between 600 and 900 Ω to satisfy the return loss requirements. R14 also supplies the operating current for the majority of the circuitry inside GL6981.

It is recommended to select a value near 900 Ω , in order to maximize the available output level from the transmit amplifier a lower value of R14 requires a larger capacitor C4 for the stabilization of the supply voltage at pin 6. C5 should be located near the circuit to effectively suppress any radio interference pick-up.

DC-characteristics

The DC-behaviour is adjusted by resistor R4, which determines the slope at the V-I curve. For line currents above 10mA, the circuit acts as a series combination of R4 and a zener diode of 3 volts.

The minimum working voltage is approximately 1.3volts, which corresponds to about 2.5mA line current with $R4 = 47\Omega$.

R4 should be selected to give a safe operating point at very short loops. A low value results in excessive current through the circuit, while a larger resistance may raise the voltage above the maximum rated. Suitable values of R4 range from 47 to 100 Ω depending on the battery feeding system.

Microphone selection, transmitting gain and frequency response

The microphone amplifier section is intended for low-sensitivity dynamic microphones and provides about 26 dB voltage gain. A differential input stage (pins 10 and 11) gives good common mode rejection. A resistor R1 as shown in figure 4, may be required to define a correct load impedance for an electromagnetic microphone if used. Dynamic microphones can be connected directly to the input pins.

The total transmitting gain is adjusted by a resistive attenuator R2 and R3. Capacitor C1 is inserted to give a low-frequency cut-off in the transmit path. The values of R2 and R3 should be selected to present about 3k Ω source impedance for the transmit amplifier input at pin3.

The transmit amplifier itself has a current generator output which means that the voltage gain is partly determined by the ratio between R14 in parallel with the line impedance and R4. The voltage gain from the input at pin 3 to the output output(pin 1) varies approximately between 32 and 37 dB over the regulation range with $R14 = 900\Omega$, $R4 = 47\Omega$ and a line impedance of 600 Ω . The available gain is therefore enough to enable an electret microphone to be connected directly to pin 3. In such a case, it is necessary to utilize the current generator at pin 9 to feed the electret buffer amplifier since the transmit amplifier itself is not affected by the MUTE input. The current generator at pin 9, which is switched off when the circuit is muted, is selected by tying pin2 10 and 11 to pin 6. Another method of interfacing an electret microphone is shown in figure6.

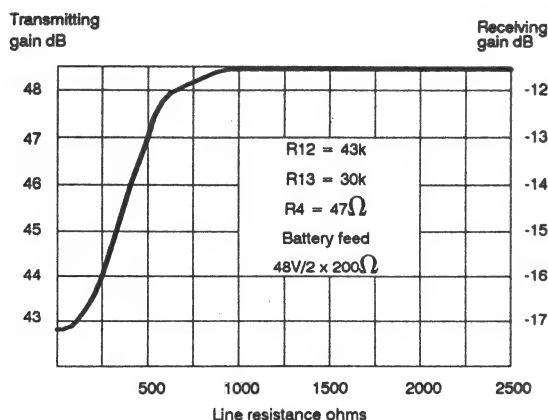


Fig 5. Gain Regulation

Gain regulation

Automatic gain regulation circuitry in the transmit and receiver amplifiers reduces the gain when the loop length decreases. The control voltage for the gain regulation is fed into pin 7. By changing the resistive attenuator consisting of R12 and R13. It is possible to shift the location of the regulation curve to get a correct compensation in different battery feeding system. The slope of the curve is determined by R4.

Side-tone level, receiving gain and frequency response

Side-tone cancellation occurs at the input of the receiver amplifier pin 14, which receives opposite-phased transmit signals from the line and the side-tone network respectively.

Resistor R5 and the actual balancing network consisting of R7, R8 and C2, simulates a first order approximation of the output impedance of the circuit and the line impedance. A practical sequence for determining the component values in the side-tone network is given below.

1. The value of R5 is chosen from two to four times R4.
2. R7, R8 and C2 should simulate the amplitude and phase response of the line impedance seen at the line terminals. The impedance level of the balancing network should be about one tenth of the line impedance. The values given in figure 4 is a good starting point in most cases.
3. The ratio between R6 and R9 should be set to make the signals coming from the line and from the side-tone network equal in amplitude so that cancellation occurs. The value of R6 should be about an order of magnitude larger than the impedance level of the balancing network.
4. R10 is selected to give the desired receiving gain.
5. Steps 2 to 4 above may have to be repeated to give the required side-tone level and receiving gain.

The coupling capacitor C3 is needed for low-frequency cut-off in the receiver amplifier. The input impedance at pin 14 is approximately 35 k Ω . A balanced push-pull output stage provides good driving capabilities even at low supply voltages. The circuit is intended to drive low-impedance (down to 150 Ω) receivers. High-inductance magnetic receivers may require a series resistor R11 to define a correct driving impedance. Internal clamping diodes in the output stage prevent excessive acoustic levels which may cause damage to the listeners ear.

GM62093

12 × 8 CROSSPOINT SWITCH WITH CONTROL MEMORY

Description

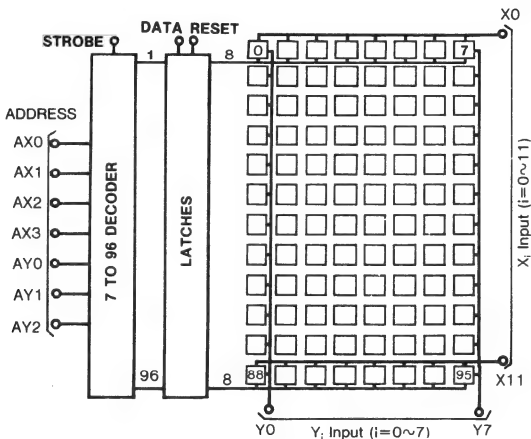
The GM62093 contains a 12×8 array of Crosspoint together with a 7 to 96 Line decoder and latch circuits. The GM62093 employs GS's advanced High voltage CMOS process technology. It provides extra low operating current and low power dissipation.

Anyone of the 96 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when is switched at logical one. The GM62093 is available in a 40 lead dual in-line plastic and ceramic packages.

Features

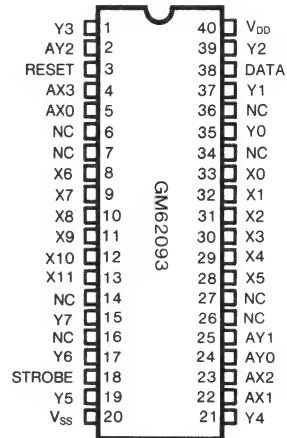
- CMOS 12 × 8 Cross Point Switch with Control Memory
- Low On Resistance: 45Ω Max at $V_{DD} = 14V$
- Internal Control Latches
- ΔR_{on} 15Ω Max
- 6V_{pp} Analog Signal Capability
- Less Than 1% Total Distortion at 0 dbm
- Extra Low Operating Current
- Extra Low Cross-Talk Between Any Two Switches
- Standard CMOS Noise Immunity
- TTL Compatible Input

Block Diagram



Pin Configuration

(Top View)



Applications

- PBX Systems
- Mobile Radio
- Test Equipment Instrumentation
- Analog/Digital Multiplexer

Absolute Maximum Ratings

DC Supply voltage	V_{DD}	-0.5 to 18 V
Input voltage range	V_{IN}	-0.5 to $V_{DD} + 0.5V$
DC input current (analog input)	I_{IN}	±10mA
Power dissipation	$P_D(P-DIP)$ (C-DIP)	0.6W 1W
Operating temperature range	T_{OPR}	0° to 70°C
Storage temperature range	T_{STG}	-65°C to 150°C

Recommended Operating Condition

DC Supply Voltage	V_{DD}	7 to 16 V
Input Voltage Range	V_{IN}	0 to V_{DD}
Operating Temperature Range	T_{OPR}	0 to 70 °C

Static Electrical Characteristics: ($T_A=0^{\circ}\text{C}$ to 70°C , $V_{DD}=14\text{V}$)

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
• CROSSPOINT						
I_{DD}	Quiescent Supply Current	All Digital Inputs at V_{SS} or V_{DD}			100	μA
		All Digital Inputs at 2.4V		7	15	mA
R_{ON}	On Resistance	$V_{IDC}=3.5\text{V}$ and $I(\text{thru S/W})=10\text{mA}$			45	Ω
ΔR_{ON}	Ron Difference Between Any Two Swtiches				15	Ω
I_{LOFF}	Off Leakage	All Switchs Off $V_{OS}=V_{IS}=0$ to V_{DD}			± 500	nA
• CONTROLS						
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{LEAK}	Input Leakage	$V_{IN}=0$ to V_{DD}			± 500	nA

Dynamic Electrical Characteristics: ($T_A=25^{\circ}\text{C}$, $C_L=50\text{pF}$, $V_{DD}=14\text{V}$)

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
• CROSSPOINT						
t_p	Propagation Delay Time	$R_L=1\text{k}\Omega$, $V_{DC}=5\text{V}$ $V_{IS}=2V_{PP}$			30	nS
f_{RES}	Frequency Response [$20 \log(V_{OUT}/V_{IN})=-3\text{dB}$]	$R_L=1\text{k}\Omega$, $V_{DC}=5\text{V}$ $V_{IS}=2V_{PP}$, $C_L=3\text{pF}$		40		MHz
	Sine Wave Response (Distortion)	$R_L=1\text{k}\Omega$, $V_{DC}=5\text{V}$, $V_{IS}=2V_{PP}$, $f=1\text{MHz}$			1	%
	Feedthrough (All S/W's Off)	$R_L=1\text{k}\Omega$, $V_{DC}=5\text{V}$, $V_{IS}=2V_{PP}$, $f=10\text{KHz}$			-80	dB
	Crosstalk Between Any Two Channels	$R_S=50\Omega$, $R_L=1\text{k}\Omega$, $V_{IS}=2V_{PP}$, $f=1\text{KHz}$		-110	-95	dB
C_X	Capacitance (X_N to Ground)	Switch Off			20	pF
C_Y	Capacitance (Y_N to Ground)	Switch Off			30	pF
C_{DI}	Digital Input Capacitance			5		pF
• CONTROLS						
t_{DS}	Strobe to Switch Delay	$R_L=1\text{k}\Omega$, $t_r=t_f=20\text{nS}$			160	nS
t_{DD}	Data to Switch Delay	$R_L=1\text{k}\Omega$, $t_r=t_f=20\text{nS}$			180	nS
t_{DA}	Address to Switch Delay	$R_L=1\text{k}\Omega$, $t_r=t_f=20\text{nS}$			200	nS
t_{DR}	Reset to Switch Delay	$R_L=1\text{k}\Omega$, $t_r=t_f=20\text{nS}$			200	nS
t_{SD} t_{SA}	Data Setup Time Address Setup Time	$R_L=1\text{k}\Omega$, $t_r=t_f=20\text{nS}$	30			nS
t_{HD} t_{HA}	Data Hold Time Address Hold Time	$R_L=1\text{k}\Omega$, $t_r=t_f=20\text{nS}$	30			nS
t_{SW} t_{RW}	Minimum Strobe Pulse Width Minimum Reset Pulse Width	$R_L=1\text{k}\Omega$, $t_r=t_f=20\text{nS}$	200			nS

Functional Description

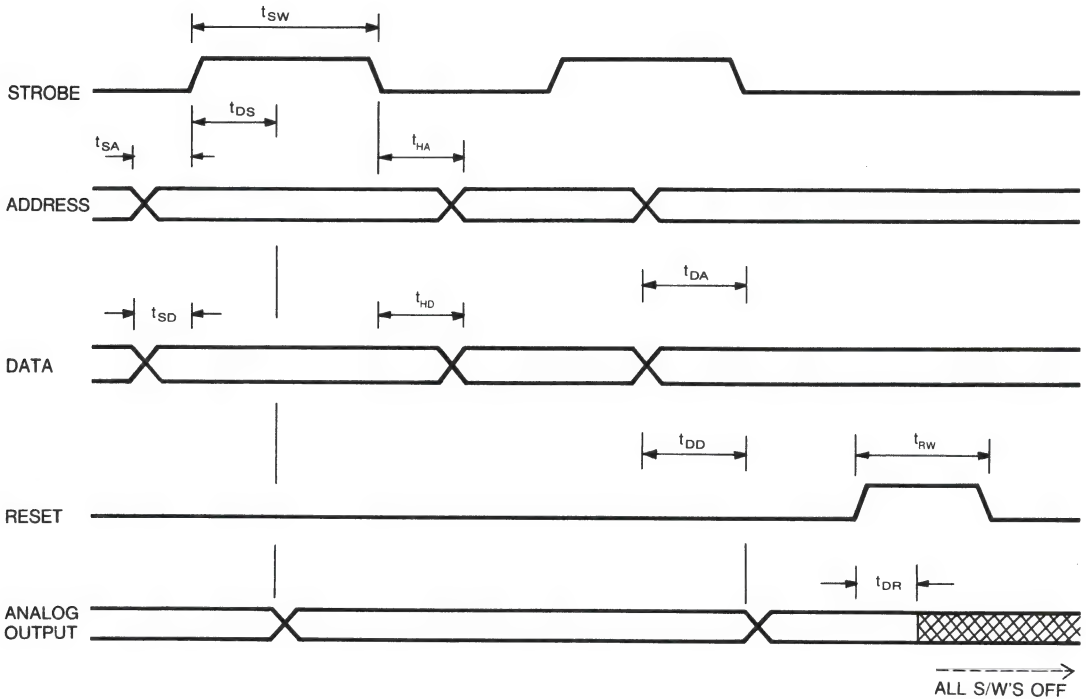
The GM62093 contains a 12×8 array of analog switches, each with a latch to maintain its on(closed) or off (opened) state.

Seven ADDRESS lines (AX0~AX3, AY0~AY2) are provided to address any one of the 96 switches.

After any one of the switches is selected, the DATA pin

may be held high to turn the switch on, or low to turn it off. Finally a positive pulse to the STROBE pin initiates the action determined by the ADDRESS and DATA pins. All 96 switches can be turned off by forcing the RESET pin high.

Timing Diagram

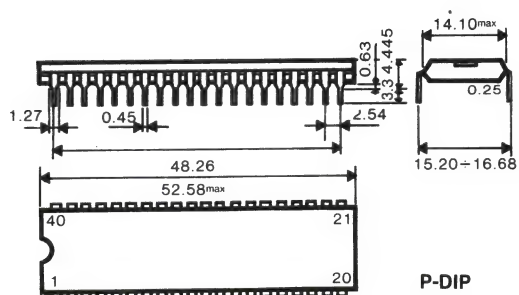


Truth Table

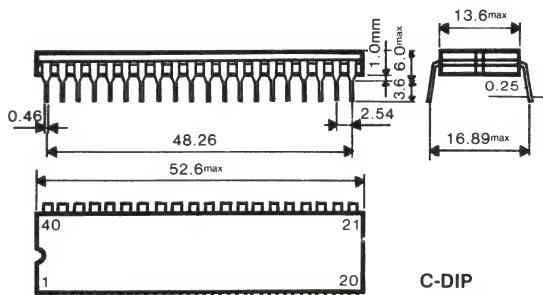
Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 -Y0
1	0	0	0	0	0	0	X1 -Y0
0	1	0	0	0	0	0	X2 -Y0
1	1	0	0	0	0	0	X3 -Y0
0	0	1	0	0	0	0	X4 -Y0
1	0	1	0	0	0	0	X5 -Y0
0	0	0	1	0	0	0	X6 -Y0
1	0	0	1	0	0	0	X7 -Y0
0	1	0	1	0	0	0	X8 -Y0
1	1	0	1	0	0	0	X9 -Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	0	0	0	1	0	0	X0 -Y1
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	0	0	X11-Y1
0	0	0	0	0	1	0	X0 -Y2
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	0	1	0	X11-Y2
0	0	0	0	1	1	0	X0 -Y3
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	1	0	X11-Y3
0	0	0	0	0	0	1	X0 -Y4
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	0	0	1	X11-Y4
0	0	0	0	1	0	1	X0 -Y5
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	0	1	X11-Y5
0	0	0	0	0	1	1	X0 -Y6
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	0	1	1	X11-Y6
0	0	0	0	1	1	1	X0 -Y7
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	1	1	X11-Y7

Ax=0110, 1110, 0111 and 1111 and not allowed

Package Dimensions



Dimensions in mm



	DATA SHEET INDEX	
	QUALITY ASSURANCE MANUAL	
1.	TV APPLICATION	
2.	VCR APPLICATION	
3.	AUDIO APPLICATION	
4.	TELECOM APPLICATION	
5.	REMOTE CONTROL APPLICATION	
6.	INDUSTRY APPLICATION	
	GOLDSTAR SEMICONDUCTOR SALES NETWORK	

GM3043

CMOS REMOTE CONTROL TRANSMITTER

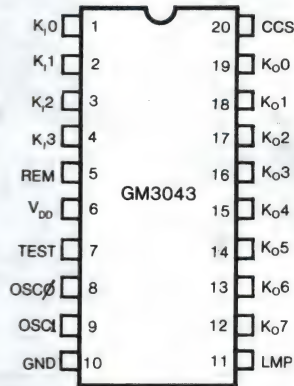
Description

The GM3043 is a CMOS IC for control circuits of infrared remote control transmitter which is available for TV, STEREO, VTR and TOY etc. GM3043 is designed to transmit 8960 commands $[(32 \text{ KEY} + 3) \times 256 \text{ custom code}]$. For the digital commands, this uses a P.P.M system of 16 bit code, which transmit the code twice (invert in the second time) to prevent operation by false codes. This IC is designed to be received with 4 bit CPU (DTS).

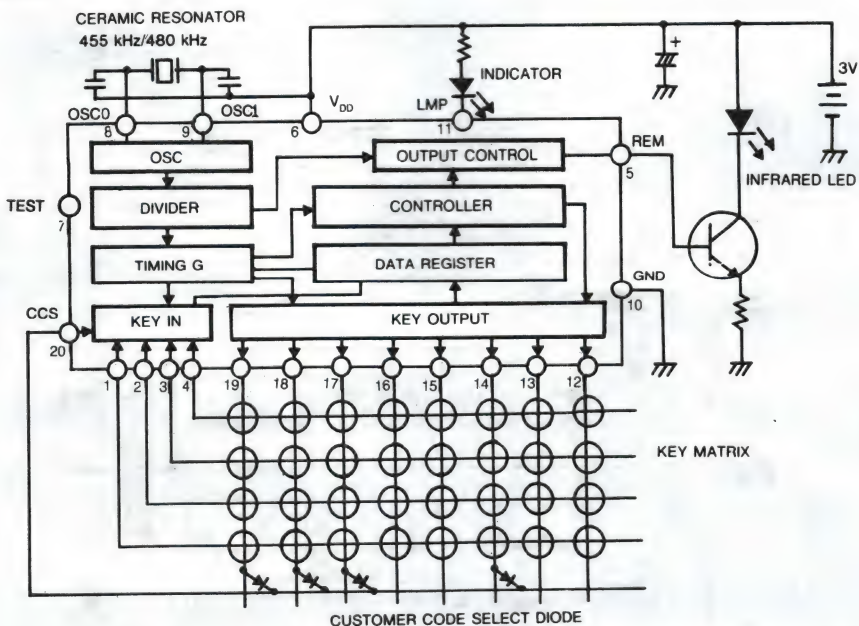
Features

- Low Voltage Operation $V_{DD} = 2.0 \sim 3.3V$
- Low Power Consumption ... $I_{DD} < 1 \mu A$ at Standby Mode
- 32 Function KEY and 3 dual Action KEY
- 256 Custom Codes Selected by External Diode
- 16 Bit Pulse Position Modulated Code
- High Efficiency Transmission IR LED on Duty 3%
- Indicator Output
- Package 20 SO Package

Pin Configuration



Block Diagram



Absolute Maximum Ratings ($T_a=25^{\circ}\text{C}$)

Supply Voltage	V_{DD-GND}	4.0	V
Input voltage	V_{IN-GND}	-0.3 to V_{DD}	V
Output Current	$I_{OH(REM, LMP)}$	-15.0	mA
Power Dissipation	P_d	250	mW
Operating Temperature Range	T_{opr}	-20~ +75	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-40~+125	$^{\circ}\text{C}$

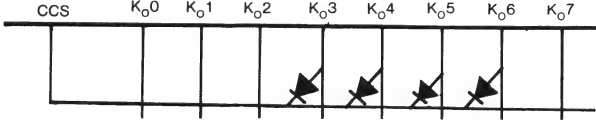
Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	2.0	3.0	3.3	V
Oscillation Frequency	f_{OSC}	400	455	500	kHz
Lamp Output Current	$I_{OL(LMP)}$		1		mA

Electrical Characteristics ($T_A=25^{\circ}\text{C}$, $V_{DD}=3.0\text{V}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Current	$I_{DD(OP)}$	$f_{OSC}=455\text{ kHz}$		0.1	1.0	mA
Supply Current	$I_{DD(ST)}$	$f_{OSC}=\text{STOP}$			1	μA
Input High Voltage	$V_{IH(KI)}$		0.7 V_{DD}		V_{DD}	V
Input Low Voltage	$V_{IL(KI)}$		0		0.3 V_{DD}	V
Input Pull Down R	$R_{(KI)}$		150	900	1500	$k\Omega$
Output Current	$I_{OH(REM)}$	$V_{OH(REM)}=1.5\text{V}$	-5			mA
Output Low Voltage	$V_{OL(LMP)}$	$I_{OL}=1.0\text{ mA}$			0.3	V

Pin Description

PIN NO.	SYMBOL	EXPLANATION
1~4	$K_0\sim K_3$	Key Input; Internally Pull-down to GND by Resister.
5	REM	Remote Output
6	V_{DD}	Positive Supply 2.0 to 3.3V
7	TEST	TEST Terminal Normally Open
8	OSCO	Oscillator Output Ceramic Resonator
9	OSCI	Oscillator Input (400 to 500 kHz)
10	LMP	LAMP Output Indicator for Transmission
11	GND	Ground
12~19	$K_0\sim K_7$	Key Output
20	CCS	<p>Custom Code Select Input</p> <p>Custom Code is selected by diode Connection to Key Output (K_0 to K_7)</p> <p>This terminal is usually pull up to V_{DD} by internal Resistor.</p>  <p>Custom Code Select</p> <p>Example C0 to C7 = 00011110</p>

Key Data Code

Key	CONNECTION					DATA CODE								REMARKS
	K _i 0	K _i 1	K _i 2	K _i 3	K _o	D0	D1	D2	D3	D4	D5	D6	D7	
K1	*				K _o 0	0	0	0	0	0	0	0	0	
K2		*				1	0	0	0	0	0	0	0	
K3			*			0	1	0	0	0	0	0	0	
K4				*		1	1	0	0	0	0	0	0	
K5	*				K _o 1	0	0	1	0	0	0	0	0	
K6		*				1	0	1	0	0	0	0	0	
K7			*			0	1	1	0	0	0	0	0	
K8				*		1	1	1	0	0	0	0	0	
K9	*				K _o 2	0	0	0	1	0	0	0	0	
K10		*				1	0	0	1	0	0	0	0	
K11			*			0	1	0	1	0	0	0	0	
K12				*		1	1	0	1	0	0	0	0	
K13	*				K _o 3	0	0	1	1	0	0	0	0	
K14		*				1	0	1	1	0	0	0	0	
K15			*			0	1	1	1	0	0	0	0	
K16				*		1	1	1	1	0	0	0	0	
K17	*				K _o 4	0	0	0	0	1	0	0	0	
K18		*				1	0	0	0	1	0	0	0	
K19			*			0	1	0	0	1	0	0	0	
K20				*		1	1	0	0	1	0	0	0	
K21	*				K _o 5	0	0	1	0	1	0	0	0	
K22		*				1	0	1	0	1	0	0	0	
K23			*			0	1	1	0	1	0	0	0	
K24				*		1	1	1	0	1	0	0	0	
K25	*				K _o 6	0	0	0	1	1	0	0	0	
K26		*				1	0	0	1	1	0	0	0	
K27			*			0	1	0	1	1	0	0	0	
K28				*		1	1	0	1	1	0	0	0	
K29	*				K _o 7	0	0	1	1	1	0	0	0	
K30		*				1	0	1	1	1	0	0	0	
K31			*			0	1	1	1	1	0	0	0	
K32				*		1	1	1	1	1	0	0	0	

Dual Action Key Code

KEY	D0	D1	D2	D3	D4	D5	D6	D7	REMARKS
K21 + K22	1	0	1	0	1	1	0	0	
K21 + K23	0	1	1	0	1	1	0	0	
K21 + K24	1	1	1	0	1	1	0	0	

Custom Code

EX:	D0	D1	D2	D3	D4	D5	D6	D7
	1	0	1	0	1	1	0	0

Operation of Dual Action Key

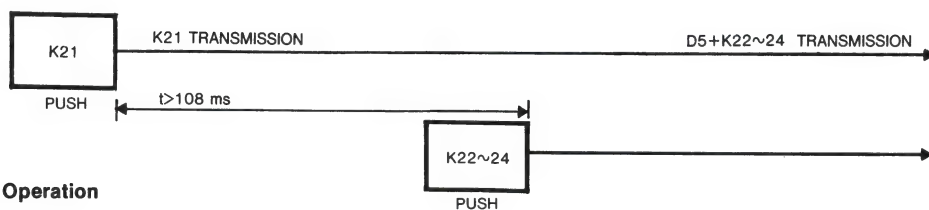
Keys (K21 to K24) are used for preventing failure caused by mistakes

Ex: Cassette Tape Recoder K21 REC KEY

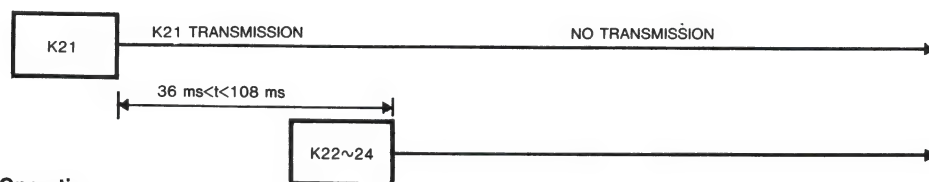
K22 PLAY KEY

KEY	D0	D1	D2	D3	D4	D5	D6	D7
K21 + K22	1	0	1	0	1	1	0	0
K21 + K23	0	1	1	0	1	1	0	0
K21 + K24	1	1	1	0	1	1	0	0

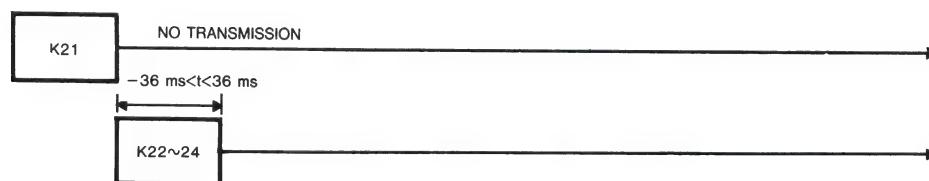
(a) Operation



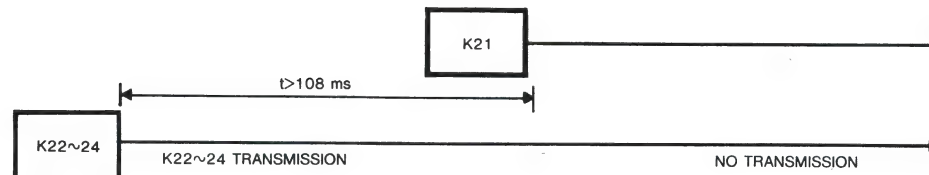
(b) No Operation



(c) No Operation



(d) No Operation





GM3044

CMOS REMOTE CONTROL TRANSMITTER

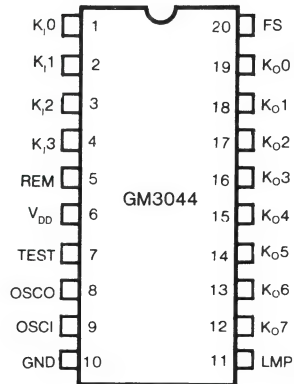
Description

The GM3044 is CMOS IC for control circuits of infrared remote control transmitter which are available for TV, STEREO, VTR and TOY etc.

For the digital commands, this use a P.P.M system of 16 bit code, which transmit the code twice (invert in the second time) to prevent operation by false codes.

This IC is designed to be received with 4 bit CPU(DTS).

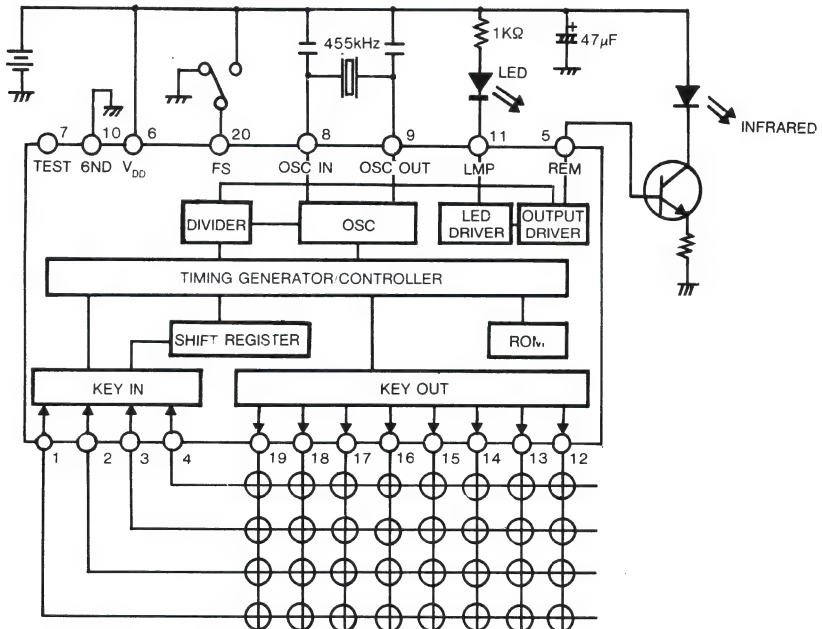
Pin Configuration



Feature

- Low Voltage Operation $V_{DD} = 2.0 \sim 3.3V$
- Frequency Select Terminal is Attached
- LED Driver for TX is Included
- 32 Function Key (8×4 key Matrix)
- Custom Code is Included
- 16 bit Pulse Position Modulated Code
- Custom Code Select Diode is not Necessary
- Package 20 SO Package

Block Diagram



Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Supply Voltage	V_{DD-GND}	4.0	V
Power Dissipation	P_d	500	mW
Operating Temperature Range	T_{opr}	-20 to +75	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to +125	$^\circ\text{C}$

Electrical Characteristics ($T_a=25^\circ\text{C}$, $V_{DD}=3.0\text{V}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		2.0	3.0	3.3	V
Supply Current	$I_{DD(OP)}$	$f_{OSC}=455\text{ kHz}$		0.1	1.0	mA
Supply Current	$I_{DD(ST)}$				1	μA
Input High Voltage	$V_{IH(KI)}$	PIN 1~4	$0.7 V_{DD}$		V_{DD}	V
Input Low Voltage	$V_{IL(KI)}$	PIN 1~4	0		$0.3 V_{DD}$	V
Input Pull Down R	$R_{(KI)}$	PIN 1~4	150	900	1500	$k\Omega$
Output Current	$I_{OH(REM)}$	$V_{OH(REM)}=1.5\text{ V}$	6	15	—	mA
Lamp Output Current	$I_{OL(LMP)}$	$V_{OL(LMP)}=0.3\text{ V}$	1	2	—	mA

Pin Description

PIN NO.	SYMBOL	DESCRIPTION
1~4	$K_1O\sim K_3$	Key Input; Internally Pull-down to GND by Resistor.
5	REM	Remote Output
6	V_{DD}	Positive Supply ... 2.0 to 3.3V
7	TEST	Normaly "H" state, due to Internal Pull-up Resistor to V_{DD} . In order to test, set to "L" state.
8	OSC0	Oscillator Output Ceramic Resonator
9	OSC1	Oscillator Input (400 to 500 kHz)
10	GND	Ground
11	LMP	LAMP Output Indicator for Transmission
12~19	$K_0O\sim K_7$	Key Output As Time of 36ms has passed after key-push, REM Output is transmitted.
20	FS	Frequency Select When set to "H" state, the basic frequency is reduced to half the normal one. Therefore, 64 function keys can be available. When used as 32 function key mode, set to "L" state.

Key Data Code

Key	CONNECTION					DATA CODE							
	K ₀	K ₁	K ₂	K ₃	K ₀	D0	D1	D2	D3	D4	D5	D6	D7
K1	*				K ₀₀	0	0	0	0	0	0	0	0
K2		*				1	0	0	0	0	0	0	0
K3			*			0	1	0	0	0	0	0	0
K4				*		1	1	0	0	0	0	0	0
K5	*				K ₀₁	0	0	1	0	0	0	0	0
K6		*				1	0	1	0	0	0	0	0
K7			*			0	1	1	0	0	0	0	0
K8				*		1	1	1	0	0	0	0	0
K9	*				K ₀₂	0	0	0	1	0	0	0	0
K10		*				1	0	0	1	0	0	0	0
K11			*			0	1	0	1	0	0	0	0
K12				*		1	1	0	1	0	0	0	0
K13	*				K ₀₃	0	0	1	1	0	0	0	0
K14		*				1	0	1	1	0	0	0	0
K15			*			0	1	1	1	0	0	0	0
K16				*		1	1	1	1	0	0	0	0
K17	*				K ₀₄	0	0	0	0	1	0	0	0
K18		*				1	0	0	0	1	0	0	0
K19			*			0	1	0	0	1	0	0	0
K20				*		1	1	0	0	1	0	0	0
K21	*				K ₀₅	0	0	1	0	1	0	0	0
K22		*				1	0	1	0	1	0	0	0
K23			*			0	1	1	0	1	0	0	0
K24				*		1	1	1	0	1	0	0	0
K25	*				K ₀₆	0	0	0	1	1	0	0	0
K26		*				1	0	0	1	1	0	0	0
K27			*			0	1	0	1	1	0	0	0
K28				*		1	1	0	1	1	0	0	0
K29	*				K ₀₇	0	0	1	1	1	0	0	0
K30		*				1	0	1	1	1	0	0	0
K31			*			0	1	1	1	1	0	0	0
K32				*		1	1	1	1	1	0	0	0

Dual Action Key Code

KEY	D0	D1	D2	D3	D4	D5	D6	D7
K21 + K22	1	0	1	0	1	1	0	0
K21 + K23	0	1	1	0	1	1	0	0
K21 + K24	1	1	1	0	1	1	0	0

ROM Data for Custom Code

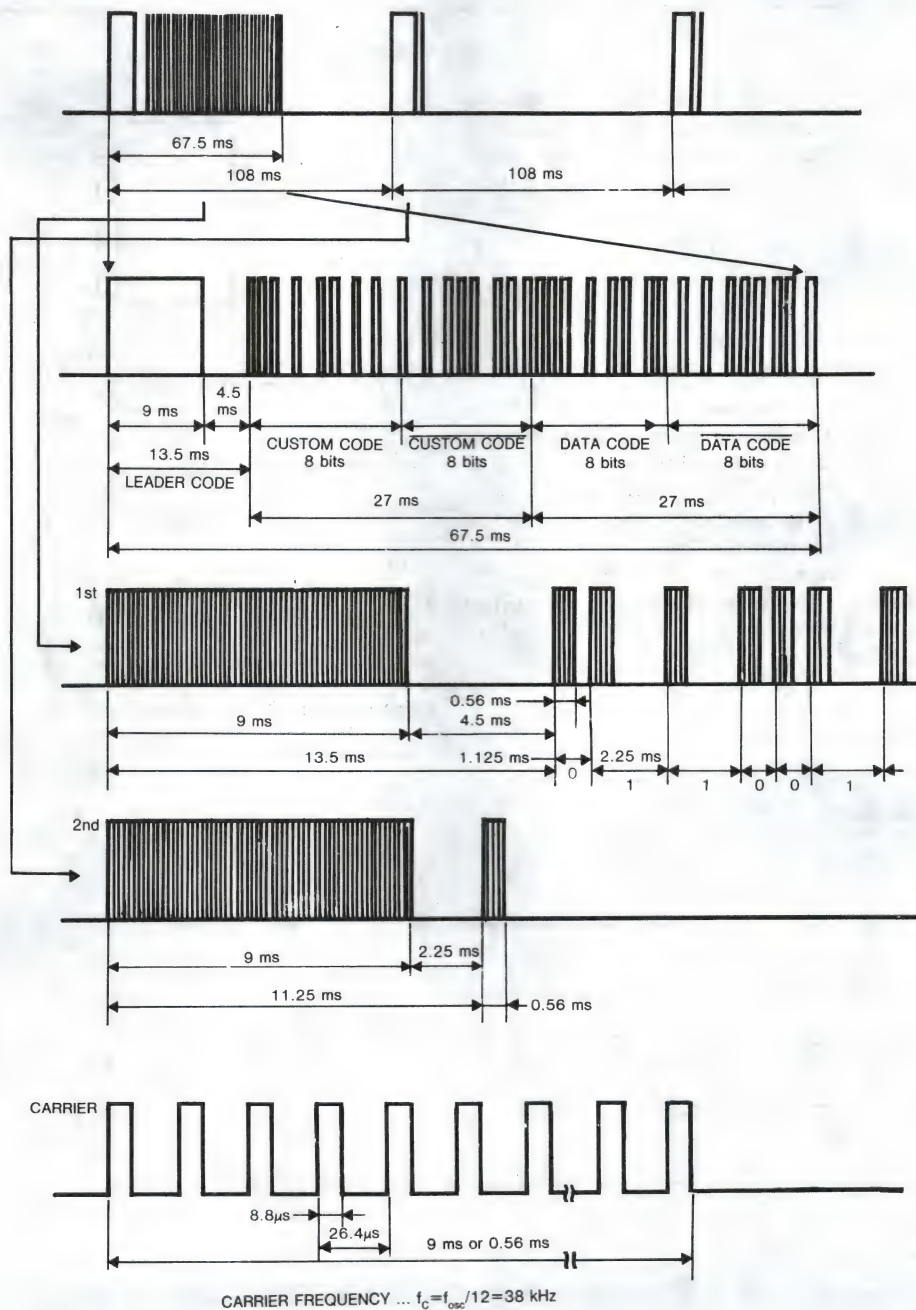
EX:

C0	C1	C2	C3	C4	C5	C6	C7
0	1	1	1	0	1	1	0

Remote Output Waveforms

* For $f_{osc} = 455\text{kHz}$, FS="L",

* For FS="H", time is doubled



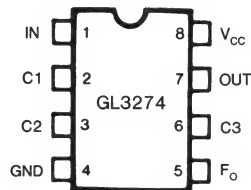
GL3274

Preamplifier for Remote Control Use

Description

The GL3274 is a bipolar IC for receiving preamplifier of infrared remote control system. It is comprised of a primary stage amplifier, limiter amplifier, BPF, signal waveform detecting circuit, waveform shaping circuit, etc.

Pin Configurations



Features

- Low Power Consumption ($V_{CC}=5V$, 9 mW typ.)
- Low Power Supply Voltage ($V_{CC}=5V$)
- Built-in Filter(Enables to Vary Center frequency with an Externally Attached Resistor.
 $f_o = 30 \text{ kHz to } 60 \text{ kHz}$, 40 kHz typ.)
- It is free from Inductance due to Magnetic Field Since it uses no Inductance Coil.
- Possible to Direct Connection to a Photodiode
- Open Collector Output(Possible to Direct Connection to TTL and CMOS)
- Package 8 SIP(A) or 8SOP(D)

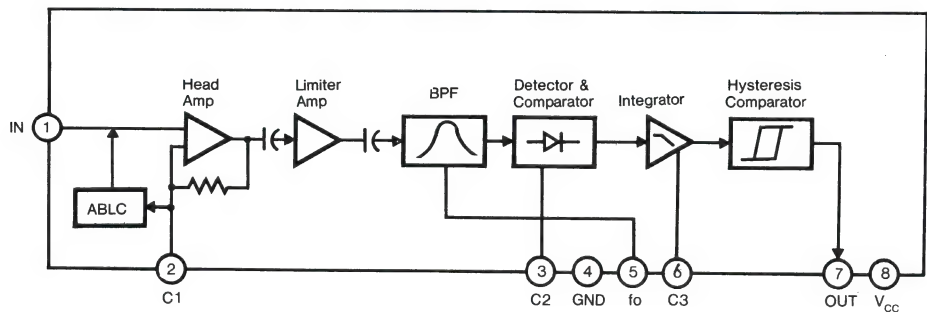
Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

Supply Voltage	V_{CC}	17	V
Input Voltage	V_{IN}	5	V_{p-p}
Operation Temperature	T_{opr}	-20 to +75	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Allowable Power Dissipation	P_D	0.6 (A) 0.3 (D)	W

Recommended Operating Condition

Supply Voltage	V_{CC}	4.7 to 5.3	V
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Block Diagram



Electrical Characteristics: $V_{CC}=5V$, $T_A=25^{\circ}C$

No.	Item	Symbol	Test condition			Test Point	Min.	Typ.	Max.	Unit	Remark
			Signal	Level	ON-SW						
1	Input pin voltage (1)	V_{IN1}			S1, 8, 11-a	A	2.0	2.5	3.1	V	
2	Input pin voltage (2)	V_{IN2}			S1, 2, 4, 8, 11-a	A	0.6	1.0	1.7	V	
3	L Level output voltage	V_{OL}			S3, 7-a, 10, 11-a	D	—	0.2	0.4	V	
4	Output leakage current	I_{OH}			S3, 7-b, 9, 11-a	C	—	0	2.2	μA	
5	Voltage gain	A_V	40 kHz cw		$50\mu V_{p-p}$ S2, 5, 6, 7-c, 11-a	B	74	79	84	dB	
6	BPF characteristics	A_{VO}	30kHz, 37 kHz, 43kHz, 50kHz cw		$50\mu V_{p-p}$ S2, 5, 6, 7-c, 11-a	B	4	9	—	dB	*1
7	Input impedance	r_{in}	40kHz cw		$0.2 V_{p-p}$ S1, 2, 6, 8, 11-a	A	27	40	55	k Ω	Input level denotes V_i and measured value V_x . *2
8	Detecting ability (1)	V_{in1}	burst wave		$60\mu V_{p-p}$ S2, 5, 6, 8, 10, 11-a	D	440	540	770	μs	Input a burst wave signal of 1.2 mS cycle, 40 kHz.
9	Detecting ability (2)	V_{in2}	burst wave		$50mV_{p-p}$ S2, 5, 6, 8, 10, 11-b	D	440	660	770	μs	Input a burst wave signal of 1.2 mS cycle, 40 kHz.
10	Consumption current	I_{CC}			S3, 8, 11-a	E	1.0	1.8	2.8	mA	

Note: *1 The level ratio between AC level of during 37 kHz and that of 30 kHz denotes A1 [dB].

$$A1 \equiv 20 \log \frac{\text{measure value (f=37 kHz)}}{\text{measure value (f=30 kHz)}}$$

The level ratio between AC level of during 43 kHz and that of 50 kHz denotes A2 [dB].

$$A2 \equiv 20 \log \frac{\text{measure value (f=43 kHz)}}{\text{measure value (f=50kHz)}}$$

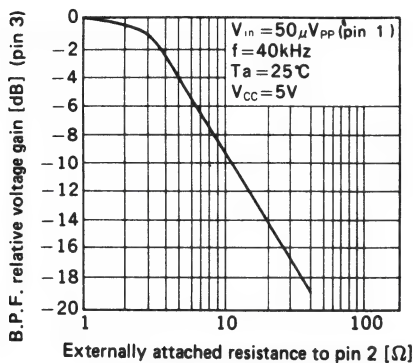
Note: *2 $r_{in} \equiv \frac{47 \text{ k}\Omega}{\frac{V_i}{V_x} - 1} [\text{k}\Omega]$

Pin Description: Pin voltages are depended on the DC Characteristics Test Circuit.

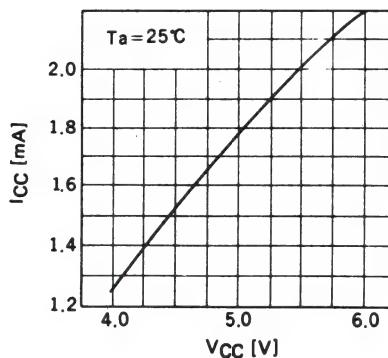
No.	Symbol	Voltage	Equivalent circuit	Description
1	IN	2.5V		<p>An input pin.</p> <p>Connect a photodiode with PIN structure between the pin and GND.</p>
2	C1	2.5V		<p>Connect a resistor and capacitor in series between the pin and GND and set the frequency characteristics and gain of the "Head amp".</p> <p>When the resistance is large and capacitance is small, the gain becomes small.</p> <p>When the capacitance is large, the sensitivity is lowered against the transient response.</p>
3	C2	1.5V		<p>Connect a detection capacitor between the pin and GND.</p> <p>When the capacitance is large, the sensitivity becomes lowered against the mean value detection wave and transient response.</p> <p>When the capacitance is small, fluctuation of the peak detection wave and output pulse width becomes large.</p> <p>The capacitor to be used is of standard $3.3 \mu\text{F}$, however, set it so that the output pulse width fluctuation and noise elimination characteristics become optimum.</p>
4	GND			<p>An GND pin of the IC.</p> <p>Make the pattern design so that the parts to be attached externally will be located as closely as possible to this pin and to be grounded them at the same one point.</p> <p>The reaching distance and noise elimination characteristics are greatly influenced by the pattern design of around the GND.</p>
5	fo	1.4V		<p>Connect a resistor between the pin and the power supply.</p> <p>Set the center frequency of the built-in BPF.</p> <p>See "Pin 5 externally attached resistor vs, Center frequency characteristics".</p>

No.	Symbol	Voltage	Equivalent circuit	Description
6	C3	1.0V		<p>Connect an integral capacitor between the pin and GND.</p> <p>Connect an integral capacitor of standard 330 pF.</p> <p>When a large capacitance is used, it becomes strong against disturbance noise and the low level section of the output pulse becomes longer. However, if the capacitance becomes too large, the reaching distance becomes shorter.</p>
7	OUT	5.0V		<p>An open-collector output. Connect a loading resistor between this pin and the power supply.</p> <p>It should be low level standard of 0.2V when using a loading resistor of 2.2kΩ.</p>
8	V _{CC}	5.0V		The power supply voltage pin.

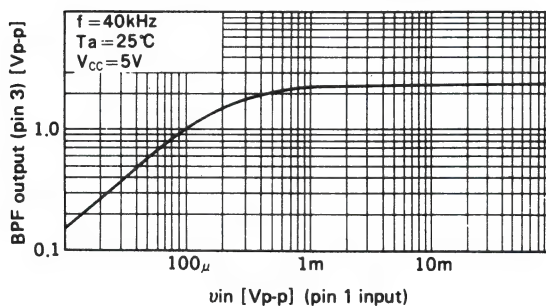
**A_v characteristics vs.
Externally attached resistance to pin 2**



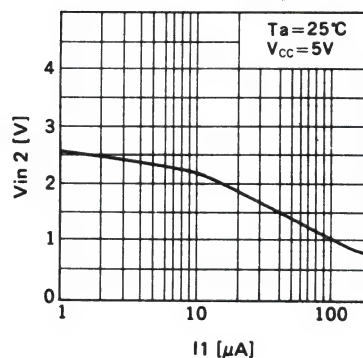
I_{CC} vs. V_{CC} characteristics



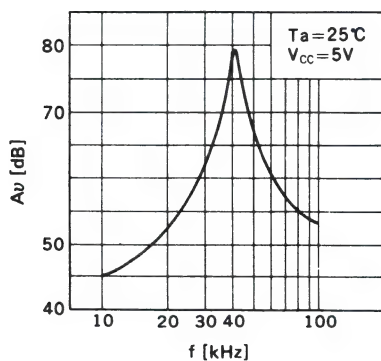
**Pin 3 output voltage characteristics vs.
Pin 1 input voltage**



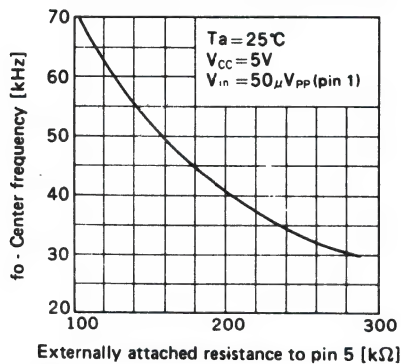
V_{in2} vs. I_1 characteristics



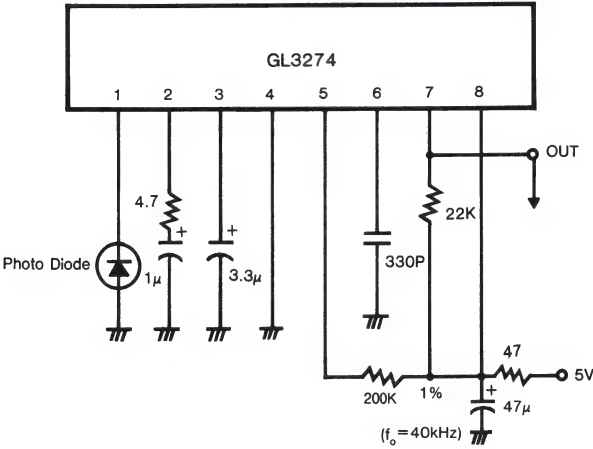
A_v vs. f characteristics



**Center frequency characteristics
vs.
Externally attached resistance**



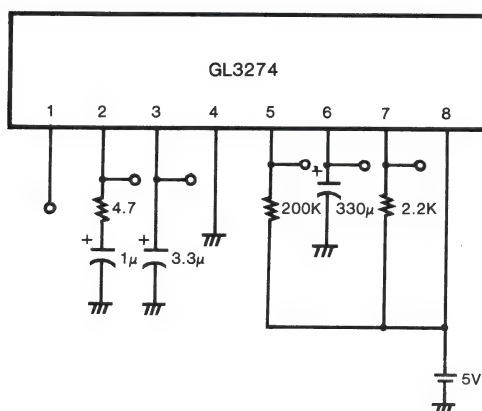
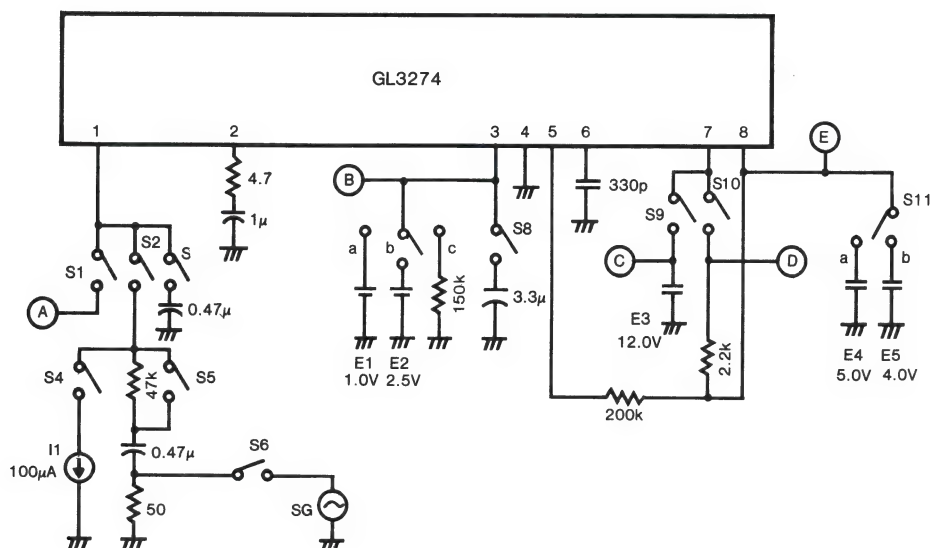
Application Circuit



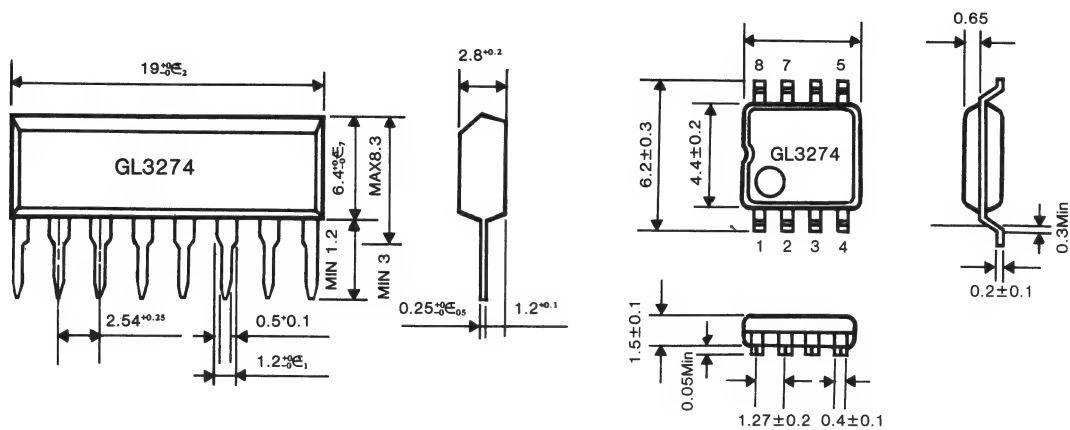
Description of Operation (See the Block Diagram)

Receive the infrared signal transmitted from the infrared remoted control commander with a photodiode and output rectangular waves as an output.

I/O pin	Waveform	Operation
Pin 1 input waveform		Converts the signal current of a photodiode into voltage and amplifies it.
BPF output waveform (Pin 3)		Suppresses the noise component with BPF.
Pin 6 Hysteresis Comparator input waveform		Detects the signal component and performs wave detection.
Pin 7 output waveform		Integrates the signal component and makes it as rectangular wave output from the Hysteresis Comparator.



Output Dimension



	DATA SHEET INDEX	
	QUALITY ASSURANCE MANUAL	
1.	TV APPLICATION	
2.	VCR APPLICATION	
3.	AUDIO APPLICATION	
4.	TELECOM APPLICATION	
5.	REMOTE CONTROL APPLICATION	
6.	INDUSTRY APPLICATION	
	GOLDSTAR SEMICONDUCTOR SALES NETWORK	

GL324/324A

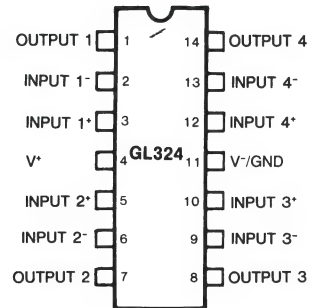
QUAD OPERATIONAL AMPLIFIER

Description

The GL324 consists of four independent high gain, internally frequency compensated operational amplifiers which were specifically to operate from a single power supply over a wide range of voltages and the power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, gain blocks and all the conventional OP AMP circuits which now can be more easily implemented in single power systems.

Pin Configuration



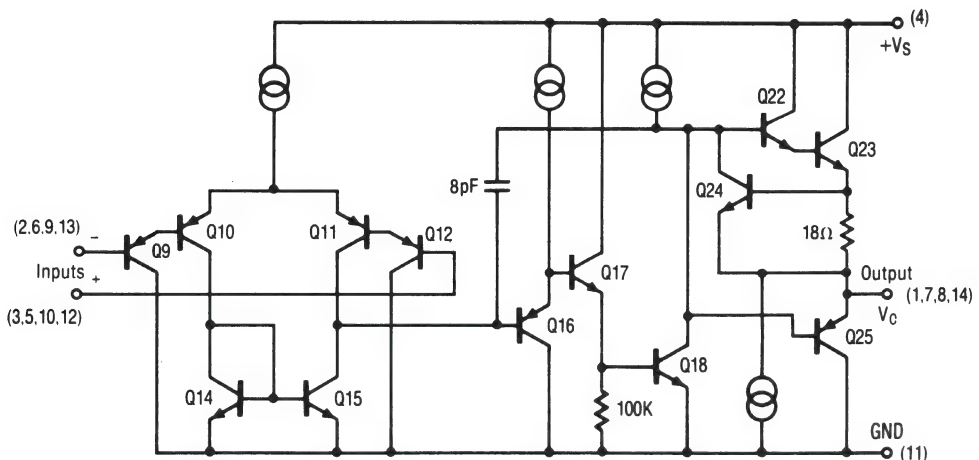
Features

- Input Common mode Voltage Range Includes Ground.
- Wide Power Supply Range. (Single or Dual Supply) 3V to 32V or $\pm 1.5V$ to $\pm 16V$
- Large Output Voltage Swing. 0V to $V^+ - 1.5V$
- Internally Frequency Compensated for Unity Gain.
- Low Input Bias Current.
- Low Input Offset Voltage.
- Very Low Supply Current Drain.

Absolute Maximum Ratings

Supply Voltage, V^+	32	or ± 16	V
Differential Input Voltage	± 32		V
Input Voltage	-0.3	to 32	V
Power Dissipation	670		mW
Operating Temperature Range	0	to 70	$^{\circ}C$
Storage Temperature Range	-55	to 125	$^{\circ}C$
Lead Temperature	260		$^{\circ}C$

Schematic-Diagram (Each Amplifier)



Electrical Characteristics:

Unless otherwise specified, these specification apply for $V^+=5V$, $V^+ \text{ Max}=30V$ and $0^\circ C \leq T_A \leq 70^\circ C$

PARAMETER	SYMBOL	TEST CONDITIONS		GL324			GL324A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	$V^+=5V$ to Max, $V_O=1.4V$, $R_S=0\Omega$ $V_{ICR}=0V$ to $V^+-1.5V$ $T_A=25^\circ C$			± 2	± 7 ± 9		± 2	± 3 ± 5	mV
Input Offset Current	I_{IO}	$I_{IN(+)} - I_{IN(-)}$, $V_O=1.4V$ $T_A=25^\circ C$			± 5	± 50 ± 150		± 5	± 30 ± 75	nA
Input Bias Current	I_{IB}	$I_{IN(+)}$ or $I_{IN(-)}$, $V_O=1.4V$ $T_A=25^\circ C$			45 40	250 500		45 40	100 200	nA
Input Common-Mode Voltage range	V_{ICR}	$V^+=5V$ to Max $T_A=25^\circ C$		0 to $V^+-1.5V$ $V^+-2.0V$			0 to $V^+-1.5V$ $V^+-2.0V$			V
Supply Current	I^+, I^-	$R_L = \infty$	$V^+=5V$, $V_O=2.5V$		0.7	1.2		0.7	1.2	mA
			$V^+=\text{Max}$, $V_O=15V$		1.5	3		1.5	3	
Large-Signal Voltage Gain	A_{VD}	$V^+=15V$, $R_L \geq 2K\Omega$ $V_O=-5V$ to $+5V$ $T_A=25^\circ C$		25 15	100		25 15	100		V/mV
Output Voltage Swing	V_{OH}	$V^+=\text{MAX}$	$R_L=2K\Omega$	26			26			V
	V_{OL}		$R_L \geq 10K\Omega$	27	28		27	28		
Common Mode Rejection Ratio	CMRR	$T_A=25^\circ C$ $V^+=5V$ to Max		65	70		65	85		dB
Power Supply Rejection Ratio	PSRR	$V^+=5V$ to Max $T_A=25^\circ C$		65	100		65	100		dB
Output Current	Source	$V_{IN(+)}=1V$, $V_{IN(-)}=0V$ $T_A=25^\circ C$ $V^+=15V$, $V_O=4V$		20	40		20	40		mA
	Sink	$V^+=15V$	$V_O=15V$	10	20		10	20		mA
		$V_{IN(-)}=1V$ $V_{IN(+)}=0V$ $T_A=25^\circ C$	$V_O=200mV$	12	50		12	50		μA
Short Circuit Current	I_{OS}	$V^+=5V$ $T_A=25^\circ C$ $V_O=0V$			40	60		40	60	mA
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$				7			7		$\mu V/^\circ C$
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$				10			10		pA/°C

Typical Performance Curves

Figure 1 — Input Voltage Range

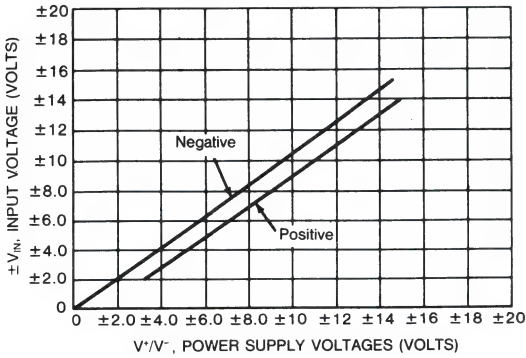
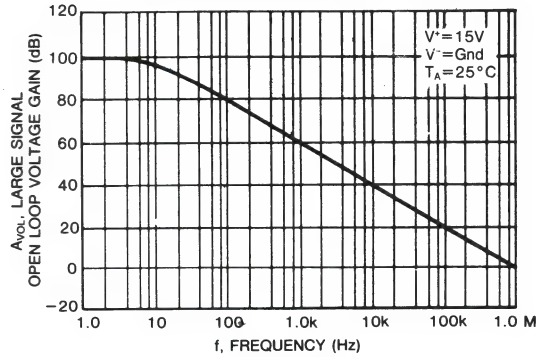


Figure 2 — Open Loop Response



Figures 3 — Large Signal Frequency Response

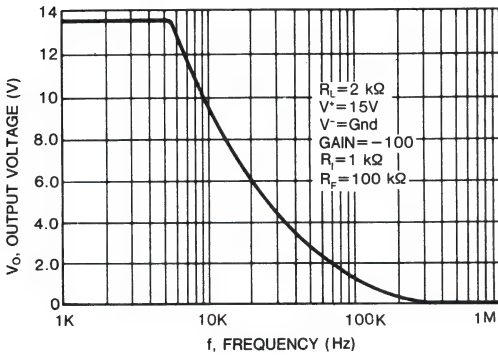


Figure 4 — Small Signal Voltage Follower Pulse Response (Non-Inverting)

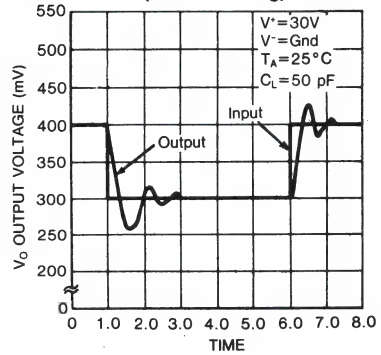


Figure 5 — Supply Current Versus Supply Voltage

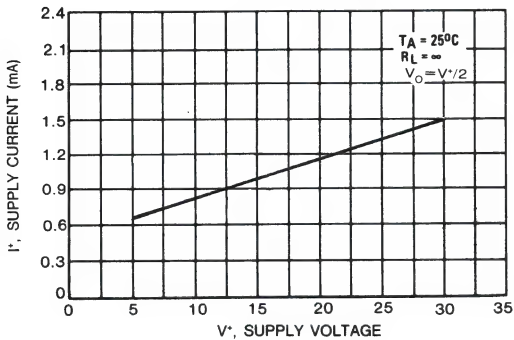
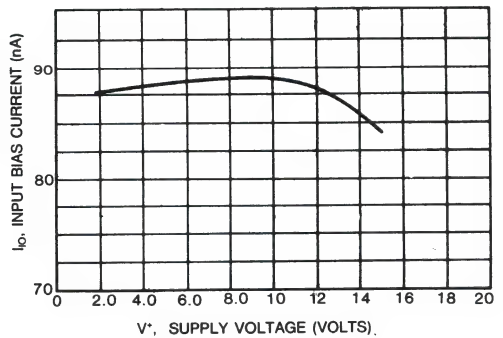


Figure 6 — Input Bias Current Versus Supply Voltage



Typical Application

Figure 1 — Function Generator

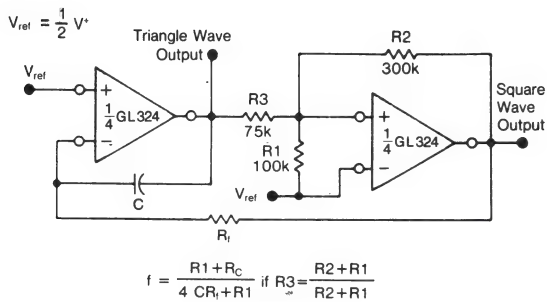


Figure 2 — Wien Bridge Oscillator

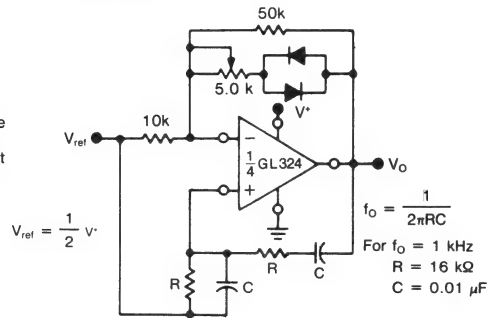


Figure 3 — High Impedance Differential Amplifier

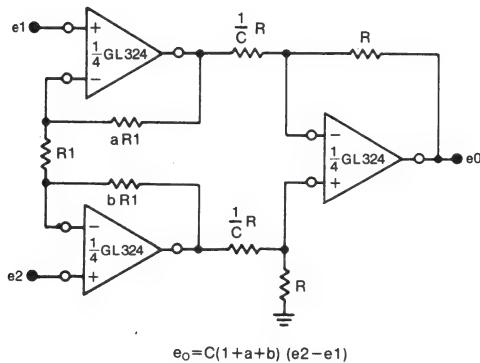


Figure 4 — Comparator With Hysteresis

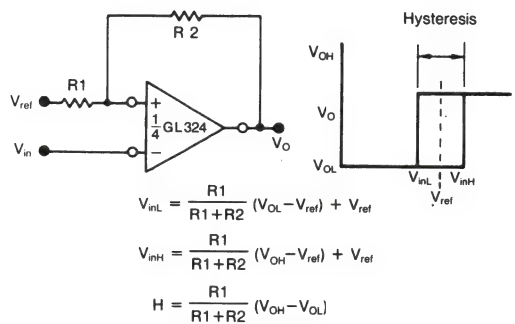
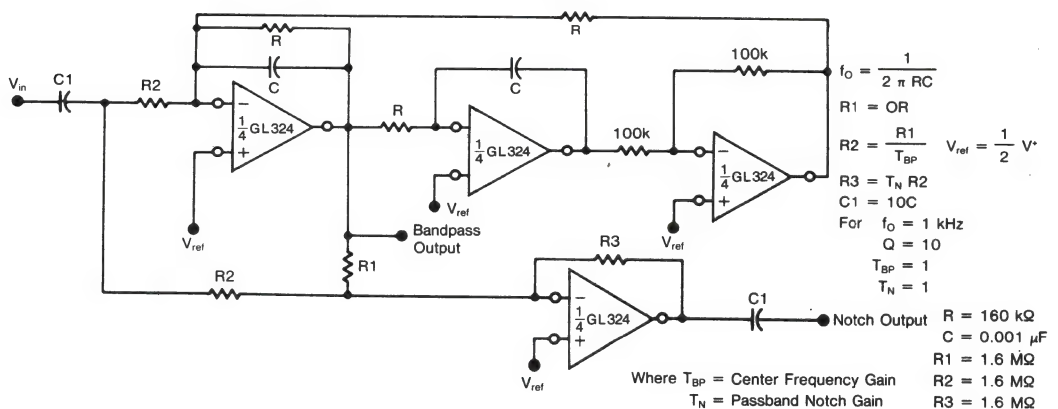


Figure 5 — Bi-Quad Filter



GL348

QUAD OPERATIONAL AMPLIFIER

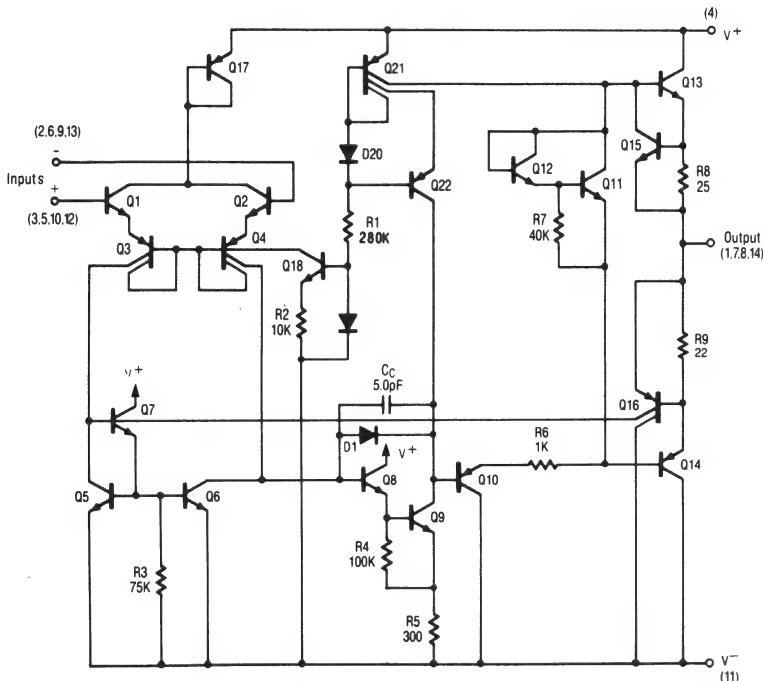
Description

The GL348 is a true quad 741. It consists of four independent high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single 741 type of amp. Other features include input offset currents and input bias currents which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

Features

- 741 Op Amp Operating Characteristics
- Low Supply Current Drain — 0.6 mA/Amplifier
- Class AB Output Stage — No Crossover Distortion.
- Pin Compatible With the GS324
- Low Input Offset Voltage — 1.0mV Typ.
- Low Input Offset Current — 4.0nA Typ.
- Low Input Bias Current — 30nA Typ.
- Gain Bandwidth Product (Unity Gain) — 1.0MHz Typ.
- High Degree of Isolation Between Amplifiers — 120dB
- Overload Protection for Inputs and Outputs

Schematic Diagram (Each Amplifier)



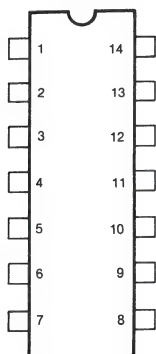
Absolute Maximum Ratings

PARAMETER	VALUE	UNIT
Supply Voltage	± 18	V
Differential Input Voltage	± 36	V
Input Voltage	± 18	V
Power Dissipation At 25°C	700	mW

PARAMETER	VALUE	UNIT
Operating Temperature Range	0 to 70	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (10 SEC)	260	°C

Electrical Characteristics ($V^+ = \pm 15V$, $T_A = +25^\circ\text{C}$ unless otherwise specified)

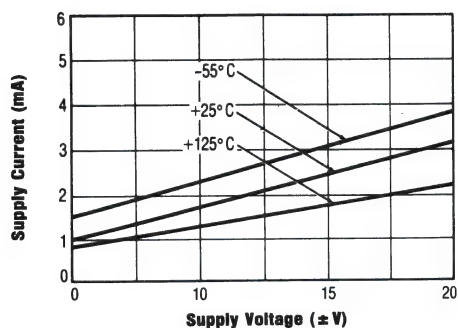
PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_s \leq 10k\Omega$		1.0	6.0	mV
Input Offset Current			4.0	50	nA
Input Bias Current			30	200	nA
Input Resistance (Differential Mode)		0.8	2.5		M Ω
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25	160		V/mV
Output Voltage Swing	$R_L = 10k\Omega$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	± 12	± 13		V
	$R_L = 2k\Omega$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	± 10	± 12		
Input Voltage Range	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	± 12			V
Common Mode Rejection Ratio	$R_s \leq 10k\Omega$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	70	90		dB
Power Supply Rejection Ratio	$R_s \leq 10k\Omega$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	77	96		dB
Short Circuit Current			25		mA
Supply Current (All Amps)			2.4	4.5	mA
Input Offset Voltage	$R_s \leq 10k\Omega$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$			7.5	mV
Input Offset Current	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$			100	nA
Input Bias Current	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$			400	nA
Slew Rate	$R_L \geq 2k\Omega$		0.5		V/ μS
Channel Separation	$f = 10\text{kHz}$, $R_s = 1k\Omega$, Gain = 100		120		dB
Unity Gain Bandwidth	Gain = 1		1.0		MHz

Pin Configuration

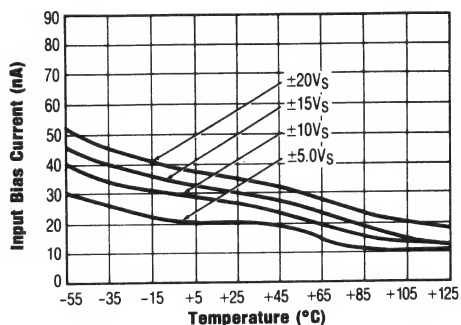
Pin	Function
1	Output A
2	- $V_{IN A}$
3	+ $V_{IN A}$
4	+ V_S
5	$V_{IN B}$
6	- $V_{IN B}$
7	Output B
8	Output C
9	- $V_{IN C}$
10	+ $V_{IN C}$
11	- V_S
12	+ $V_{IN D}$
13	- $V_{IN D}$
14	Output D

Typical Performance Characteristics

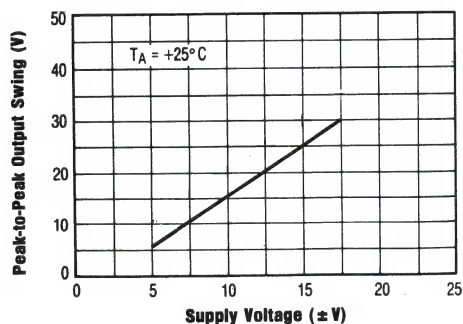
Supply Current vs. Supply Voltage



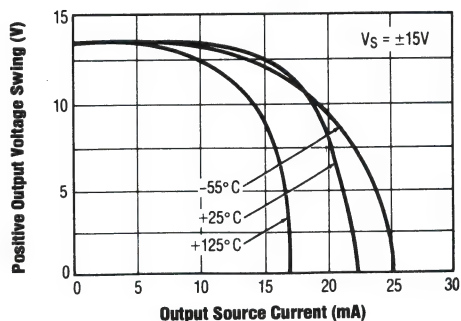
Input Bias Current vs. Temperature



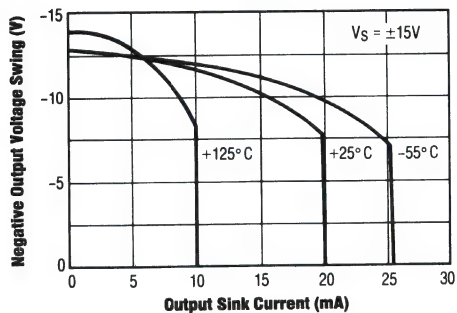
Output Voltage Swing vs. Supply Voltage



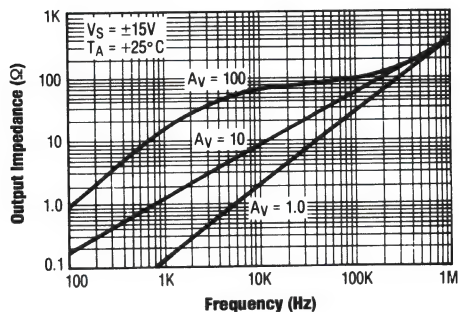
Positive Current Limit



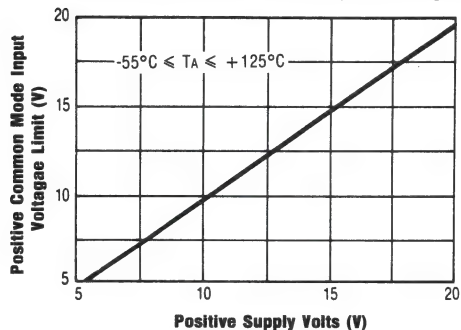
Negative Current Limit



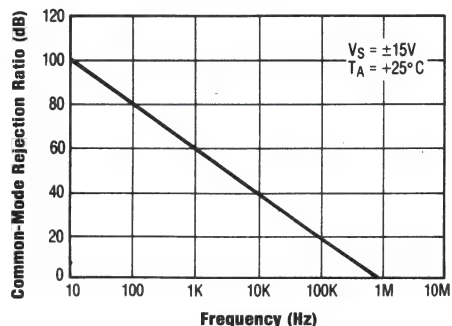
Output Impedance vs. Frequency



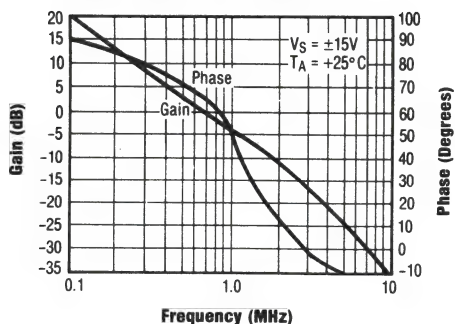
Positive Common Mode Input Voltage Limit



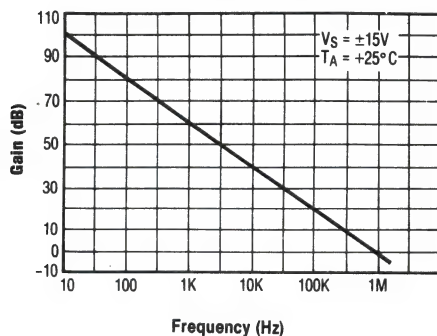
Common Mode Rejection Ratio vs. Frequency



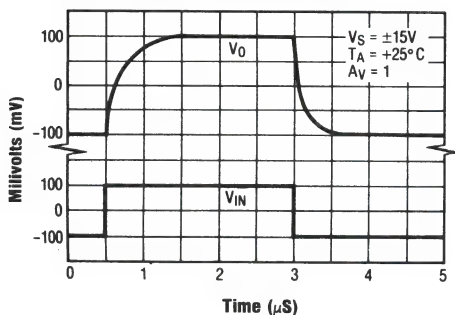
Phase Margin vs. Frequency



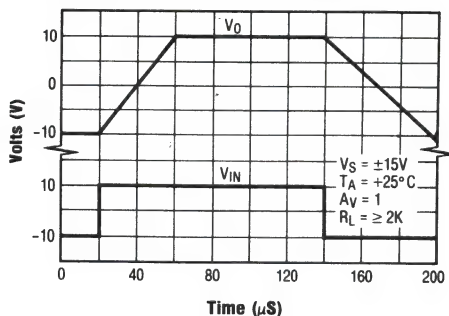
Open Loop Frequency Response vs. Frequency



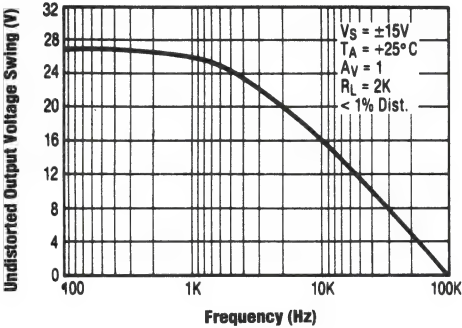
Small Signal Pulse Response



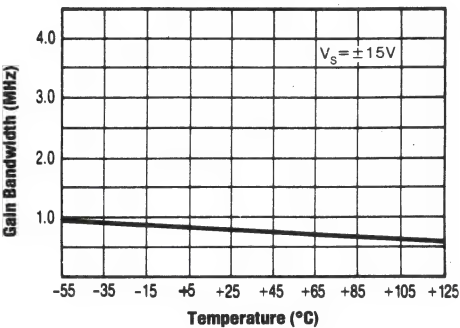
Large Signal Pulse Response



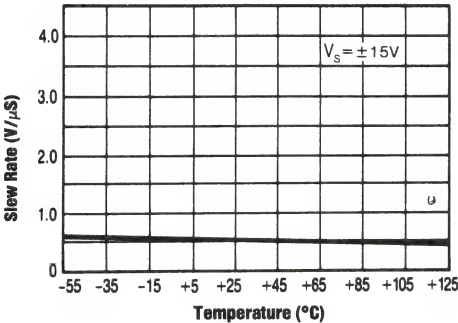
Undistorted Output Voltage Swing
vs. Frequency



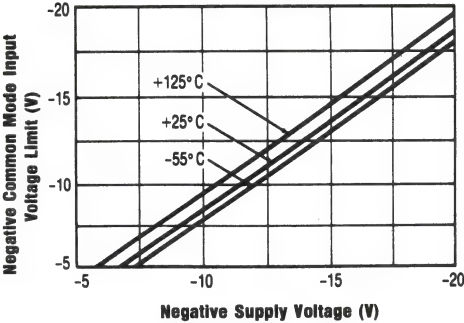
Gain Bandwidth vs. Temperature



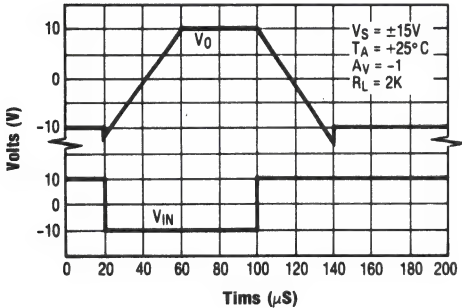
Slew Rate vs. Temperature



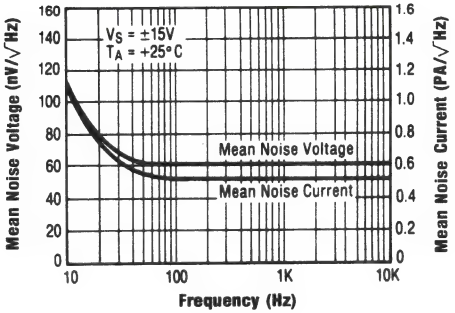
Negative Common Mode
Input Voltage Limit



Inverting Large Signal Pulse Response



Input Noise Voltage and Noise Current



Typical Applications

The GL348 is low power quad operational amplifiers that exhibit performance comparable to the popular 741. Substitution can therefore be made with no change in circuit behavior.

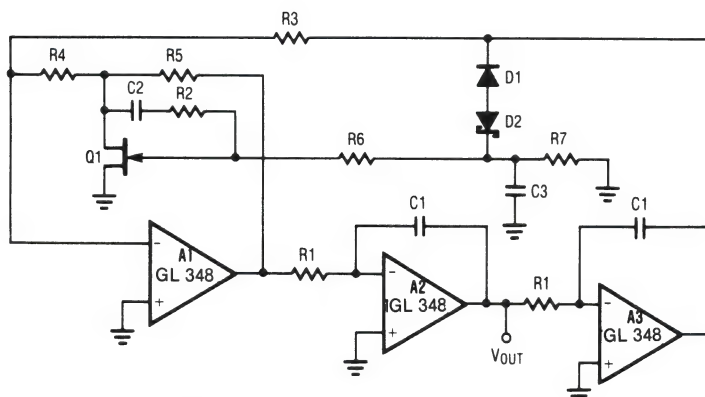
The input characteristics of these devices allow differential voltages which exceed the supplies. Output phase will be correct as long as one of the inputs are within the operating common mode range. If both exceed the negative limit, the output will latch positive. Current limiting resistors should be used on the inputs in case voltages become excessive.

When capacitive loading becomes much greater than 100pF, a resistor should be placed between the output and feedback connection in order to reduce phase

shift.

The GL348 is short circuit protected to either ground or the supplies continuously when only one of the four amplifiers is shorted. If multiple shorts occur simultaneously, the unit can be destroyed due to excessive power dissipation.

To assure stability and to minimize pickup, feedback resistors should be placed close to the input to maximize the feedback pole frequency (a function of input to ground capacitance). A good rule of thumb is that the feedback pole frequency should be 6 times the operating -3.0dB frequency. If less, a lead capacitor should be placed between the output and input.



$$f = \frac{1}{2\pi R_1 C_1} \times \sqrt{K}, K = \frac{R_4 R_5}{R_3} \left(\frac{1}{r_{DS}} + \frac{1}{R_4} + \frac{1}{R_5} \right) \cdot r_{DS} \approx \left(\frac{R_{ON}}{1 - \frac{V_{GS}}{V_P}} \right)^{1/2}$$

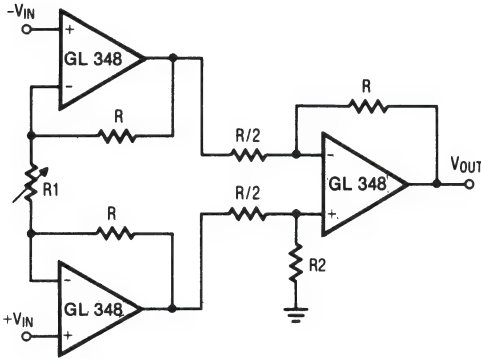
$f_{MAX} = 5.0\text{kHz}$, $THD \leq 0.03\%$

$R_1 = 100\text{K pot.}$, $C_1 = 0.0047\mu\text{F}$, $C_2 = 0.01\mu\text{F}$, $C_3 = 0.1\mu\text{F}$, $R_2 = R_6 = R_7 = 1\text{M}$, $R_3 = 5.1\text{K}$, $R_4 = 12\Omega$.

$R_5 = 240\Omega$, $Q_1 = \text{NS5102}$, $D_1 = 1\text{N914}$, $D_2 = 3.6\text{V avalanche diode (ex. LM103)}$, $V_S = \pm 15\text{V}$

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Figure 1. One Decade Low Distortion Sinewave Generator



$$V_{OUT} = 2 \left(\frac{2R}{R1} + 1 \right), -V_S - 3V \leq V_{IN CM} \leq +V_S - 3V,$$

$$V_S = \pm 15V$$

R = R2, trim R2 to boost CMRR

Figure 3. Low Cost Instrumentation Amplifier

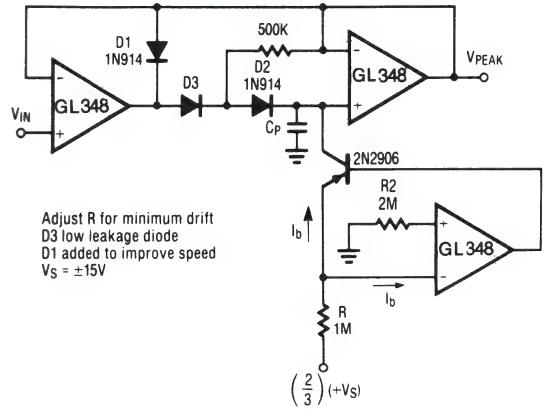


Figure 4. Low Voltage Peak Detector With Bias Current Compensation

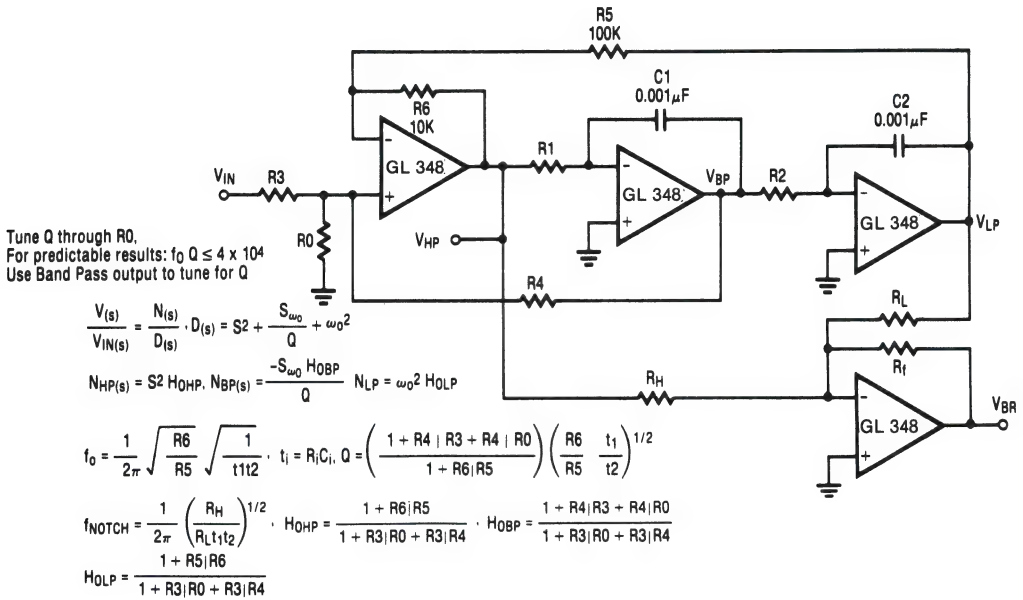
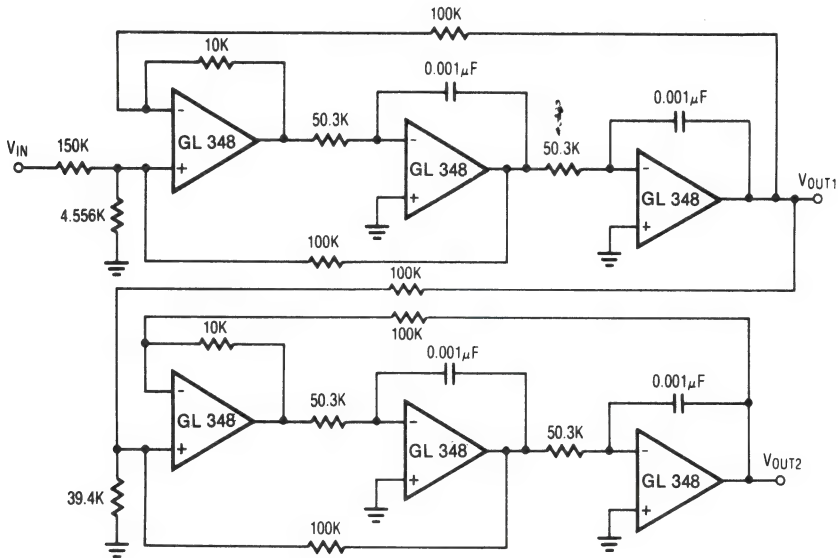
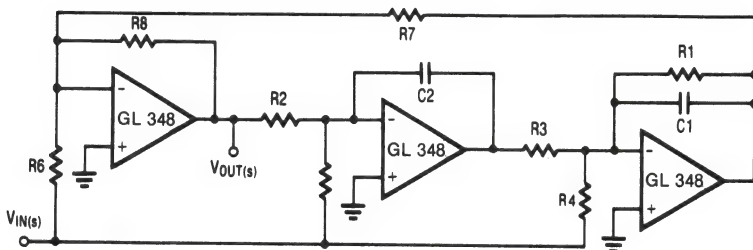


Figure 5. Universal State-Space Filter



Use general equations, and tune each section separately
 $Q_{1st} \text{ Section} = 0.541$, $Q_{2nd} \text{ Section} = 1.306$
 The response should have 0dB peaking

Figure 6. 1kHz 4 Pole Butterworth Filter



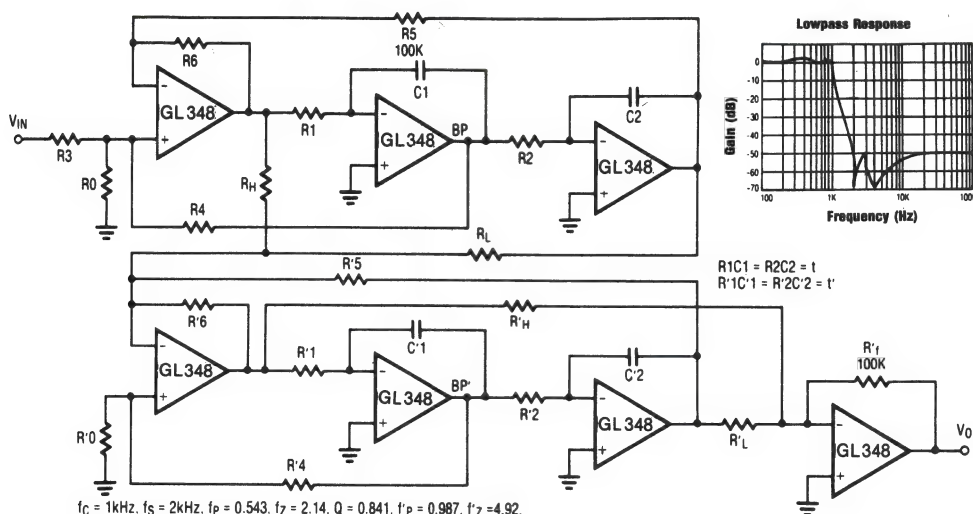
$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}} \cdot f_o = \frac{1}{2\pi\sqrt{\frac{R8}{R7}}} \times \frac{1}{\sqrt{R2R3C1C2}} \cdot f_{NOTCH} = \frac{1}{2\pi\sqrt{\frac{R6}{R3R5R7C1C2}}}$$

$$\text{Necessary condition for notch: } \frac{1}{R6} = \frac{R1}{R4R7}$$

Ex: $f_{NOTCH} = 3\text{kHz}$, $Q = 5$, $R1 = 270\text{K}$, $R2 = R3 = 20\text{K}$, $R4 = 27\text{K}$, $R5 = 20\text{K}$, $R6 = R8 = 10\text{K}$, $R7 = 100\text{K}$,
 $C1 = C2 = 0.001\mu\text{F}$

Better noise performance than the state-space approach

Figure 7. 3 Amplifier Bi-Quad Notch Filter



$f_c = 1\text{kHz}$, $f_s = 2\text{kHz}$, $f_p = 0.543$, $f_z = 2.14$, $Q = 0.841$, $f'_p = 0.987$, $f'_z = 4.92$.

$Q' = 4.403$, normalized to ripple BW

$$f_p = \frac{1}{2\pi} \sqrt{\frac{R_6}{R_5}} \times \frac{1}{t}, \quad f_z = \frac{1}{2\pi} \sqrt{\frac{R_H}{R_L}} \times \frac{1}{t}, \quad Q = \frac{1 + R_4/R_3 + R_4/R_0}{1 + R_6/R_5} \times \sqrt{\frac{R_6}{R_5}}, \quad Q' = \sqrt{\frac{R'_6}{R'_5}} \times \frac{1 + R'_4/R'_0}{1 + R'_6/R'_5 + R'_6/R'_p}$$

$$R_p = \frac{R_H R_L}{R_H + R_L}$$

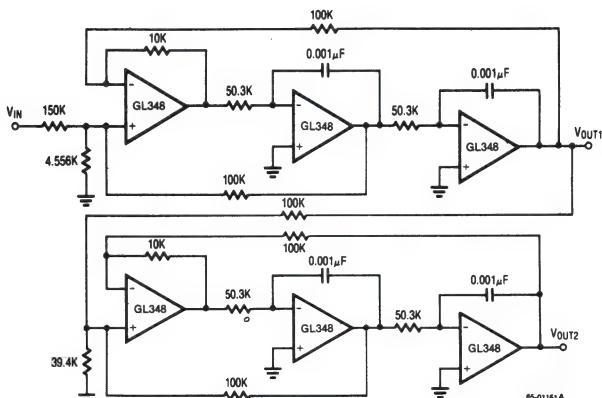
Use the BP outputs to tune Q , Q' ; tune the 2 sections separately

$R_1 = R_2 = 92.6\text{K}$, $R_3 = R_4 = R_5 = 100\text{K}$, $R_6 = 10\text{K}$, $R_0 = 107.8\text{K}$, $R_L = 100\text{K}$, $R_H = 155.1\text{K}$.

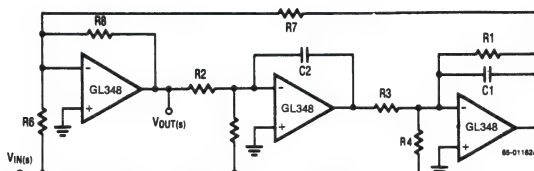
$R'_1 = R'_2 = 50.9\text{K}$, $R'_4 = R'_5 = 100\text{K}$, $R'_6 = 10\text{K}$, $R'_0 = 5.78\text{K}$, $R'_L = 100\text{K}$, $R'_H = 248.12\text{K}$, $R'_p = 100\text{K}$.

All capacitors are $0.001\mu\text{F}$

Figure 8. 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)



Use general equations, and tune each section separately
 $Q_{1st \text{ Section}} = 0.541$, $Q_{2nd \text{ Section}} = 1.306$
 The response should have 0dB peaking

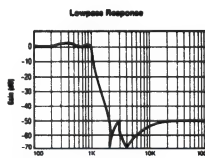
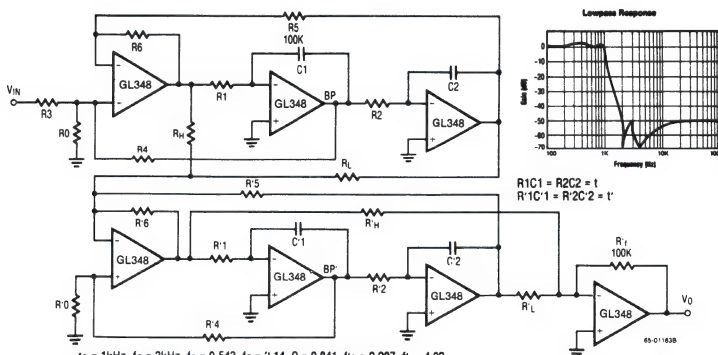


$$Q = \sqrt{\frac{R6}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}} \cdot f_0 = \frac{1}{2\pi} \sqrt{\frac{R6}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}} \cdot f_{NOTCH} = \frac{1}{2\pi} \sqrt{\frac{R6}{R3R5R7C1C2}}$$

Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: $f_{NOTCH} = 3\text{kHz}$, $Q = 5$, $R1 = 270K$, $R2 = R3 = 20K$, $R4 = 27K$, $R5 = 20K$, $R6 = R8 = 10K$, $R7 = 100K$,
 $C1 = C2 = 0.001\mu F$

Better noise performance than the state-space approach



$$R1C1 = R2C2 = 1$$

$$R1'C1'1 = R2'C2'2 = 1'$$

$f_c = 1\text{kHz}$, $f_s = 2\text{kHz}$, $f_p = 0.543$, $f_z = 2.14$, $Q = 0.841$, $f_p = 0.987$, $f_z = 4.92$,
 $Q' = 4.403$, normalized to ripple BW

$$f_p = \frac{1}{2\pi} \sqrt{\frac{R6}{R5}} \times \frac{1}{t} \cdot f_z = \frac{1}{2\pi} \sqrt{\frac{R_H}{R_L}} \times \frac{1}{t} \cdot Q = \frac{1 + R4/R3 + R4/R0}{1 + R6/R5} \times \sqrt{\frac{R6}{R5}} \cdot Q' = \sqrt{\frac{R6}{R5}} \cdot \frac{1 + R4/R0}{1 + R6/R5 + R6/Rp}$$

$$Rp = \frac{R_H R_L}{R_H + R_L}$$

Use the BP outputs to tune Q, Q', tune the 2 sections separately

$R1 = R2 = 92.6K$, $R3 = R4 = R5 = 100K$, $R6 = 10K$, $R0 = 107.8K$, $R_L = 100K$, $R_H = 155.1K$,
 $R1' = R2' = 50.9K$, $R4' = R5' = 100K$, $R6' = 10K$, $R0' = 5.78K$, $R_L' = 100K$, $R_H' = 248.12K$, $R1' = 100K$.

All capacitors are $0.001\mu F$

GL358/358A

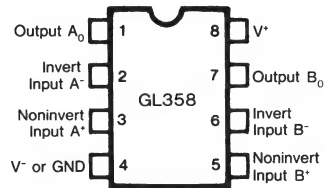
DUAL OPERATIONAL AMPLIFIER

Description

The GL358 consists of two independent, high gain, internally frequency compensated operational amplifiers which were specifically to operate from a single power supply over a wide range of voltage and the power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional OP AMP circuits which now can be more easily implemented in single power systems.

Pin Configuration



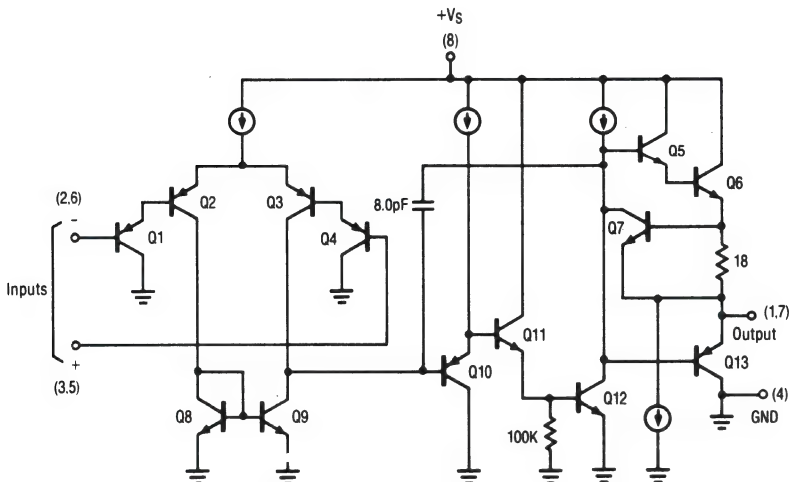
Features

- **Input Common Mode Voltage Range Includes Ground.**
- **Wide Power Supply Range. (Single or Dual Supply) 3V to 30V or $\pm 1.5V$ to $\pm 16V$**
- **Large Output Voltage Swing. 0V to $V^+ - 1.5V$**
- **Internally Frequency Compensated for Unity Gain.**
- **Low Input Bias Current.**
- **Low Input Offset Voltage.**
- **Very Low Supply Current Drain.**

Absolute Maximum Ratings

Supply Voltage, V^+	32 or ± 16	V
Differential Input Voltage	± 32	V
Input Voltage	-0.3 to 32	V
Power Dissipation	570	mW
Operating Temperature Range	0 to 70	$^{\circ}\text{C}$
Storage Temperature Range	-55 to 125	$^{\circ}\text{C}$
Lead Temperature	260	$^{\circ}\text{C}$

Schematic Diagram (Each Amplifier)



Electrical Characteristics:

Unless otherwise stated, these specification apply for $V^*=5V$, $V^*Max=30V$ and $0^{\circ}C \leq T_A \leq 70^{\circ}C$

PARAMETER	SYMBOL	TEST CONDITIONS	GL358			GL358A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	$V^*=5V$ to Max, $V_O=1.4V$, $R_S=0\Omega$ $V_{ICR}=0V$ to $V^*-1.5V$ $T_A=25^{\circ}C$		± 2	± 7 ± 9		± 2	± 3 ± 5	mV
Input Offset Current	I_{IO}	$I_{IN}(+) - I_{IN}(-)$, $V_O=1.4V$ $T_A=25^{\circ}C$		± 5	± 50 ± 150		± 5	± 30 ± 75	nA
Input Bias Current	I_{IB}	$I_{IN}(+)$ or $I_{IN}(-)$, $V_O=1.4V$ $T_A=25^{\circ}C$		45 40	250 500		45 40	100 200	nA
Input Common-Mode Voltage range	V_{ICR}	$V^*=5V$ to Max $T_A=25^{\circ}C$	0 to $V^*-1.5V$ $V^*-2.0V$			0 to $V^*-1.5V$ $V^*-2.0V$			V
Supply Current	I^+, I^-	$R_L = \infty$ $V^*=5V$, $V_O=2.5V$ $V^*=Max$, $V_O=15V$		0.7 1	1.2 2		0.7 1	1.2 2	mA
Large-Signal Voltage Gain	A_{VD}	$V^*=15V$, $R_L \geq 2K\Omega$ $V_O=-5V$ to $+5V$ $T_A=25^{\circ}C$	25 15	100		25 15	100		V/mV
Output Voltage Swing	V_{OH} V_{OL}	$V^*=MAX$ $V^*=5V$, $R_L \leq 10K\Omega$	26 27	28		26 27	28		V mV
Common Mode Rejection Ratio	CMRR	$T_A=25^{\circ}C$ $V^*=5V$ to Max	65	70		65	85		dB
Power Supply Rejection Ratio	PSRR	$V^*=5V$ to Max $T_A=25^{\circ}C$	65	100		65	100		dB
Output Current	Source	$V_{IN}(+) = 1V$, $V_{IN}(-) = 0V$ $T_A=25^{\circ}C$ $V^*=15V$, $V_O=4V$	20	40		20	40		mA
	Sink	$V^*=15V$ $V_{IN}(-) = 1V$ $V_{IN}(+) = 0V$ $T_A=25^{\circ}C$ $V_O=15V$	10	20		10	20		mA
		$V_O=200mV$	12	50		12	50		μA
Short Circuit Current	I_{OS}	$V^*=5V$ $T_A=25^{\circ}C$ $V_O=0V$		40	60		40	60	mA
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			7			7		$\mu V/^{\circ}C$
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$			10			10		pA/ $^{\circ}C$

TYPICAL PERFORMANCE CURVES

Figure 1 – Input Voltage Range

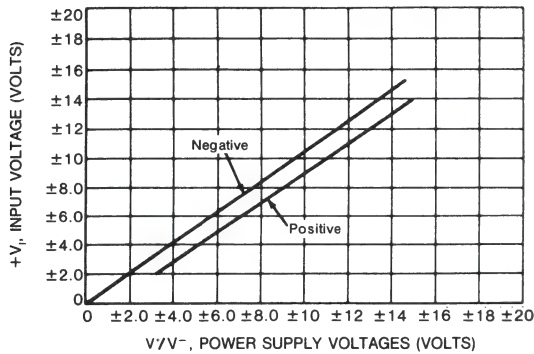


Figure 2 – Open Loop Frequency Response

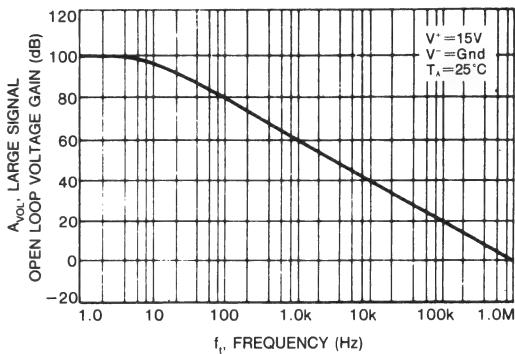


Figure 3 – Large Signal Frequency Response

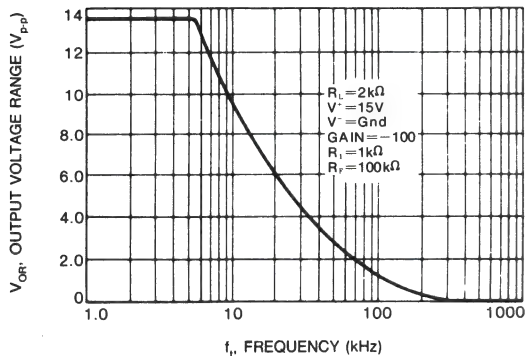


Figure 4 – Small Signal Voltage Follower Pulse Response (Non Inverting)

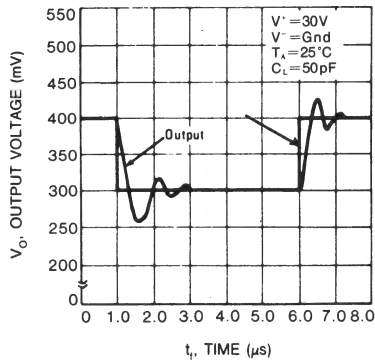


Figure 5 – Power Supply Current versus Power Supply Voltage

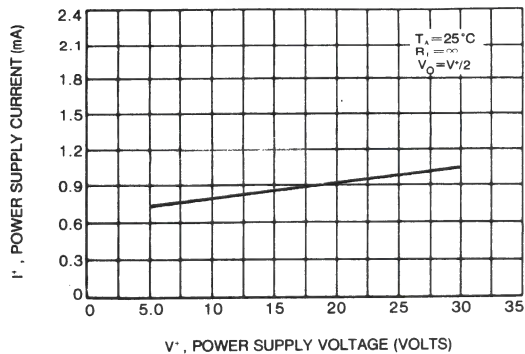
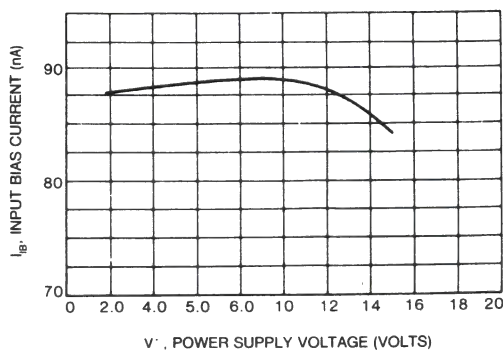


Figure 6 – Input Bias Current versus Supply Voltage



$$f = \frac{R1 + R_C}{4 \cdot C R1 + R1} \text{ if } R3 = \frac{R2 + R1}{R2 + R1}$$

V_{ref}

$50k$

$5.0k$

$10k$

V^-

$1/2$ GL358

V_o

$V_{ref} = \frac{1}{2} V^-$

$f_o = \frac{1}{2\pi RC}$

For $f_o = 1 \text{ kHz}$
 $R = 16 \text{ k}\Omega$
 $C = 0.01 \text{ }\mu\text{F}$

$e_0 = C(1 + a + b)(e_2 - e_1)$

The diagram shows a Schmitt trigger circuit using a 741 op-amp. The non-inverting input (+) is connected to a voltage divider with resistors R1 and R2. R1 is connected to the input signal V_{in} , and R2 is connected to the output V_O . The inverting input (-) is connected to a reference voltage V_{ref} . The output V_O is shown with a hysteresis loop, switching between V_{OH} and V_{OL} at threshold voltages V_{inL} and V_{inH} .

$$V_{inL} = \frac{R1}{R1+R2} (V_{OL}-V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1+R2} (V_{OH}-V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1+R2} (V_{OH}-V_{OL})$$

$f_o = \frac{1}{2 \pi RC}$
 $R1 = OR$
 $R2 = \frac{R1}{T_{BP}} \quad V_{ref} = \frac{1}{2} V^+$
 $R3 = T_N R2$
 $C1 = 10C$
 For $f_o = 1 \text{ kHz}$
 $Q = 10$
 $T_{BP} = 1$
 $T_N = 1$

Where T_{BP} = Center Frequency Gain
 T_N = Passband Notch Gain

$R = 160 \text{ k}\Omega$
 $C = 0.001 \mu\text{F}$
 $R1 = 1.6 \text{ M}\Omega$
 $R2 = 1.6 \text{ M}\Omega$
 $R3 = 1.6 \text{ M}\Omega$

GL4558

DUAL OPERATIONAL AMPLIFIERS

Description

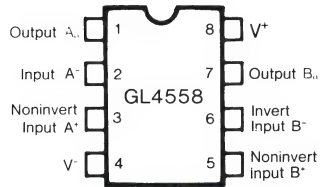
The GL4558 is dual general purpose operational amplifiers with half electrically similar to μ A741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage follower application.

The devices are short circuit protected and the internal frequency compensation ensures stability without external components.

These are characterized for operation from 0°C to 70°C.

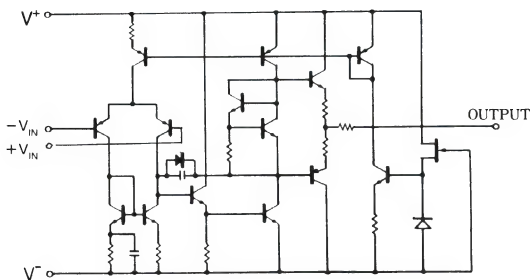
PIN Configuration



Features

- Short-Circuit Protection
- Wide common-mode and differential voltage ranges
- No frequency compensation required
- Low power consumption
- No latch-up
- 3 MHz unity gain bandwidth guaranteed
- Gain and phase match between amplifiers

Schematic Diagram (Each Amplifier)



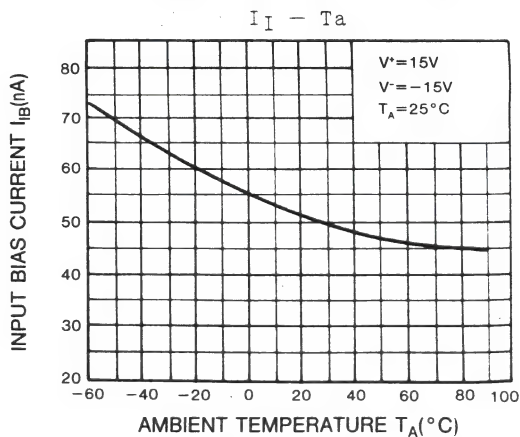
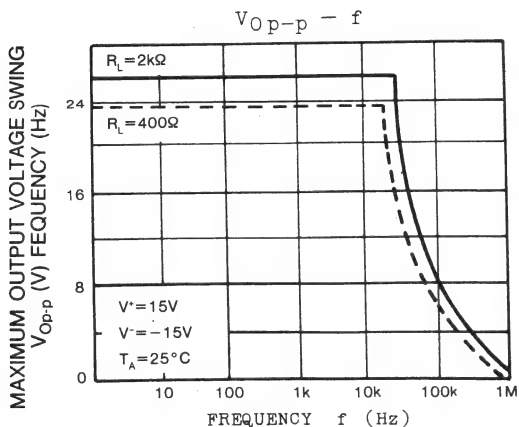
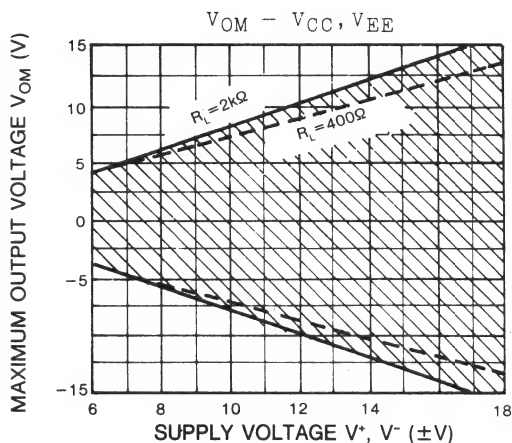
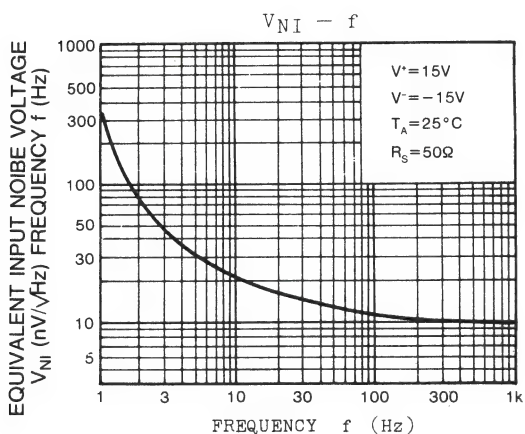
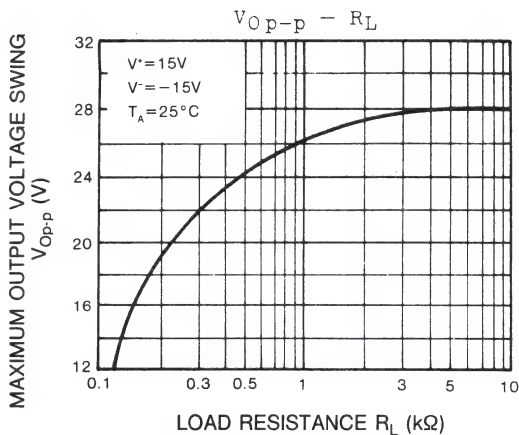
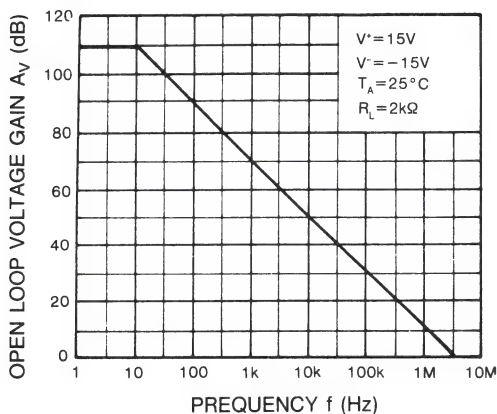
Absolute Maximum Ratings

PARAMETER	GL4558	UNIT
Supply Voltage	± 18	V
Differential Input Voltage	± 30	V
Input Voltage	± 15	V
Power Dissipation	570	mW
Operating Temperature Range	0 to 70	°C
Storage Temperature Range	-55 to 125	°C
Lead Temperature	260	°C

Electrical Characteristics ($V^+ = +15V$, $V^- = -15V$, $T_A = 25^\circ C$)

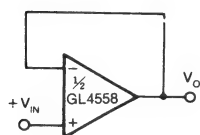
PARAMETER	SYMBOL	TEST CONDITIONS	GL4558			UNIT
			MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	$R_S \leq 10k\Omega$	—	± 0.5	± 5	mV
Input Offset Current	I_{IO}		—	± 5	± 200	nA
Input Bias Current	I_{IB}		—	50	500	nA
Input Resistance	r_i		0.3	2.0	—	M Ω
Large-Signal Voltage Gain	A_V	$R_L \geq 2k\Omega$, $V_C = \pm 10V$	20	200	—	V/mV
Output Voltage Swing	V_{OM}	$R_L \geq 10k\Omega$	± 12	± 14	—	V
		$R_L \geq 2k\Omega$	± 10	± 13	—	V
Input Common-Mode Voltage range	V_{ICR}		± 12	± 13	—	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$	70	90	—	dB
Supply Voltage Rejection Ratio		$R_S \leq 10k\Omega$	—	30	150	$\mu V/V$
Supply Current	I^+, I^-		—	2.3	5.6	mA
Slew Rate	SR	$R_L \geq 2k\Omega$	—	1.0	—	V/ μs
Power Consumption	P_C	$R_L = \infty$	—	100	170	mW
Input Noise Voltage	V_N	$R_S = 1k\Omega$ $f = 30Hz \sim 30KHz$	—	2.5	—	μV_{rms}
Source Current	I_{source}		—	40	—	mA
Sink Current	I_{sink}		—	40	—	mA

Typical Performance Curves

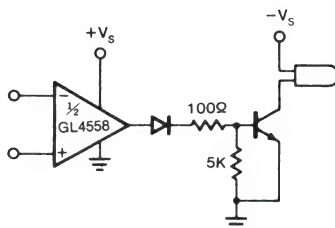


Typical Applications

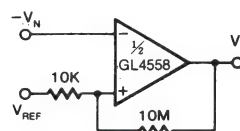
Voltage Follower



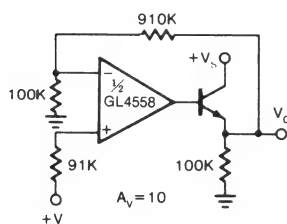
Lamp Driver



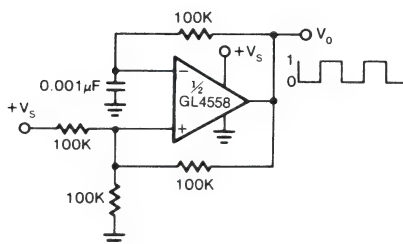
Comparator With Hysteresis



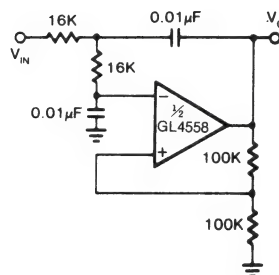
Power Amplifier



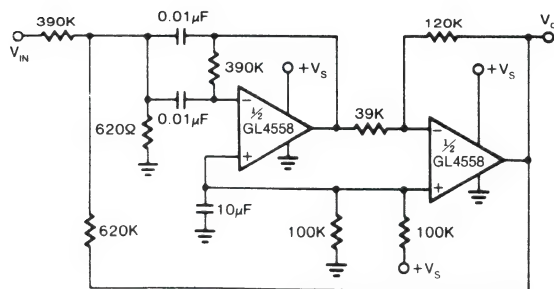
Squarewave Oscillator



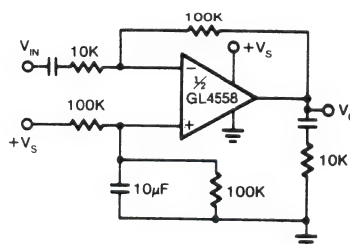
DC Coupled 1kHz Low-Pass Active Filter



1kHz Bandpass Active Filter



AC Coupled Inverting Amplifier



GLC 9458

LOW POWER

CMOS OPERATIONAL AMPLIFIER

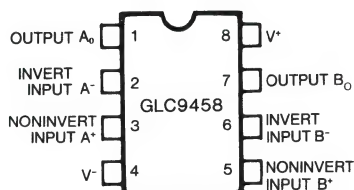
Description

The GLC9458 is a monolithic operation amplifier. These devices provide the designer with high performance operation at low voltages and are an ideal design tool when ultra low input current and low power dissipation are desired. The basic amplifier will operate at supply voltages ranging from $\pm 1.0\text{V}$ to $\pm 8\text{V}$, and may be operated from a single Lithum^e cell.

Output swings range to within a few millivolts of the supply voltages. Of particular significance is the extremely low (1pA) input current, input noise current of $0.01\text{ pA}/\sqrt{\text{Hz}}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications. The inputs are internally protected and require no special handling procedures.

AC performance is excellent, with a slew rate of $0.16\text{V}/\mu\text{s}$, and unity bandwidth of 0.48 MHz . Because of the low power dissipation, operating temperatures and drift are quite low. Application utilizing these features may include stable instruments, extended life designs, or high density packages.

Pin Configuration



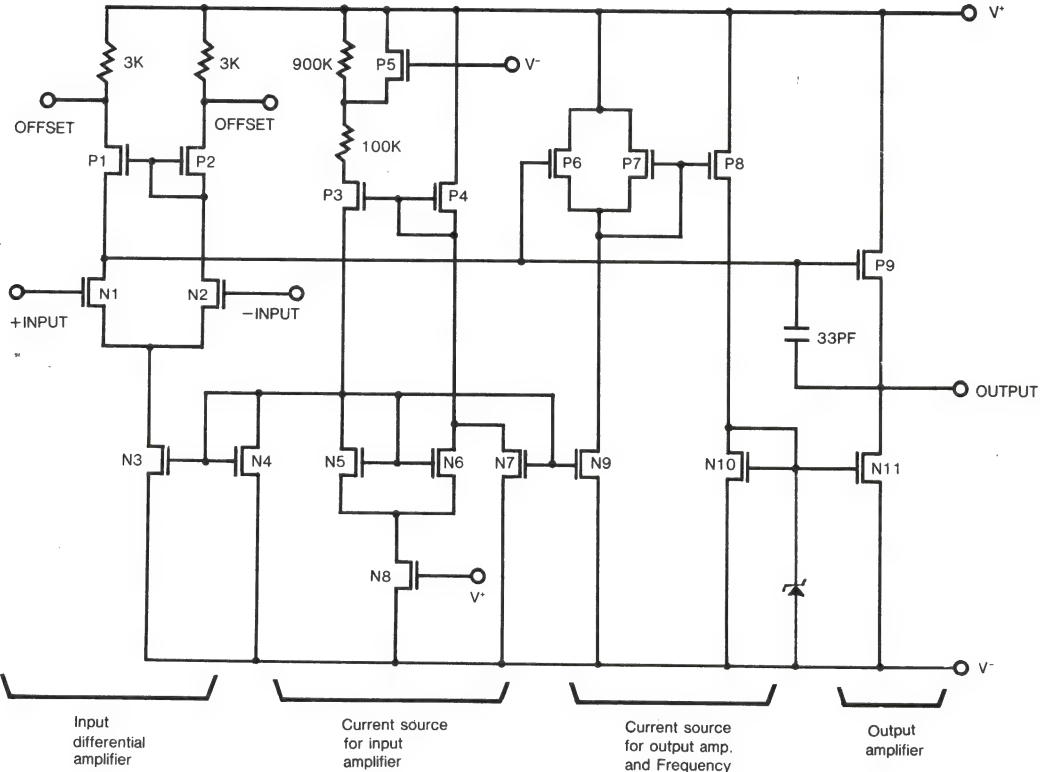
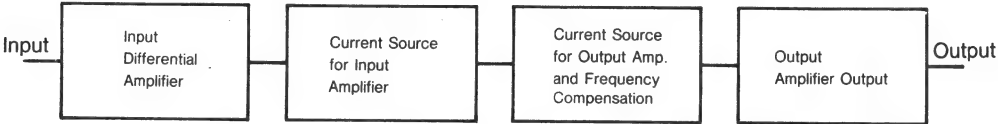
Feature

- Wide Operating Voltage Range $\pm 1.0\text{V}$ to $\pm 8.0\text{V}$
- High Input Impedance — $10^{12}\Omega$
- Input Current Lower Than BIEFTs—Typ 1 pA
- Output Voltage Swings to Within Millivolts of V⁻ And V⁺
- Low Power Replacement for Many Standard Op Amps

Absolute Maximum Ratings.

Supply Voltage	18	V
Input Voltage	V ⁻ - 0.3 to V ⁺ + 0.3	V
Differential Input Voltage	$\pm [(V^{+} + 0.3) - (V^{-} - 0.3)]$	V
Duration of Output Short Circuit	Unlimited	
Power Dissipation (@ 25°C)	250	mW
Storage Temperature Range	-65 to + 150°C	°C
Operating Temperature Range	0 to + 70	°C

Block Diagram (One Section)



Electrical Characteristics: ($V_{+} = \pm 5V$, $T_A = 25^{\circ}C$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	$R_S \leq 100K\Omega$, $T_A = 25^{\circ}C$			15	mV
Temperature Coefficient(V_{os})	$R_S = 100K\Omega$		25		$\mu V/^{\circ}C$
Input offset current			0.5	30	pA
Input Bias current			1.0	50	pA
Common Mode Voltage Range		± 4.2			V
Output voltage swing	$R_L = 100k$	± 4.9			V
Large Signal Voltage Gain	$V_O = +4V$, $R_L = 100k$	80	102		dB
Unity Gain Bandwidth	$I_O = 100\mu A$		0.48		MHz
Input resistance			10^{12}		Ω
Common Mode Rejection Ratio	$R_S \leq 100k\Omega$, $I_O = 100\mu A$	70	91		dB
Power Supply Rejection Ratio	$R_S \leq 100k\Omega$, $I_O = 100\mu A$	80	86		dB
Input Referred Noise Voltage	$R_S = 100\Omega$, $f = 1kHz$		100		nV/\sqrt{Hz}
Input Referred Noise Current	$R_S = 100\Omega$, $f = 1kHz$		0.01		pA/\sqrt{Hz}
Supply Current (Each AMP)	No Signal, No Load		0.1	0.25	mA
Channel Separation	$A_{VOL} = 100$		120		dB
Slew Rate	$A_{VOL} = 1$, $C_L = 100pF$ $R_L = 100k$		0.16		V/ μS
Rise time	$V_{in} = 50mV$, $C_L = 100pF$ $R_L = 100k$		2		μS
Overshoot	$V_{in} = 50mV$, $C_L = 100pF$ $R_L = 100k$		10		%

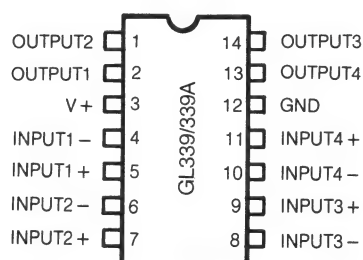
GL339/339A

LOW POWER, LOW OFFSET VOLTAGE QUAD COMPARATORS

Description

The GL339 consists of four independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected pnp input stage allows the input common-mode voltage to include ground.

Pin Configuration



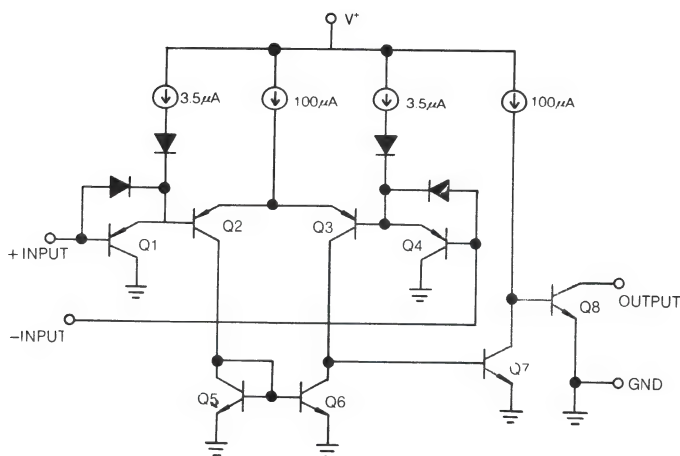
Features

- Single Supply Operation +2.0V to +36V
- Dual Supply Operation $\pm 1.0V$ to $\pm 18V$
- Compatible with All forms of Logic
- Allow Comparison of Voltages Near Ground Potential
- Low Current Drain 800 μA TYP
- Low Input Bias Current 25nA TYP
- Low Input Offset Current ± 5 nA TYP
- Low Offset Voltage $\pm 2mV$

Absolute Maximum Ratings

Supply Voltage, V^+	+36V or $\pm 18V$
Differential Input Voltage	36V
Input Voltage Range	$-0.3V$ to +36V
Power Dissipation	1000 mW
Input current ($V_{IN} < -0.3V$)	50 mA
Operating Temperature Range	$0^\circ C$ to $+70^\circ C$
Storage Temperature Range	$-55^\circ C$ to $+125^\circ C$
Pin Temperature	$260^\circ C$

Schematic Diagram



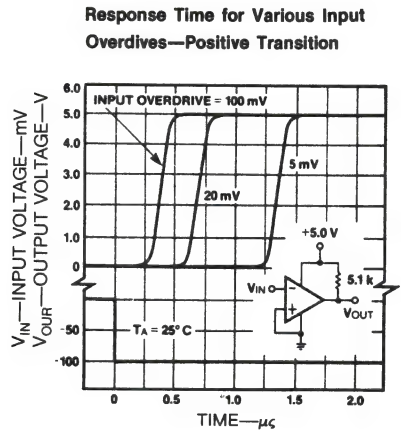
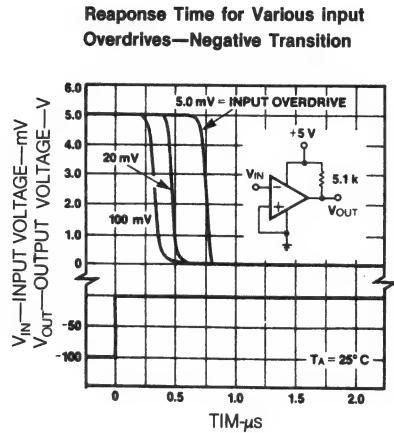
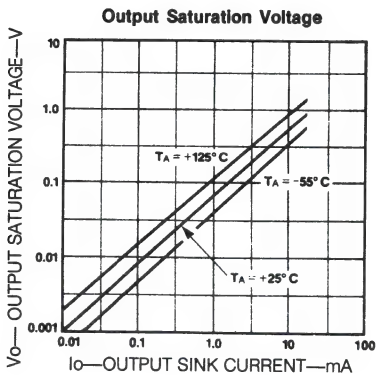
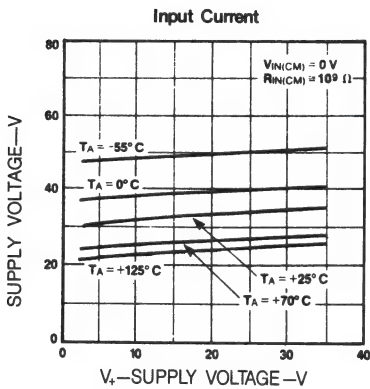
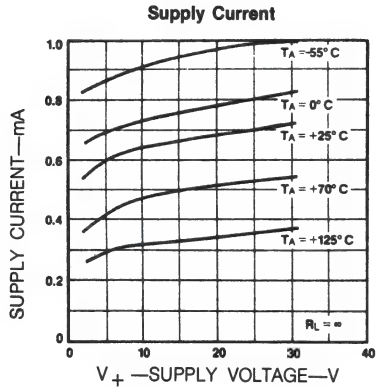
Electrical Characteristics: $V^+ = 5V$, $T_A = 25^\circ C$, unless otherwise specified)

PARAMETER	Test Conditions	GL339			GL339A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	At out. switch point $V_O = 1.4$; $R_S = 0$ $V_{REF} = 1.4V$ $0^\circ C \leq T_A \leq 70^\circ C$		± 2	± 5		± 1	± 2	mV
				9			4	
Input Bias Current (1)	Output in linear range $0^\circ C \leq T_A \leq 70^\circ C$		25	250		25	250	nA
				400			400	
Input Offset Current	$0^\circ C \leq T_A \leq 70^\circ C$		± 5	± 50		± 5	± 50	nA
				± 150			± 150	
Input Common-Mode Voltage Range (2)	$0^\circ C \leq T_A \leq 70^\circ C$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
		0		$V^+ - 2.0$	0		$V^+ - 2.0$	
Supply Current	$R_L = \infty$		0.8	2.0		0.8	2.0	mA
Supply Current	$V_{CC} = 30V$, $R_L = \infty$			2.5			2.5	mA
Voltage Gain	$R_L \geq 15K\Omega$, $V^+ = 15V$	93	106		93	106		dB
Large Signal Response Time	$V_{IN} =$ TTL logic swing; $V_{REF} = 1.4V$; $R_L = 5.1K\Omega$ $V_{RL} = 5V$		300			300		ns
Response Time (3)	$V_{RL} = 5V$; $R_L = 5.1K\Omega$		1.3			1.3		μs
Ouptur Sink Current	$V_{IN(-)} \geq 1V$; $V_{IN(+)} = 0V$; $V_O \leq 1.5V$	6	16		6	16		mA
Output Saturation	$V_{IN(-)} \geq 1V$ $V_{IN(+)} = 0V$ $I_{sink} \leq 4mA$ $0^\circ C \leq T_A \leq 70^\circ C$		250	400		250	400	mV
				700			700	
Output Leakage	$V_{IN(+)} \geq 1V$ $V_{IN(-)} = 0V$ $0^\circ C \leq T_A \leq 70^\circ C$		0.1			0.1		nA
				1000			1000	
Differential Input Voltage	All $V_{IN} \geq 0V$ (or V^- if split supply is used) $0^\circ C \leq T_A \leq 70^\circ C$			V^+			V^+	V

NOTES:

- (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.
- (2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50mA.
- (3) The response time specified is for a 100mA input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

TYPICAL PERFORMANCE CURVES



APPLICATION NOTE

The GL339/A are high-gain, wide-bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\text{ k}\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the GL339/A establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V to 30 V.

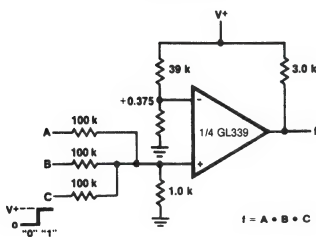
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3V (at 25°C). An input clamp diode can be used as shown in the applications section.

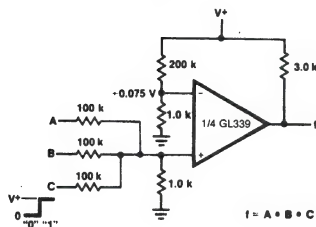
The output of the GL339/A is the uncommitted collector of a grounded-emitter npn output transistor. Many collectors can be tied together to provide an output ORing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the GL339/A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately $60\ \Omega$ saturation resistance of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

1. TYPICAL APPLICATIONS ($V^+ = 15\text{ V}$)

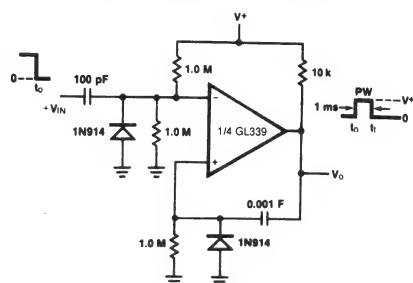
AND GATE



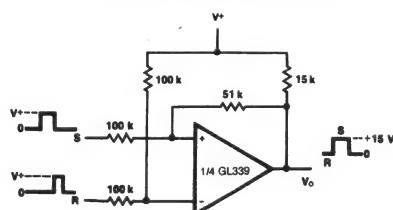
OR GATE



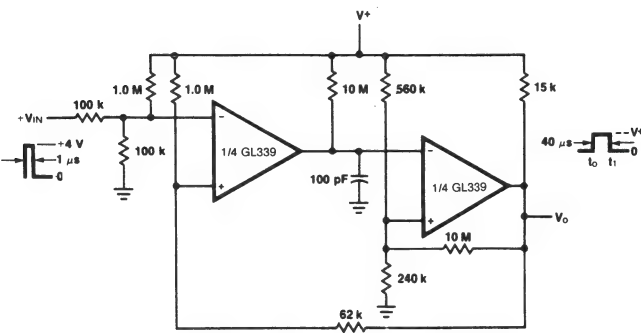
ONE-SHOT MULTIVIBRATOR



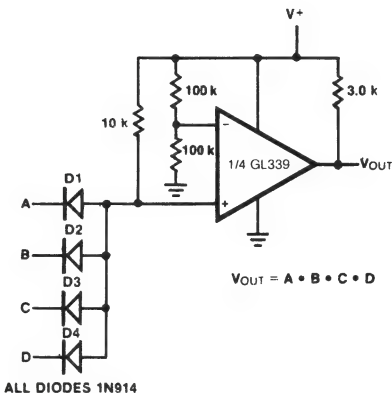
BI-STABLE MULTIVIBRATOR



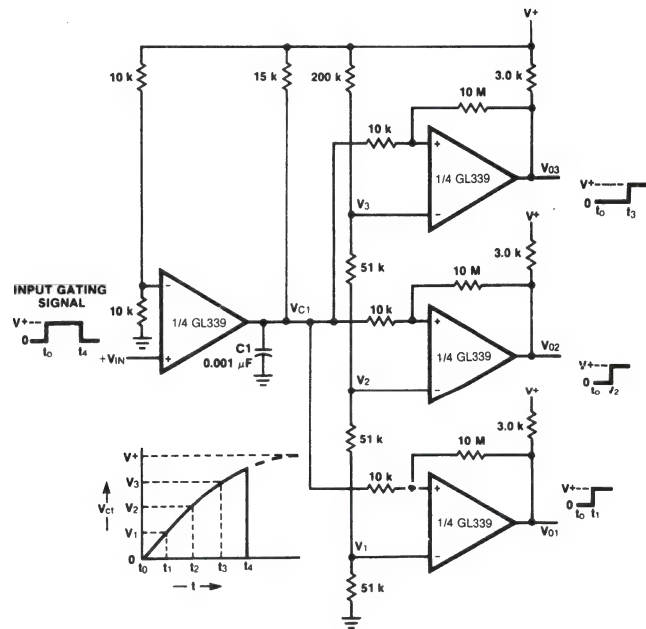
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT



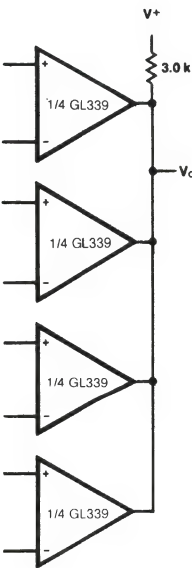
LARGE FAN-IN AND GATE



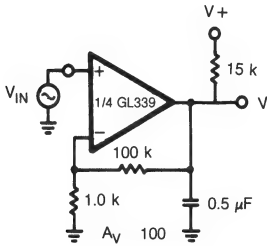
TIME DELAY GENERATOR



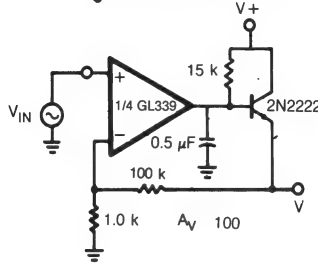
ORING THE OUTPUTS



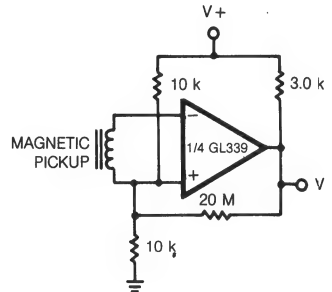
LOW FREQUENCY OP AMP



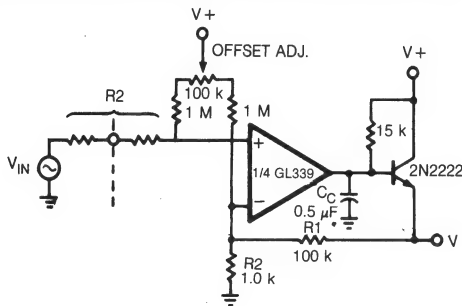
LOW FREQUENCY OP AMP
($V_O = 0$ V FOR $V_{IN} = 0$ V)



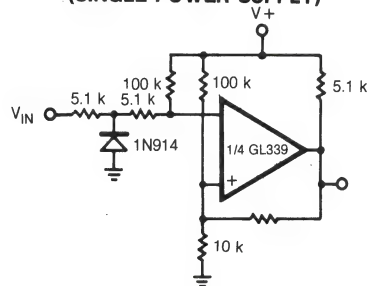
TRANSDUCER AMPLIFIER



LOW FREQUENCY OP AMP WITH OFFSET ADJUST

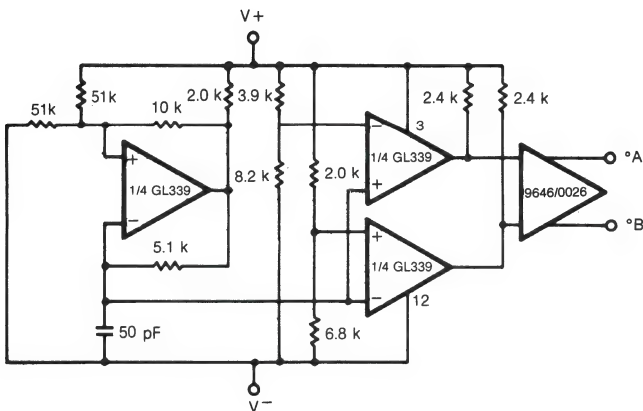


ZERO-CROSSING DETECTOR
(SINGLE POWER SUPPLY)

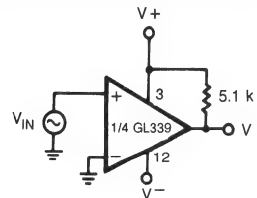


2. SPLIT-SUPPLY APPLICATIONS $V^+ = +15$ V and $V^- = -15$ V

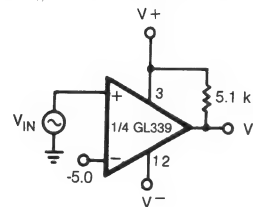
MOS CLOCK DRIVER



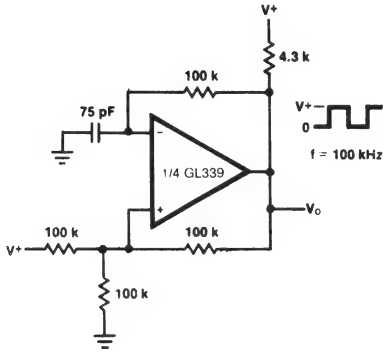
ZERO CROSSING DETECTOR



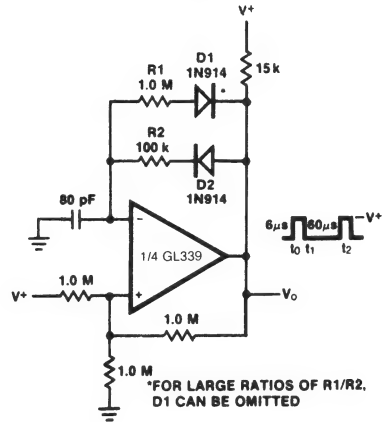
COMPARATOR WITH A NEGATIVE REFERENCE



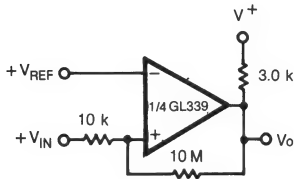
SQUAREWAVE-OSCILLATOR



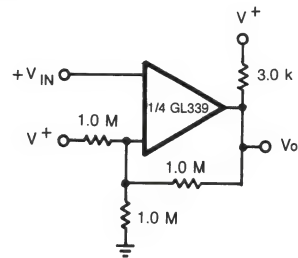
PULSE GENERATOR



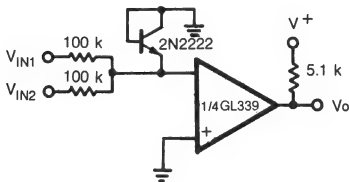
NON-INVERTING COMPARATOR WITH HYSTERESIS



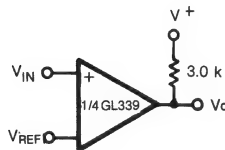
INVERTING COMPARATOR WITH HYSTERESIS



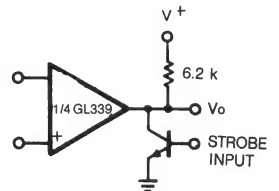
COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY



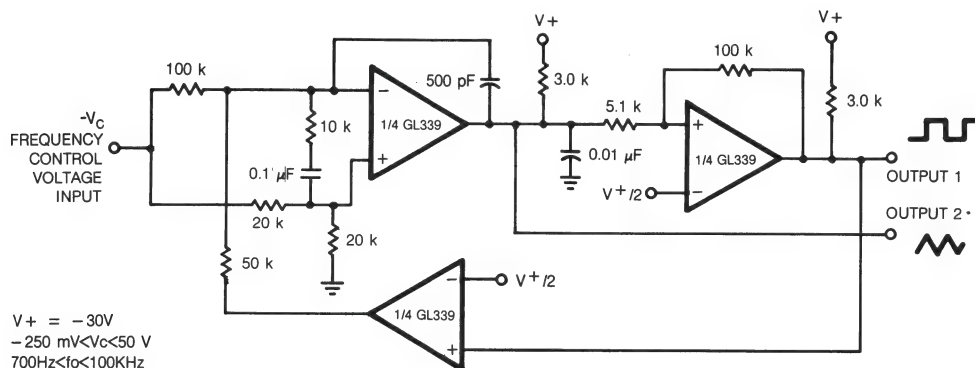
BASIC COMPARATOR



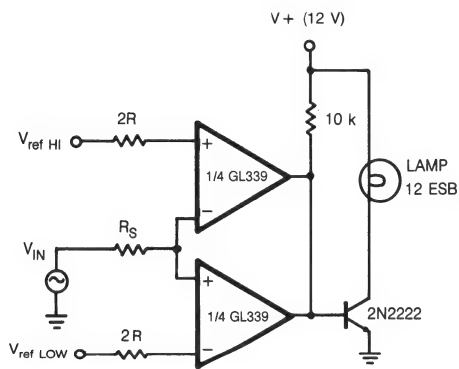
OUTPUT STROBING



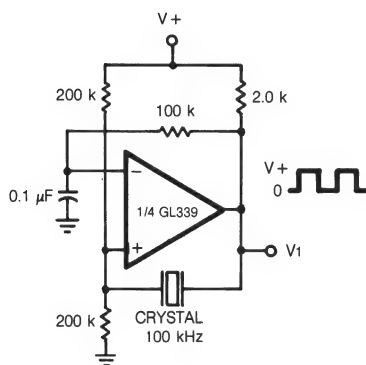
OR LOGIC GATE WITHOUT PULL-UP RESISTOR



LIMIT COMPARATOR



CRYSTAL CONTROLLED OSCILLATOR



GL393/393A

LOW POWER, LOW OFFSET VOLTAGE DUAL COMPARATORS

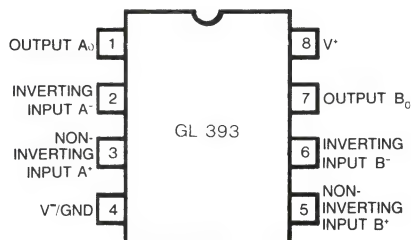
Description

The GL393 consists of two independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected pnp input stage allows the input common-mode voltage to include ground.

Features

- Single Supply Operation $+2.0\text{V}$ to $+36\text{V}$
- Dual Supply Operation $\pm 1.0\text{V}$ to $\pm 18\text{V}$
- Compatible with All forms of Logic
- Allow Comparison of Voltages Near Ground Potential
- Low Current Drain $400\text{ }\mu\text{A}$ TYP
- Low Input Bias Current 25 nA TYP
- Low Input Offset Current $\pm 5\text{ nA}$ TYP
- Low Offset Voltage $\pm 2\text{ mV}$

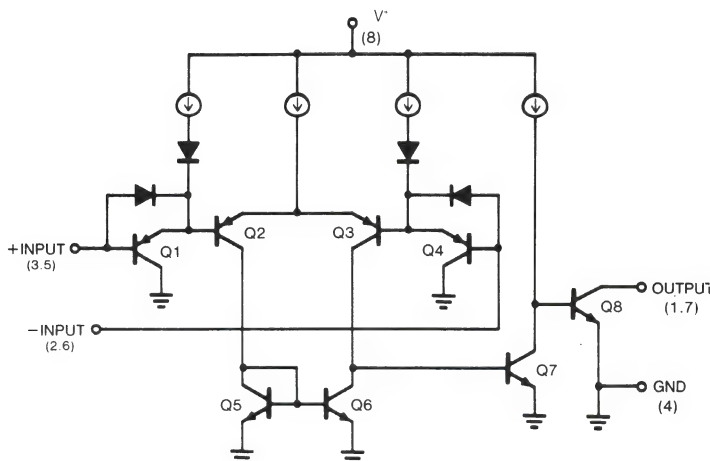
Pin Configuration



Absolute Maximum Ratings

Supply Voltage, V^+	$+36\text{V}$ or $\pm 18\text{V}$
Differential Input Voltage	36V
Input Voltage Range	-0.3V to $+36\text{V}$
Power Dissipation	500 mW
Input Current ($V_{IN} < -0.3\text{V}$)	50 mA
Operating Temperature Range	0°C to $+70^\circ\text{C}$
Storage Temperature Range	-55°C to $+125^\circ\text{C}$
Pin Temperature	260°C

Schematic Diagram



Electrical Characteristics: $V^+ = 5V$ $T_A = 25^\circ C$, unless otherwise specified)

PARAMETER	Test Conditions	GL393			GL393A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	At out. switch point $V_O = 1.4$; $R_S = 0$ $V_{REF} = 1.4V$		± 2	± 5		± 1	± 2	mV
	$0^\circ C \leq T_A \leq 70^\circ C$			9			4	
Input Bias Current (1)	Output in linear range		25	250		25	250	nA
	$0^\circ C \leq T_A \leq 70^\circ C$			400			400	
Input Offset Current			± 5	± 50		± 5	± 50	nA
	$0^\circ C \leq T_A \leq 70^\circ C$			± 150			± 150	
Input Common-Mode Voltage Range (2)		0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
	$0^\circ C \leq T_A \leq 70^\circ C$	0		$V^+ - 2$	0		$V^+ - 2$	
Supply Current	$R_L = \infty$		0.4	1		0.4	1	mA
Supply Current	$V_{CC} = 30V$, $R_L = \infty$			2.5			2.5	mA
Voltage Gain	$R_L \geq 15K\Omega$, $V^+ = 15V$	93	106		93	106		dB
Large Signal Response Time	$V_{IN} =$ TTL logic swing; $V_{REF} = +1.4V$; $R_L = 5.1K\Omega$ $V_{RL} = 5V$		300			300		ns
Response Time (3)	$V_{RL} = 5V$; $R_L = 5.1k\Omega$		1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1V$; $V_{IN(+)} = 0V$; $V_O \leq 1.5V$	6	16		6	16		mA
Output Saturation	$V_{IN(-)} \geq 1V$ $V_{IN(+)} = 0V$ $I_{sink} \leq 4mA$		150	400		150	400	mV
	$0^\circ C \leq T_A \leq 70^\circ C$			700			700	
Output Leakage	$V_{IN(+)} \geq 1V$ $V_{IN(-)} = 0V$		0.1			0.1		nA
	$0^\circ C \leq T_A \leq 70^\circ C$			1000			1000	
Differential Input Voltage	All $V_{IN} \geq 0V$ (or V^- if split supply is used) $0^\circ C \leq T_A \leq 70^\circ C$			V^+			V^+	V

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This conditions is not destructive providing the input current is limited to less than 50mA.

(3) The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300 nsec can be obtained.

Typical Performance Curves

Figure 1—Supply Current

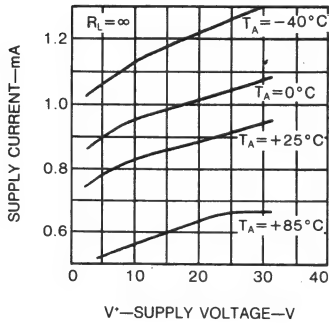


Figure 2—Input Current

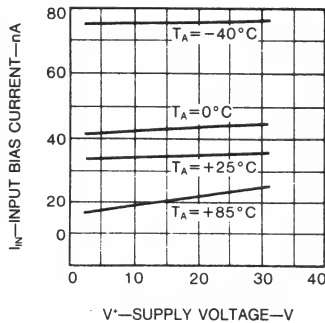


Figure 3—Output Saturation Voltage

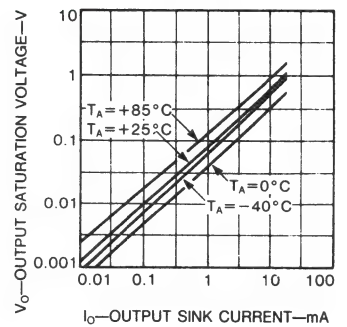


Figure 4—Response Time for Various Input Overdrives Negative Transition

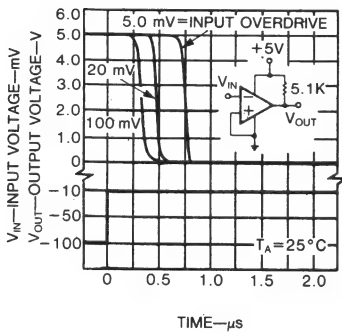
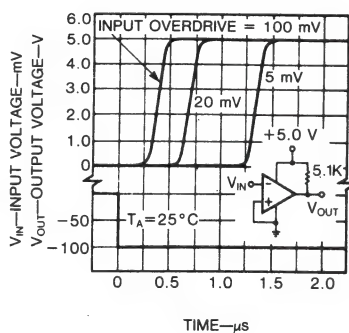


Figure 5—Response Time for Various Input Overdrives Positive Transition

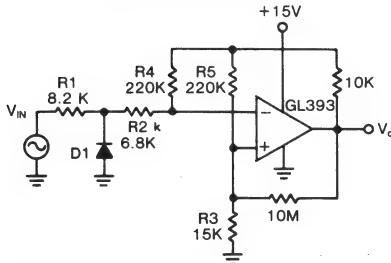


Applications

These dual comparators feature high gain, wide band width characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situa-

tion input resistors $< 10k\Omega$ should be used. The addition of positive feedback ($< 10mV$) is also recommended. It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than $-0.3V$ should not be used.

Figure 6-Zero Crossing Detector (Single Supply)



D1 prevents input from going negative by more than 0.6V

$$R1 + R = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing}$$

Figure 7-Zero Crossing Detector (Split Supplies)

$$V_{IN \text{ MIN}} \approx 0.4 \text{ peak for } 1\% \text{ phase distortion } (\Delta\theta)$$

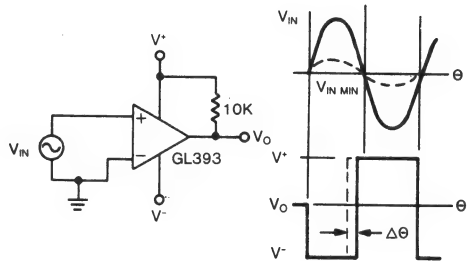


Figure 8-Free-Running Square-Wave Oscillator

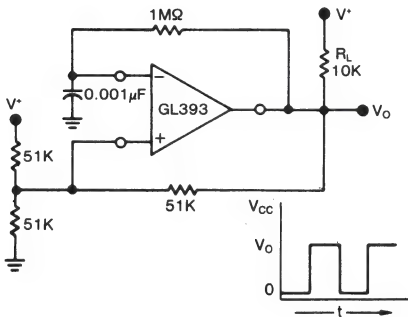


Figure 9-Time Delay Generator

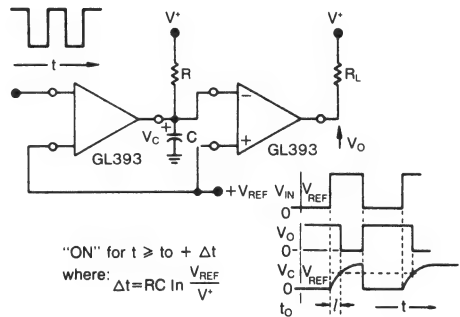
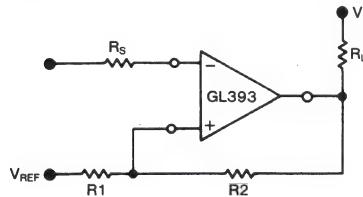


Figure 10-Comparator With Hysteresis



$$R_S = R1 \parallel R2$$

$$V_{in1} = V_{REF} + \frac{(V_{CC} - V_{REF}) R1}{R1 + R2 + R_L}$$

$$V_{in2} = V_{REF} + \frac{(V_{REF} - V_O \text{ Low}) R1}{R1 + R2 + R_L}$$

GL317

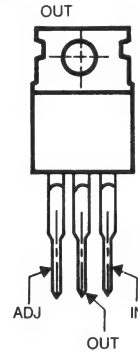
3-TERMINAL POSITIVE ADJUSTABLE REGULATOR

Description

The GL317 is a 3-Terminal Adjustable Positive Voltage Regulator capable of supplying in excess of 1.5A over an output voltage range of 1.2V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current-limiting, thermal-shutdown and safe-area compensation, making it essentially blow-out proof.

The GL317 serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, and a programmable output regulator; or by connecting a fixed resistor between the adjustment and output, the GL317 can be used as a precision current regulator.

Pin Configuration (Top View)



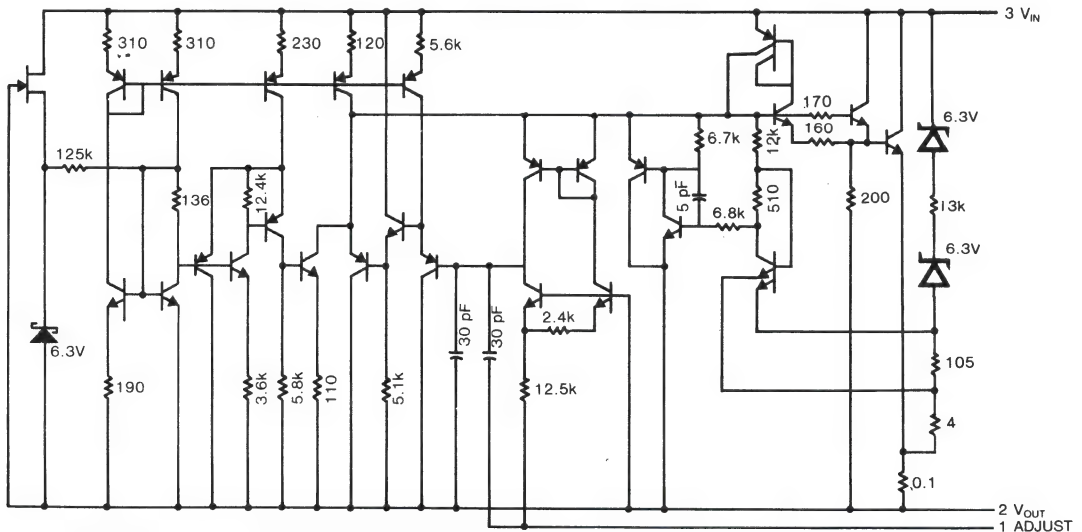
Features

- Output Current in Excess of 1.5 A in TO-220 Package.
- Output Adjustable Between 1.2V and 37V
- Internal Thermal-Overload Protection
- Internal Short-Circuit Current-Limiting Constant Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High-Voltage Applications

Absolute Maximum Ratings

Input-Output Voltage Differential	40 V _{dc}
Power Dissipation	Internally Limited
Operating Junction Temperature	0°C to +125°C
Storage Temperature	-55°C to +150°C
Pin Temperature	260°C
(Soldering, 10s Time Limit)	

Schematic Diagram



Electrical Characteristics

 $V_I - V_O = 5V$; $I_O = 0.5A$
 T_J = Operation Temperature; I_{Max} (1.5A) and P_{Max} (20W); unless otherwise specified.

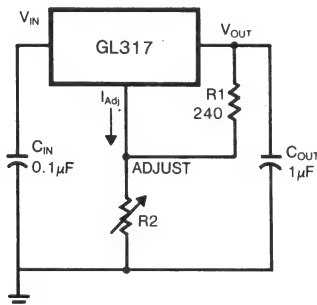
SYMBOL	PARAMETER	CONDITION	GL317			UNIT
			MIN	TYP	MAX	
Reg_{Line}	Line Regulation (Note 5)	$T_A = 25^\circ C$, $3V \leq V_I - V_O \leq 40V$		0.01	0.04	%/V
		$3V \leq V_I - V_O \leq 40V$		0.02	0.07	%/V
Reg_{Load}	Load Regulation (Note 1)	$T_A = 25^\circ C$, $10mA \leq I_O \leq I_{Max}$		$V_O \leq 5V$ 5	$V_O \geq 5V$ 25	mV
				0.1	0.5	%
		$10mA \leq I_O \leq I_{Max}$		$V_O \leq 5V$ 20	$V_O \geq 5V$ 70	mV
				0.3	1.5	%
I_{Adj}	Adjustment Pin Current			50	100	μA
ΔI_{Adj}	Adjustment Pin Current Change	$2.5V \leq V_I - V_O \leq 40V$ $10mA \leq I_L \leq I_{Max}$, $P_D \leq P_{Max}$		0.2	5	μA
V_{Ref}	Reference Voltage (Note 2)	$3V \leq V_I - V_O \leq 40V$ $10mA \leq I_O \leq I_{Max}$, $P_D \leq P_{Max}$	1.20	1.25	1.30	V
T_S	Temperature Stability			1		%
$I_{L(Min)}$	Minimum Load Current to Maintain Regulation	$V_I - V_O = 40V$		3.5	10	mA
I_{Max}	Maximum Output Current	$V_I - V_O \leq 15V$, $P_D \leq P_{Max}$	1.5	2.2		A
		$V_I - V_O = 40V$, $P_D \leq P_{Max}$, $T_A = 25^\circ C$		0.4		
N	RMS Noise, % of V_O	$T_A = 25^\circ C$, $10Hz \leq f \leq 10 kHz$		0.003		%
RR	Ripple Rejection (Note 3)	$V_O = 10V$, $f = 120 Hz$		Without C_{Adj} 65		dB
			$C_{Adj} = 10\mu F$	66	80	
S	Long-Term Stability, ($T_J = T_{high}$ (Note 4))	$T_A = 125^\circ C$		0.3	1	%
$R_{\theta JC}$	Thermal Resistance Junction to Case			5		$^\circ C/W$

Notes

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
2. Selected devices with tightened tolerance reference voltage available.
3. C_{Adj} , when used, is connected between the adjustment pin and ground.
4. Long Term Stability specification is an engineering estimate of average stability from lot to lot.

Application

Standard Application



C_{IN} is required if regulator is located an appreciable distance from power supply filter.

$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + I_{Adj} R2$$

Since I_{Adj} is controlled to less than 100 μA , the error associated with this term is negligible in most applications.

Basic Circuit Operation

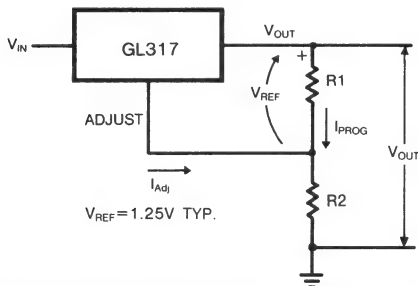
The GL317 is a 3-terminal floating regulator. In operation, the GL317 develops and maintains a nominal 1.25V reference (V_{REF}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG} by $R1$ (see Figure 1)), and this constant current flows through $R2$ to ground. The regulated output voltage is given by:

$$V_{OUT} = V_{REF} \left(1 + \frac{R2}{R1}\right) + I_{Adj} R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the GL317 was designed to control I_{Adj} to less than 0 and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the GL317 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Fig. 1. Basic Circuit Configuration



Load Regulation

The GL317 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor ($R1$) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of $R2$ can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{IN}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

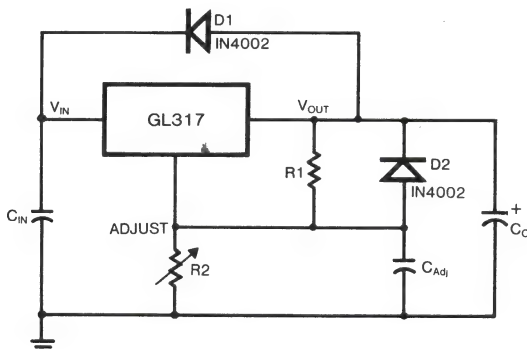
Although the GL317 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

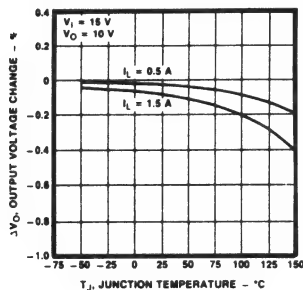
Figure 2 shows the GL317 with the recommended protection diodes for output voltages in excess of 25V or high capacitance values ($C_O > 25 \mu F$, $C_{Adj} > 10 \mu F$). Diode D1 prevents C_O from discharging through the IC during an input short circuit. Diode D2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Fig. 2. Voltage Regulator with Protection Diodes

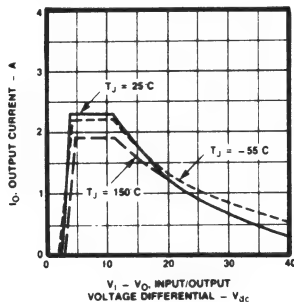


Typical Performance Curves

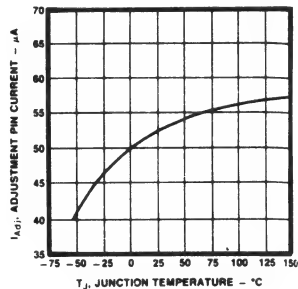
Load Regulation



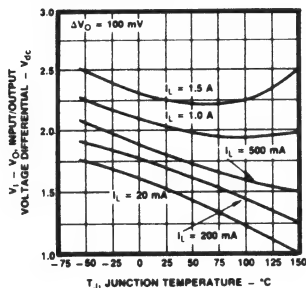
Current Limit



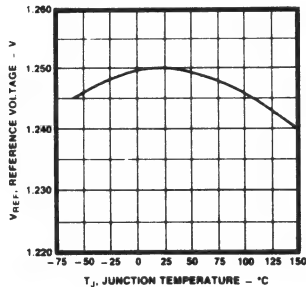
Adjustment Pin Current



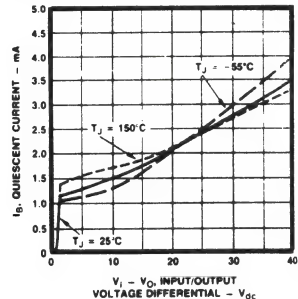
Dropout Voltage



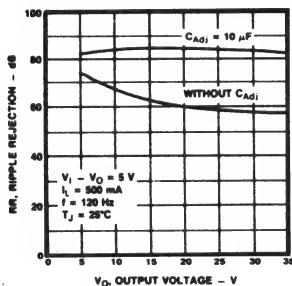
Temperature Stability



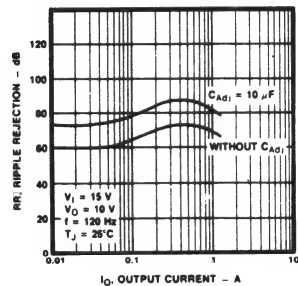
Minimum Operating Current



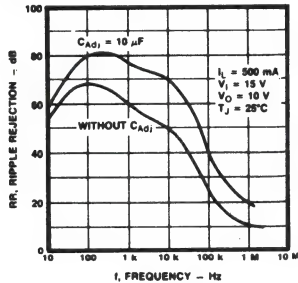
Ripple Rejection as a Function of Output Voltage



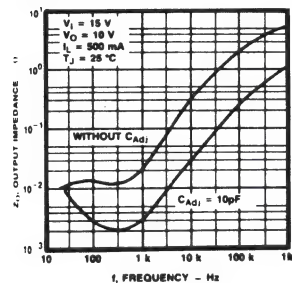
Ripple Rejection as a Function of Output Current



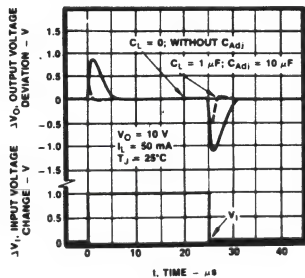
Ripple Rejection as a Function of Frequency



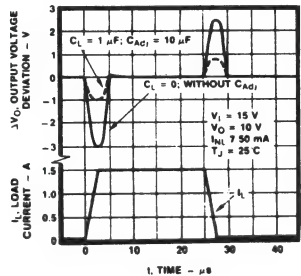
Output Impedance



Line Transient Response



Load Transient Response



GL494

PWM CONTROL CIRCUIT

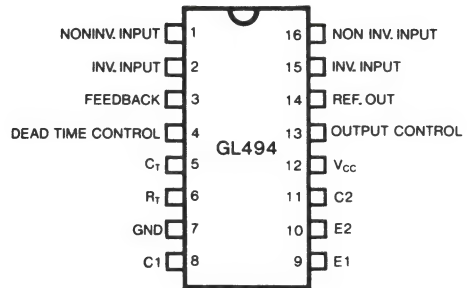
Description

The GL494 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, the GL494 contains an on-chip 5-volt regulator, two error amplifiers, adjustable oscillator, dead-time control comparator, pulse-steering flip-flop, and output-control circuitry. The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Push-pull or single-ended output operation may be selected through the output-control function. The architecture of the GL494 prohibits the possibility of either output being pulsed twice during push-pull operation.

Features

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for 200 mA Sink or Source
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Internal Regulator Provides a Stable 5V Reference Supply
- Variable Dead-Time Provides Control Over Total Range

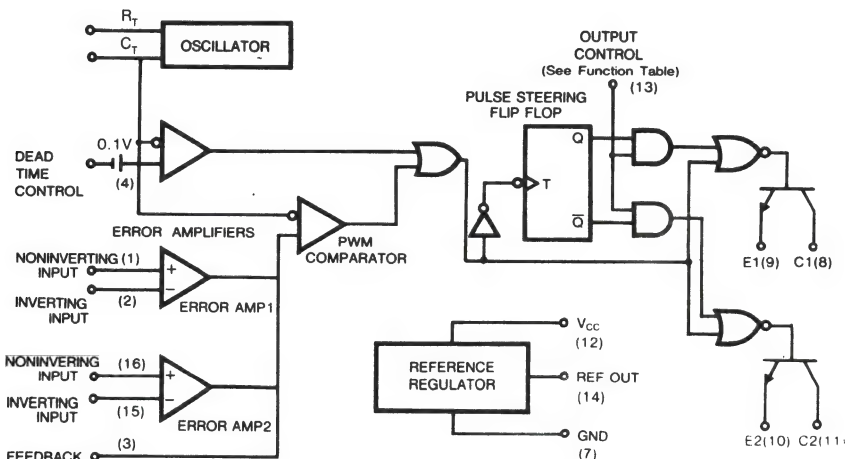
Pin Configuration



Function Table

Output Control	Output Function
Grounded	Single-ended or Parallel Output
At V_{ref}	Normal Push-Pull Operation

Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{CC}	41	V
Amplifier Input Voltage	$V_{CC}+0.3$	V
Collector Output Voltage	41	V
Continuous Total dissipation at (or below) 25°C	1000	mW
Operating Free-Air Temperature Range	-20 to 85	°C
Storage Temperature Range	-65 to 150	°C
Collector Output Current	250	mA

Recommended Operation Conditions

PARAMETER	MIN	MAX	UNIT
Supply Voltage, V_{CC}	7	40	V
Amplifier Input Voltage, V_I	-0.3	$V_{CC}-2$	V
Collector Output Voltage, V_O		40	V
Collector Output Current (Each Transistor)		200	mA
Current Into Feed back Terminal		0.3	mA
Timing Capacitor, C_T	0.47	10,000	nF
Timing Resistor, R_T	1.8	500	K Ω
Oscillator Frequency	1	300	KHz
Operating Free-Air Temperature	-20	85	°C

Electrical Characteristics (Temperature -20~85°C, $V_{CC}=15V$, $f=10KHz$)**Reference Section**

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Output voltage (V_{ref})	$I_O=1\text{ mA}$	4.75	5	5.25	V
Input regulation	$V_{CC}=7V\text{ to }40V$, $T_A=25^\circ\text{C}$		2	25	mV
Output regulation	$I_O=1\text{ to }10\text{mA}$, $T_A=25^\circ\text{C}$		1	15	mV
Output Voltage change with temperature	$T_A=-20^\circ\text{C to }85^\circ\text{C}$		0.2	1	%
Short-circuit output current(2)	$V_{ref}=0$		35		mA

Oscillator Section

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Frequency	$C_T=0.01\mu\text{F}$ $R_T=12\text{k}\Omega$		10		KHz
Standard deviation of frequency (3)	All values of V_{CC} , C_T , R_T , T_A Constant		10		%
Frequency change with voltage	$V_{CC}=7V\text{ to }40V$, $T_A=25^\circ\text{C}$		0.1		%
Frequency change with temperature	$C_T=0.01\mu\text{F}$, $R_T=12\text{k}\Omega$ $T_A=-20^\circ\text{C to }85^\circ\text{C}$			2	%

Dead Time Control Section

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Input bias current (pin 4)	$V_I = 0$ to 5.25V		-2	-10	μA
Maximum duty cycle, each output	$V_{I(\text{pin } 4)} = 0\text{V}$	45			%
Input threshold voltage (pin 4)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			V

Error Amp Sections

PARAMETER	TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
Input offset voltage	$V_{O(\text{PIN}3)} = 2.5\text{V}$			2	10	mV
Input offset current	$V_{O(\text{PIN}3)} = 2.5\text{V}$			25	250	nA
Input bias current	$V_{O(\text{PIN}3)} = 2.5\text{V}$			0.2	1	μA
Common-mode input voltage range	$V_{CC} = 7\text{V}$ to 40V	LOW	-0.3			V
		HIGH	$V_{CC} - 2$			
Open-loop voltage amplification	$\Delta V_O = 3\text{V}$, $V_O = 0.5$ to 3.5V		70	95		dB
Unity-gain bandwidth				800		KHz
Common-mode rejection ratio	$V_{CC} = 40\text{V}$, $T_A = 25^\circ\text{C}$		65	80		dB
Output sink current (pin 3)	$V_{ID} = -15\text{mV}$ to -5V , $V_{O(\text{pin } 3)} = 0.7\text{V}$		0.3	0.7		mA
Output source current (pin 3)	$V_{ID} = 15\text{mV}$ to 5V, $V_{O(\text{pin } 3)} = 3.5\text{V}$		-2			mA

PWM Comparator Section

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Input threshold voltage (pin 3)	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	$V_{O(\text{PIN}3)} = 0.7\text{V}$	0.3	0.7		mA

Switching Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Output voltage rise time	Common-emitter configuration, See Test Circuit 3		100	200	ns
Output voltage fall time			25	100	ns
Output voltage rise time	Emitter-follower configuration, See Test Circuit 4		100	200	ns
Output voltage fall time			40	100	ns

Output Section

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Collector off-state current		$V_{CE}=40V, V_{CC}=40V$		2	100	μA
Emitter off-state current		$V_{CC}=V_C=40V, V_E=0$			-100	μA
Collector-emitter saturation voltage	Common-emitter	$V_E=0, I_C=200mA$		1.1	1.3	V
	Emitter-follower	$V_C=15V, I_E=-200mA$		1.5	2.5	
Output control input current		$V_I=V_{ref}$			3.5	mA

Total Device

PARAMETER	TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
Standby supply current	All other inputs & outputs open	V _{CC} =15V		6	10	mA
		V _{CC} =40V		9	15	mA
Average supply current	V _(pin 4) =2V, See Test Circuit 1			7.5		mA

Notes:

(1) All typical values except for temperature coefficients are at $T_A=25^\circ$

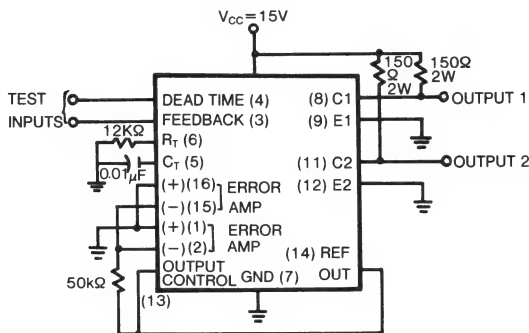
(2) Duration of the short circuit should not exceed one second.

(3) Standard deviation is a measure of the statistical distribution about the mean as derived from the formula

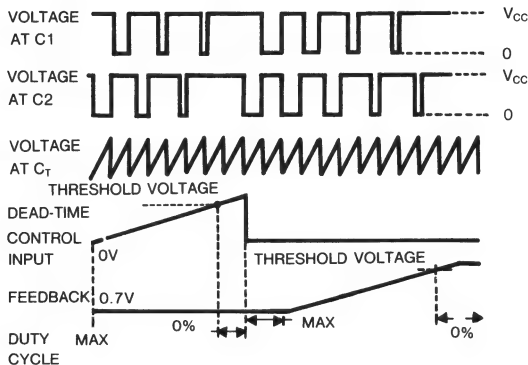
$$\sigma = \sqrt{\frac{\sum_{n=1}^N (X_n - \bar{X})^2}{N-1}}$$

Parameter Measurement Information

1. Dead time and Feedback Control

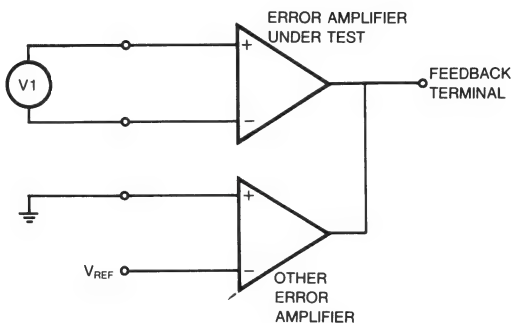


TEST CIRCUIT

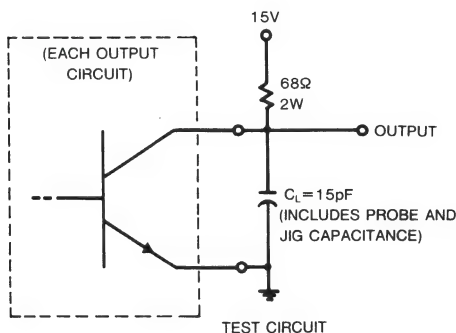


VOLTAGE WAVEFORMS

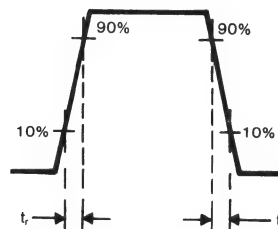
2. Error Amplifier Characteristics



3. Common-Emitter Configuration

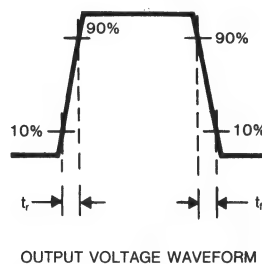
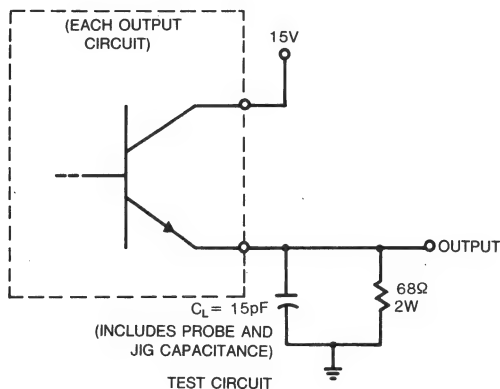


TEST CIRCUIT



OUTPUT VOLTAGE WAVEFORM

4. Emittre-Follower Configuration



Typical Performance Curves

FIGURE 1 - OSCILLATOR FREQUENCY versus TIMING RESISTANCE

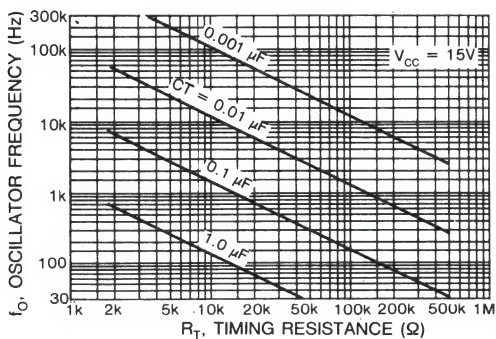


FIGURE 2 - OPEN LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

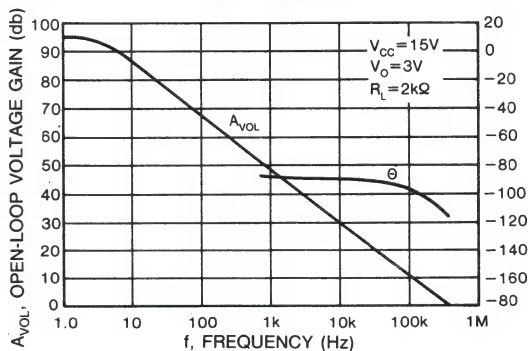


FIGURE 3 - PERCENT DEAD TIME versus OSCILLATOR FREQUENCY

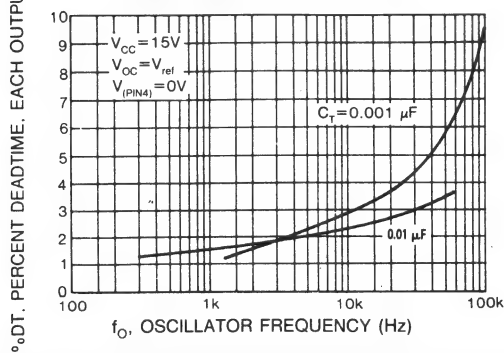
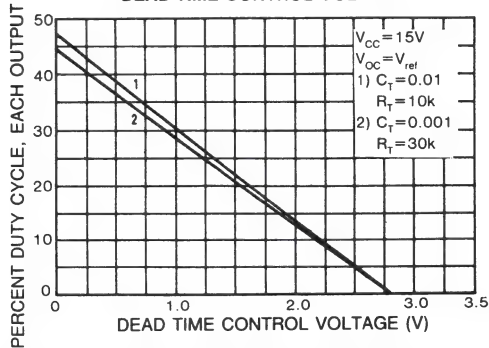
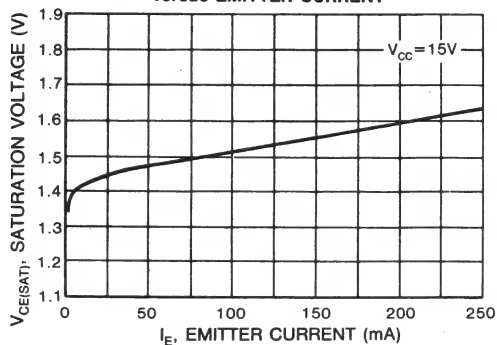


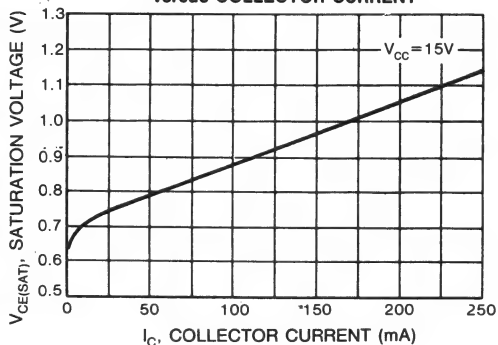
FIGURE 4 - PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE



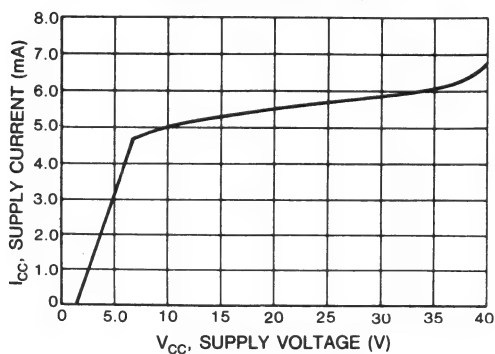
**FIGURE 5 - EMITTER-FOLLOWER CONFIGURATION,
OUTPUT-SATURATION VOLTAGE
versus EMITTER CURRENT**



**FIGURE 6 - COMMON-EMITTER CONFIGURATION
OUTPUT-SATURATION VOLTAGE
versus COLLECTOR CURRENT**



**FIGURE 7 - STANDBY-SUPPLY CURRENT
versus SUPPLY VOLTAGE**



GL78XX Series

POSITIVE VOLTAGE REGULATOR

Description

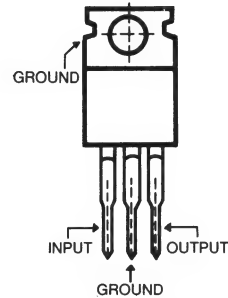
The GL78XX Series are monolithic integrated circuits designed as fixed-voltage regulator. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver over 1.5A output currents. They are intended as fixed voltage regulators in a wide range of applications.

Features

- No External Components Required
- High Line Regulation
- High Load Regulation
- Good Ripple Rejection (70dB)
- Low Temperature Coefficient of Output (1.0mV/°C)
- Wide Range Input Voltage
- Low Input Bias Current
- Low Output Noise
- Output Current in Excess of 1.5A

Pin Configuration

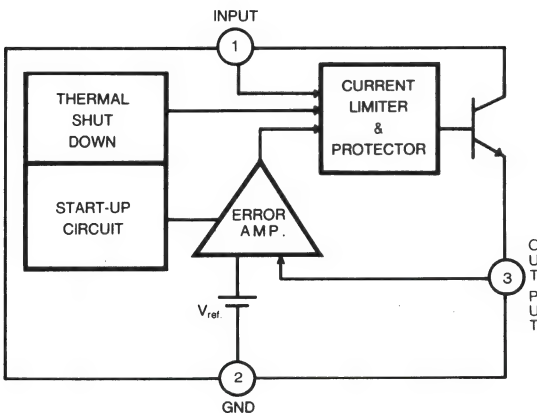
(Top View)



Type No/Voltage

GL7805	5.0 Volts
GL7806	6.0 Volts
GL7808	8.0 Volts
GL7809	9.0 Volts
GL7812	12.0 Volts
GL7815	15.0 Volts
GL7824	24.0 Volts

Block Diagram



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

- Input Voltage (5V Through 15V) 35V
(24V) 40V
- Output Current 3.3A
- Power Dissipation 15W
- Operating Junction Temp. 0°C to $+125^\circ\text{C}$
- Storage Temp. -65°C to $+150^\circ\text{C}$
- Lead Temp. (Soldering, 10S) 230°C

GL7805 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_J = 25^\circ\text{C}$, $V_{in} = 10\text{V}$, $I_o = 500\text{mA}$	4.8	5.2	V
Output Voltage (2)	V_{O2}	$7\text{V} \leq V_{in} \leq 20\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	4.75	5.25	V
Line Regulation	ΔV_{O1}	$T_J = 25^\circ\text{C}$	$7 \leq V_{in} \leq 25\text{V}$, $I_o = 500\text{mA}$		50 mV
	ΔV_{O2}		$8\text{V} \leq V_{in} \leq 12\text{V}$, $I_o = 500\text{mA}$		25 mV
Load Regulation	ΔV_{O3}	$T_J = 25^\circ\text{C}$	$5.0\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = 10\text{V}$		50 mV
	ΔV_{O4}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = 10\text{V}$		25 mV
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$, $V_{in} = 10\text{V}$, $I_o = 500\text{mA}$		8	mA
Quiescent Current Change	ΔI_{Q1}	$7\text{V} \leq V_{in} \leq 25\text{V}$, $I_o = 500\text{mA}$		1.3	mA
	ΔI_{Q2}	$5.0\text{mA} \leq I_o \leq 1.0\text{A}$, $V_{in} = 10\text{V}$		0.5	mA
Output Noise Voltage	N_o	$V_{in} = 10\text{V}$, $I_o = 500\text{mA}$, $10\text{Hz} \leq f \leq 100\text{KHz}$	40(TYP)		μV
Ripple Rejection	R_R	$T_J = 25^\circ\text{C}$, $V_i = 1\text{V}_{(rms)}$, 120Hz , $I_o = 20\text{mA}$, $8\text{V} \leq V_{in} \leq 18\text{V}$	62		dB
Input-Output Voltage Differential	V_d	$T_J = 25^\circ\text{C}$, $I_o = 1.0\text{A}$	2(TYP)		V
Short-Circuit Limit	I_{sc}	$V_{in} = 35\text{V}$, Output-GND		1.0	A
Peak Output Current	I_{peak}	$T_J = 25^\circ\text{C}$, $V_{in} = 12\text{V}$, $V_O = 4.75\text{V}$	1.5	3.3	A

GL7806 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_J = 25^\circ\text{C}$, $V_{in} = 11\text{V}$, $I_o = 500\text{mA}$	5.75	6.25	V
Output Voltage (2)	V_{O2}	$8\text{V} \leq V_{in} \leq 21\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	5.7	6.3	V
Line Regulation	ΔV_{O1}	$T_J = 25^\circ\text{C}$	$8 \leq V_{in} \leq 25\text{V}$, $I_o = 500\text{mA}$		60 mV
	ΔV_{O2}		$9\text{V} \leq V_{in} \leq 13\text{V}$, $I_o = 500\text{mA}$		30 mV
Load Regulation	ΔV_{O3}	$T_J = 25^\circ\text{C}$	$5\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = 11\text{V}$		60 mV
	ΔV_{O4}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = 11\text{V}$		30 mV
Quiescent Current	I_Q	$T_J = 25^\circ\text{C}$, $V_{in} = 11\text{V}$, $I_o = 500\text{mA}$		8.0	mA
Quiescent Current Change	ΔI_{Q1}	$8\text{V} \leq V_{in} \leq 25\text{V}$, $I_o = 500\text{mA}$		1.3	mA
	ΔI_{Q2}	$V_{in} = 11\text{V}$, $5\text{mA} \leq I_o \leq 1.0\text{A}$		0.5	mA
Output Noise Voltage	N_o	$V_{in} = 11\text{V}$, $I_o = 500\text{mA}$, $10\text{Hz} \leq f \leq 100\text{KHz}$	45(TYP)		μV
Ripple Rejection	R_R	$T_J = 25^\circ\text{C}$, $V_i = 1\text{V}_{(rms)}$, 120Hz , $I_o = 20\text{mA}$, $9\text{V} \leq V_{in} \leq 19\text{V}$	57		dB
Input-Output Voltage Differential	V_d	$T_J = 25^\circ\text{C}$, $I_o = 1.0\text{A}$	2(TYP)		V
Short-Circuit Limit	I_{sc}	$V_{in} = 35\text{V}$, Output-GND		1.0	A
Peak Output Current	I_{peak}	$T_J = 25^\circ\text{C}$, $V_{in} = 13\text{V}$, $V_O = 5.7\text{V}$	1.5	3.3	A

GL7808 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^\circ\text{C}$, $V_{in} = 14\text{V}$, $I_o = 500\text{mA}$	7.7	8.3	V
Output Voltage (2)	V_{O2}	$10.5\text{V} \leq V_{in} \leq 23\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	7.6	8.4	V
Line Regulation	ΔV_{O1}	$T_j = 25^\circ\text{C}$	$10.5\text{V} \leq V_{in} \leq 25\text{V}$, $I_o = 500\text{mA}$		80 mV
	ΔV_{O2}		$11\text{V} \leq V_{in} \leq 17\text{V}$, $I_o = 500\text{mA}$		40 mV
Load Regulation	ΔV_{O3}	$T_j = 25^\circ\text{C}$	$5.0\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = 14\text{V}$		80 mV
	ΔV_{O4}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = 14\text{V}$		40 mV
Quiescent Current	I_Q	$T_j = 25^\circ\text{C}$, $V_{in} = 14\text{V}$, $I_o = 500\text{mA}$		8.0	mA
Quiescent Current Change	ΔI_{Q1}	$10.5\text{V} \leq V_{in} \leq 25\text{V}$, $I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$5\text{mA} \leq I_o \leq 1.0\text{A}$, $V_{in} = 14\text{V}$		0.5	mA
Output Noise Voltage	N_o	$V_{in} = 14\text{V}$, $I_o = 500\text{mA}$, $10\text{Hz} \leq f \leq 100\text{KHz}$	52(TYP)		μV
Ripple Rejection	R_R	$T_j = 25^\circ\text{C}$, $V_i = 1\text{V}_{(\text{rms})}$, 120Hz , $I_o = 20\text{mA}$, $11.5\text{V} \leq V_{in} \leq 21.5\text{V}$	55		dB
Input-Output Voltage Differential	V_d	$T_j = 25^\circ\text{C}$, $I_o = 1.0\text{A}$	2(TYP)		V
Short-Circuit Limit	I_{sc}	$V_{in} = 35\text{V}$, Output-GND		1.0	A
Peak Output Current	I_{peak}	$T_j = 25^\circ\text{C}$, $V_{in} = 15\text{V}$, $V_o = 7.6\text{V}$	1.5	3.3	A

GL7809 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^\circ\text{C}$, $V_{in} = 15\text{V}$, $I_o = 500\text{mA}$	8.64	9.36	V
Output Voltage (2)	V_{O2}	$11.5\text{V} \leq V_{in} \leq 24\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	8.55	9.45	V
Line Regulation	ΔV_{O1}	$T_j = 25^\circ\text{C}$	$11.5\text{V} \leq V_{in} \leq 26\text{V}$, $I_o = 500\text{mA}$		90 mV
	ΔV_{O2}		$12\text{V} \leq V_{in} \leq 18\text{V}$, $I_o = 500\text{mA}$		45 mV
Load Regulation	ΔV_{O3}	$T_j = 25^\circ\text{C}$	$5.0\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = 15\text{V}$		90 mV
	ΔV_{O4}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = 15\text{V}$		45 mV
Quiescent Current	I_Q	$T_j = 25^\circ\text{C}$, $V_{in} = 15\text{V}$, $I_o = 500\text{mA}$		8	mA
Quiescent Current Change	ΔI_{Q1}	$11.5\text{V} \leq V_{in} \leq 26\text{V}$, $I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$V_{in} = 15\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$		0.5	mA
Output Noise Voltage	N_o	$V_{in} = 15\text{V}$, $I_o = 500\text{mA}$, $10\text{Hz} \leq f \leq 100\text{KHz}$	60(TYP)		μV
Ripple Rejection	R_R	$T_j = 25^\circ\text{C}$, $V_i = 1\text{V}_{(\text{rms})}$, 120Hz , $I_o = 20\text{mA}$, $12.5\text{V} \leq V_{in} \leq 22.5\text{V}$	55		dB
Input-Output Voltage Differential	V_d	$T_j = 25^\circ\text{C}$, $I_o = 1.0\text{A}$	2(TYP)		V
Short-Circuit Limit	I_{sc}	$V_{in} = 35\text{V}$, Output-GND		1.0	A
Peak Output Current	I_{peak}	$T_j = 25^\circ\text{C}$, $V_{in} = 16\text{V}$, $V_o = 8.55\text{V}$	1.5	3.3	A

GL7812 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^\circ\text{C}$, $V_{in} = 19\text{V}$, $I_o = 500\text{mA}$	11.5	12.5	V
Output Voltage (2)	V_{O2}	$14.5\text{V} \leq V_{in} \leq 27.0\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	11.4	12.6	V
Line Regulation	ΔV_{O1}	$T_j = 25^\circ\text{C}$	$14.5\text{V} \leq V_{in} \leq 30\text{V}$, $I_o = 500\text{mA}$	120	mV
	ΔV_{O2}		$16.0\text{V} \leq V_{in} \leq 22\text{V}$, $I_o = 500\text{mA}$	60	mV
Load Regulation	ΔV_{O3}	$T_j = 25^\circ\text{C}$	$5.0\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = 19\text{V}$	120	mV
	ΔV_{O4}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = 19\text{V}$	60	mV
Quiescent Current	I_Q	$T_j = 25^\circ\text{C}$, $V_{in} = 19\text{V}$, $I_o = 500\text{mA}$		8.0	mA
Quiescent Current Change	ΔI_{Q1}	$14.5\text{V} \leq V_{in} \leq 30\text{V}$, $I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$5.0\text{mA} \leq I_o \leq 1.0\text{A}$, $V_{in} = 19\text{V}$		0.5	mA
Output Noise Voltage	No	$V_{in} = 19\text{V}$, $I_o = 500\text{mA}$, $10\text{Hz} \leq f \leq 100\text{KHz}$	75(TYP)		μV
Ripple Rejection	R_R	$T_j = 25^\circ\text{C}$, $V_i = 1\text{V}_{(\text{rms})}$, 120Hz , $I_o = 20\text{mA}$, $15\text{V} \leq V_{in} \leq 25\text{V}$	55		dB
Input-Output Voltage Differential	V_d	$T_j = 25^\circ\text{C}$, $I_o = 1.0\text{A}$	2(TYP)		V
Short-Circuit Limit	I_{sc}	$V_{in} = 35\text{V}$, Output-GND		1.0	A
Peak Output Current	I_{peak}	$T_j = 25^\circ\text{C}$, $V_{in} = 19\text{V}$, $V_O = 11.4\text{V}$	1.5	3.3	A

GL7815 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^\circ\text{C}$, $V_{in} = 23\text{V}$, $I_o = 500\text{mA}$	14.4	15.6	V
Output Voltage (2)	V_{O2}	$17.5\text{V} \leq V_{in} \leq 30\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	14.25	15.75	V
Line Regulation	ΔV_{O1}	$T_j = 25^\circ\text{C}$	$17.5\text{V} \leq V_{in} \leq 30\text{V}$, $I_o = 500\text{mA}$	150	mV
	ΔV_{O2}		$20\text{V} \leq V_{in} \leq 26\text{V}$, $I_o = 500\text{mA}$	75	mV
Load Regulation	ΔV_{O3}	$T_j = 25^\circ\text{C}$	$5\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = 23\text{V}$	150	mV
	ΔV_{O4}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = 23\text{V}$	75	mV
Quiescent Current	I_Q	$T_j = 25^\circ\text{C}$, $V_{in} = 23\text{V}$, $I_o = 500\text{mA}$		8.0	mA
Quiescent Current Change	ΔI_{Q1}	$17.5\text{V} \leq V_{in} \leq 30\text{V}$, $I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$5.0\text{mA} \leq I_o \leq 1.0\text{A}$, $V_{in} = 23\text{V}$		0.5	mA
Output Noise Voltage	No	$V_{in} = 23\text{V}$, $I_o = 500\text{mA}$, $10\text{Hz} \leq f \leq 100\text{KHz}$	90(TYP)		μV
Ripple Rejection	R_R	$T_j = 25^\circ\text{C}$, $V_i = 1\text{V}_{(\text{rms})}$, 120Hz , $I_o = 20\text{mA}$, $18.5\text{V} \leq V_{in} \leq 28.5\text{V}$	54		dB
Input-Output Voltage Differential	V_d	$T_j = 25^\circ\text{C}$, $I_o = 1.0\text{A}$	2(TYP)		V
Short-Circuit Limit	I_{sc}	$V_{in} = 35\text{V}$, Output-GND		1.0	A
Peak Output Current	I_{peak}	$T_j = 25^\circ\text{C}$, $V_{in} = 22\text{V}$, $V_O = 14.25\text{V}$	1.5	3.3	A

GL7818 Electrical Characteristics($T_A=25^{\circ}\text{C}$)

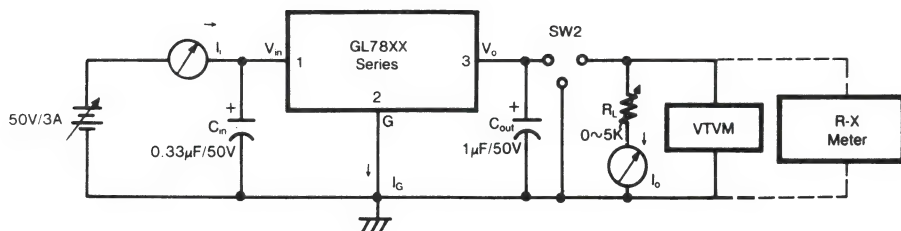
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage(1)	V_{O1}	$T_j = 25^{\circ}\text{C}$, $V_{in} = 25\text{V}$, $I_o = 500\text{mA}$	17.3	18.7	V
Output Voltage(2)	V_{O2}	$20.5\text{V} \leq V_{in} \leq 33\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	17.1	18.9	V
Line Regulation	ΔV_{O1}	$T_j = 25^{\circ}\text{C}$	$20.5\text{V} \leq V_{in} \leq 33\text{V}$, $I_o = 500\text{mA}$		180 mV
	ΔV_{O2}		$24.0\text{V} \leq V_{in} \leq 30\text{V}$, $I_o = 500\text{mA}$		90 mV
Load Regulation	ΔV_{O3}	$T_j = 25^{\circ}\text{C}$	$5.0\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = 21\text{V}$		180 mV
	ΔV_{O4}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = 25\text{V}$		90 mV
Quiescent Current	I_Q	$T_j = 25^{\circ}\text{C}$, $V_{in} = 25\text{V}$, $I_o = 50\text{mA}$		8.0	mA
Quiescent Current Change	ΔI_{Q1}	$20.5\text{V} \leq V_{in} \leq 33\text{V}$, $I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$5.0\text{mA} \leq I_o \leq 1.0\text{A}$, $V_{in} = 25\text{V}$		0.5	mA
Output Noise Voltage	N_O	$V_{in} = 25\text{V}$, $I_o = 500\text{mA}$, $10\text{Hz} \leq f \leq 100\text{KHz}$	110(TYP)		μV
Ripple Rejection	R_R	$T_j = 25^{\circ}\text{C}$, $V_i = 1\text{V}_{(\text{rms})}$, 120Hz , $I_o = 20\text{mA}$ $21\text{V} \leq V_{in} \leq 33\text{V}$	59		dB
Input-Output Voltage Differential	V_d	$T_j = 25^{\circ}\text{C}$, $I_o = 1.0\text{A}$	2(TYP)		V
Short-Circuit Limit	I_{sc}	$V_{in} = 25\text{V}$, Output-GND		1.0	A
Peak Output Current	I_{peak}	$T_j = 25^{\circ}\text{C}$, $V_{in} = 25\text{V}$, $V_o = 17.1\text{V}$	1.5	3.3	A

GL7824 Electrical Characteristics ($T_A = 25^{\circ}\text{C}$)

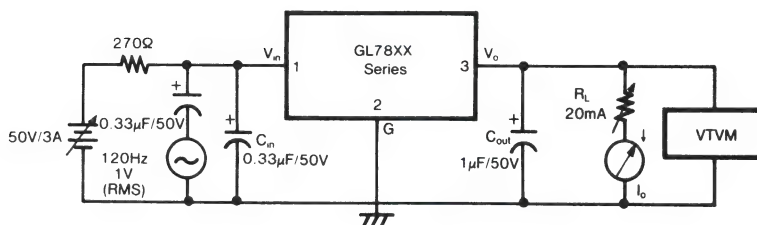
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^{\circ}\text{C}$, $V_{in} = 33\text{V}$, $I_o = 500\text{mA}$	23	25	V
Output Voltage (2)	V_{O2}	$27\text{V} \leq V_{in} \leq 38\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	22.8	25.2	V
Line Regulation	ΔV_{O1}	$T_j = 25^{\circ}\text{C}$	$27\text{V} \leq V_{in} \leq 38\text{V}$, $I_o = 500\text{mA}$		240 mV
	ΔV_{O2}		$30\text{V} \leq V_{in} \leq 36\text{V}$, $I_o = 500\text{mA}$		120 mV
Load Regulation	ΔV_{O3}	$T_j = 25^{\circ}\text{C}$	$5\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = 33\text{V}$		240 mV
	ΔV_{O4}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = 33\text{V}$		120 mV
Quiescent Current	I_Q	$T_j = 25^{\circ}\text{C}$, $V_{in} = 33\text{V}$, $I_o = 500\text{mA}$		8.0	mA
Quiescent Current Change	ΔI_{Q1}	$27\text{V} \leq V_{in} \leq 38\text{V}$, $I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$5.0\text{mA} \leq I_o \leq 1.0\text{A}$, $V_{in} = 33\text{V}$		0.5	mA
Output Noise Voltage	N_O	$V_{in} = 33\text{V}$, $I_o = 500\text{mA}$, $10\text{Hz} \leq f \leq 100\text{KHz}$	170(TYP)		μV
Ripple Rejection	R_R	$T_j = 25^{\circ}\text{C}$, $V_i = 1\text{V}_{(\text{rms})}$, 120Hz , $I_o = 20\text{mA}$, $28\text{V} \leq V_{in} \leq 38\text{V}$	56		dB
Input-Output Voltage Differential	V_d	$T_j = 25^{\circ}\text{C}$, $I_o = 1.0\text{A}$	2(TYP)		V
Short-Circuit Limit	I_{sc}	$V_{in} = 35\text{V}$, Output-GND		1.0	A
Peak Output Current	I_{peak}	$T_j = 25^{\circ}\text{C}$, $V_{in} = 31\text{V}$, $V_o = 22.8\text{V}$	1.5	3.3	A

*GL78XX Series Test Circuit (AC & DC)

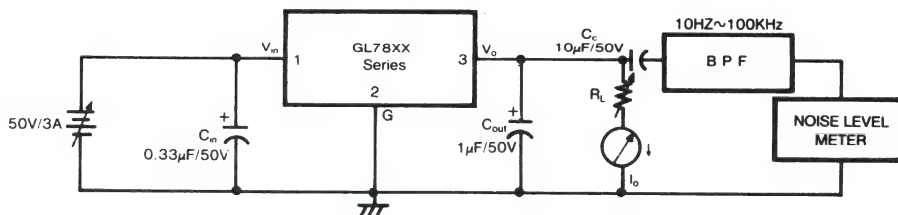
1. V_{01} , V_{02} , ΔV_o , I_Q , ΔI_Q , V_d , I_{SC} , I_{peak}



2. Ripple Rejection



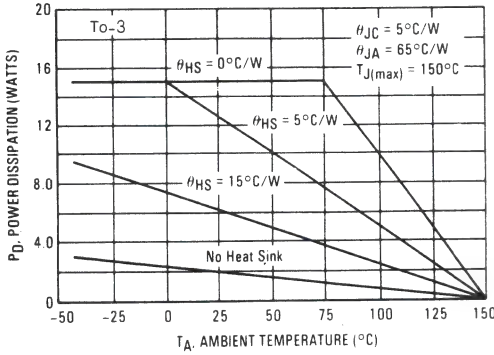
3. Output Noise Voltage



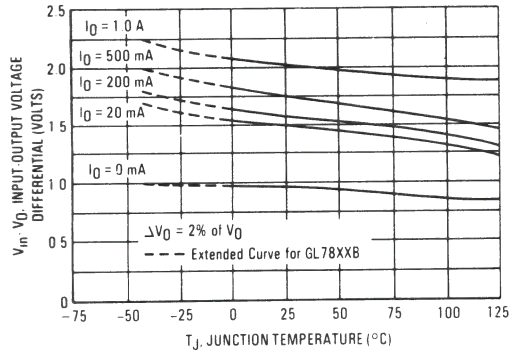
* C_{in} , C_{out} , C_c is Tantalum Capacitor

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

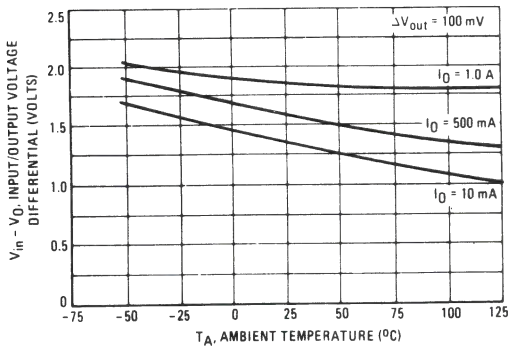
**FIGURE 1 — AVERAGE POWER DISSIPATION
versus AMBIENT TEMPERATURE**



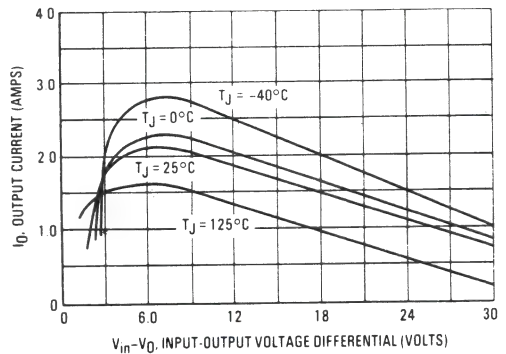
**FIGURE 2 — INPUT OUTPUT DIFFERENTIAL AS A
FUNCTION OF JUNCTION TEMPERATURE**



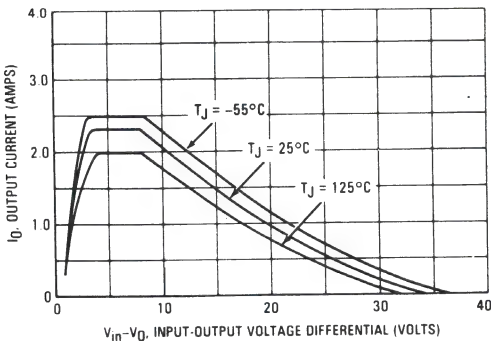
**FIGURE 3 — INPUT OUTPUT DIFFERENTIAL AS A
FUNCTION OF JUNCTION TEMPERATURE**



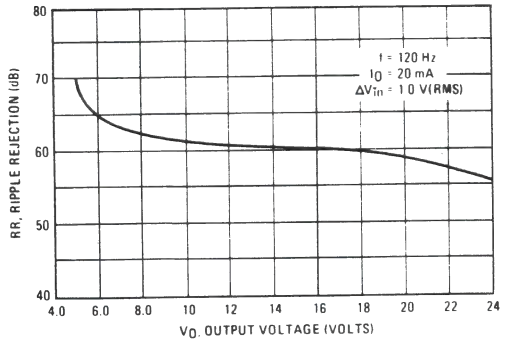
**FIGURE 4 — PEAK OUTPUT CURRENT AS A FUNCTION
OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE**



**FIGURE 5 — PEAK OUTPUT CURRENT AS A
FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE**



**FIGURE 6 — RIPPLE REJECTION AS A FUNCTION
OF OUTPUT VOLTAGES**



TYPICAL CHARACTERISTICS (continued) ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

FIGURE 7 — RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

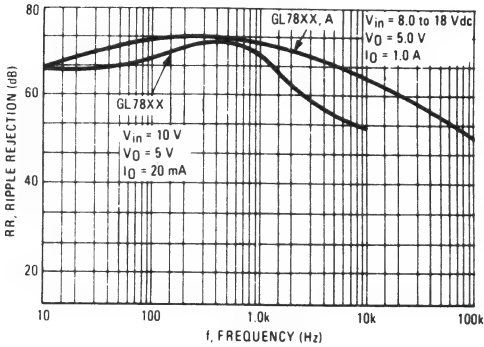


FIGURE 8 — OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

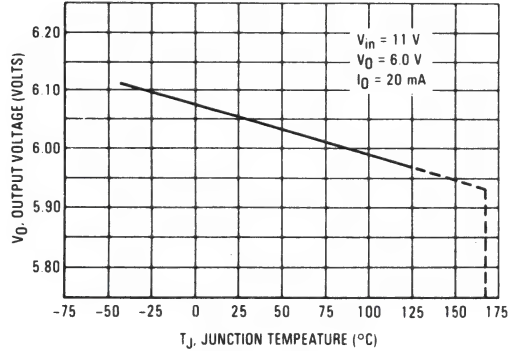


FIGURE 9 — OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE

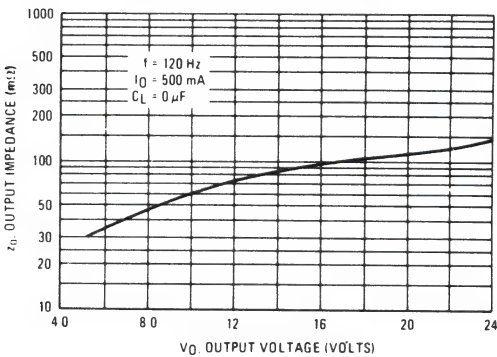


FIGURE 10 — QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

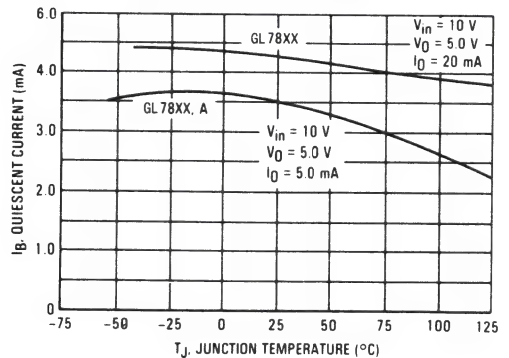
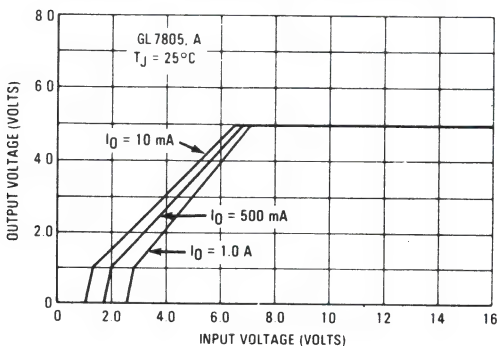


FIGURE 11 — DROPOUT CHARACTERISTICS



GL79XX Series

NEGATIVE VOLTAGE REGULATOR

Description

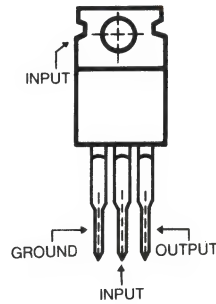
The GL79XX series of fixed output negative voltage regulators are intended as complements to the popular GL78XX series devices. Available in fixed output voltage options from -5 to -24 Volts, these regulators employ internal current limiting, thermal shutdown, and safe-area compensation-making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0A.

Features

- High Line Regulation
- High Load Regulation
- Good Ripple Rejection (70dB)
- Low Temperature Coefficient of Output* ($-1.0\text{mV}/^{\circ}\text{C}$)
- Wide Range Input Voltage
- Low Input Bias Current
- Low Output Noise
- Output Current in Excess of 1A.

Pin Configuration

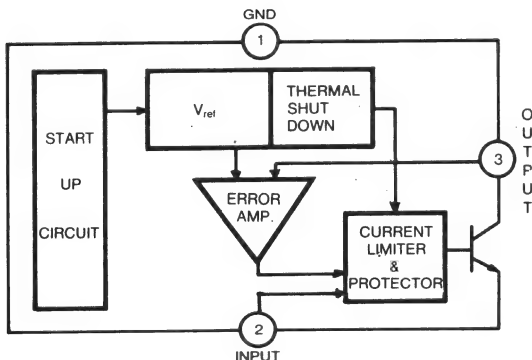
(Top View)



Type No/Voltage

GL7905	-5.0 Volts
GL7909	-9.0 Volts
GL7912	-12.0 Volts
GL7915	-15.0 Volts
GL7924	-24.0 Volts

Block Diagram



Maximum Ratings ($T_A = 25^{\circ}\text{C}$)

- Input Voltage
(-5V Through -15V) -35V
(-24V) -40V
- Output Current 2.2A
- Power Dissipation Internally Limited
- Operating Junction Temp. 0°C to $+150^{\circ}\text{C}$
- Storage Temp. -65°C to $+150^{\circ}\text{C}$
- Lead Temp. 230°C
(Soldering, 10S)

GL7905 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^\circ\text{C}$, $V_{in} = -10\text{V}$, $I_o = 500\text{mA}$	-5.2	-4.8	V
Output Voltage (2)	V_{O2}	$-20\text{V} \leq V_{in} \leq -7\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	-5.25	-4.75	V
Line Regulation	ΔV_{O1}	$T_j = 25^\circ\text{C}$	$-25\text{V} \leq V_{in} \leq -7\text{V}$, $I_o = 100\text{mA}$		50 mV
	ΔV_{O2}		$-12\text{V} \leq V_{in} \leq -8\text{V}$, $I_o = 100\text{mA}$		25 mV
	ΔV_{O3}		$-25\text{V} \leq V_{in} \leq -7\text{V}$, $I_o = 500\text{mA}$		100 mV
	ΔV_{O4}		$-12\text{V} \leq V_{in} \leq -8\text{V}$, $I_o = 500\text{mA}$		50 mV
Load Regulation	ΔV_{O5}	$T_j = 25^\circ\text{C}$	$5.0\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = -10\text{V}$		100 mV
	ΔV_{O6}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = -10\text{V}$		50 mV
Quiescent Current	I_Q	$T_j = 25^\circ\text{C}$, $V_{in} = -10\text{V}$, $I_o = 500\text{mA}$		2.0	mA
Quiescent Current Change	ΔI_{Q1}	$-25\text{V} \leq V_{in} \leq -17\text{V}$, $I_o = 500\text{mA}$		1.3	mA
	ΔI_{Q2}	$V_{in} = -10\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$		0.5	mA
Output Noise Voltage	N_o	$V_{in} = -10\text{V}$, $I_o = 500\text{mA}$ $10\text{Hz} \leq f \leq 100\text{KHz}$		80	μV
Ripple Rejection	R_R	$T_j = 25^\circ\text{C}$, $V_i = 1\text{V}_{(\text{rms})}$, 120Hz , $I_o = 20\text{mA}$, $-18\text{V} \leq V_{in} \leq -8\text{V}$	54		dB
Input-Output Voltage Differential	V_d	$T_j = 25^\circ\text{C}$, $I_o = 1.0\text{A}$		1.1 (TYP)	V

GL7909 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^\circ\text{C}$, $V_{in} = -15\text{V}$, $I_o = 500\text{mA}$	-9.35	-8.65	V
Output Voltage (2)	V_{O2}	$-24\text{V} \leq V_{in} \leq -11.5\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	-9.55	-8.55	V
Line Regulation	ΔV_{O1}	$T_j = 25^\circ\text{C}$	$-26\text{V} \leq V_{in} \leq -11.5\text{V}$, $I_o = 100\text{mA}$		90 mV
	ΔV_{O2}		$-18\text{V} \leq V_{in} \leq -12\text{V}$, $I_o = 100\text{mA}$		45 mV
	ΔV_{O3}		$-26\text{V} \leq V_{in} \leq -11.5\text{V}$, $I_o = 500\text{mA}$		180 mV
	ΔV_{O4}		$-18\text{V} \leq V_{in} \leq -12\text{V}$, $I_o = 500\text{mA}$		90 mV
Load Regulation	ΔV_{O5}	$T_j = 25^\circ\text{C}$	$5.0\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = -15\text{V}$		180 mV
	ΔV_{O6}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = -15\text{V}$		90 mV
Quiescent Current	I_Q	$T_j = 25^\circ\text{C}$, $V_{in} = -15\text{V}$, $I_o = 500\text{mA}$		3	mA
Quiescent Current Change	ΔI_{Q1}	$-26\text{V} \leq V_{in} \leq -11.5\text{V}$, $I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$V_{in} = -15\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$		0.5	mA
Output Noise Voltage	N_o	$V_{in} = -15\text{V}$, $I_o = 500\text{mA}$ $10\text{Hz} \leq f \leq 100\text{KHz}$		120	μV
Ripple Rejection	R_R	$T_j = 25^\circ\text{C}$, $V_i = 1\text{V}_{(\text{rms})}$, 120Hz , $I_o = 20\text{mA}$, $-22\text{V} \leq V_{in} \leq -12\text{V}$	54		dB
Input-Output Voltage Differential	V_d	$T_j = 25^\circ\text{C}$, $I_o = 1.0\text{A}$		1.1 (TYP)	V

GL7912 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^\circ\text{C}$, $V_{in} = -19\text{V}$, $I_o = 500\text{mA}$	-12.5	-11.5	V
Output Voltage (2)	V_{O2}	$-27\text{V} \leq V_{in} \leq -14.5\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	-12.5	-11.4	V
Line Regulation	ΔV_{O1}	$T_j = 25^\circ\text{C}$	$-30\text{V} \leq V_{in} \leq -14.5\text{V}$, $I_o = 100\text{mA}$		120 mV
	ΔV_{O2}		$-22\text{V} \leq V_{in} \leq -16\text{V}$, $I_o = 100\text{mA}$		60 mV
	ΔV_{O3}		$-30\text{V} \leq V_{in} \leq -14.5\text{V}$, $I_o = 500\text{mA}$		240 mV
	ΔV_{O4}		$-22\text{V} \leq V_{in} \leq -16\text{V}$, $I_o = 500\text{mA}$		120 mV
Load Regulation	ΔV_{O5}	$T_j = 25^\circ\text{C}$	$5.0\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = -19\text{V}$		240 mV
	ΔV_{O6}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = -19\text{V}$		120 mV
Quiescent Current	I_Q	$T_j = 25^\circ\text{C}$, $V_{in} = -19\text{V}$, $I_o = 500\text{mA}$		3	mA
Quiescent Current Change	ΔI_{Q1}	$-30\text{V} \leq V_{in} \leq -14.5\text{V}$, $I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$V_{in} = -19\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$		0.5	mA
Output Noise Voltage	N_o	$V_{in} = -19\text{V}$, $I_o = 500\text{mA}$ $10\text{Hz} \leq f \leq 100\text{kHz}$		150	μV
Ripple Rejection	R_R	$T_j = 25^\circ\text{C}$, $V_i = 1V_{(rms)}$, 120Hz , $I_o = 20\text{mA}$, $-25\text{V} \leq V_{in} \leq -15\text{V}$	54		dB
Input-Output Voltage Differential	V_d	$T_j = 25^\circ\text{C}$, $I_o = 1.0\text{A}$		1.1(TYP)	V

GL7915 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^\circ\text{C}$, $V_{in} = -23\text{V}$, $I_o = 500\text{mA}$	-15.6	-14.4	V
Output Voltage (2)	V_{O2}	$-30\text{V} \leq V_{in} \leq -17.5\text{V}$, $5.0\text{mA} \leq I_o \leq 1.0\text{A}$	-15.75	-14.25	V
Line Regulation	ΔV_{O1}	$T_j = 25^\circ\text{C}$	$-30\text{V} \leq V_{in} \leq -17.5\text{V}$, $I_o = 100\text{mA}$		150 mV
	ΔV_{O2}		$-26\text{V} \leq V_{in} \leq -20\text{V}$, $I_o = 100\text{mA}$		75 mV
	ΔV_{O3}		$-30\text{V} \leq V_{in} \leq -17.5\text{V}$, $I_o = 500\text{mA}$		300 mV
	ΔV_{O4}		$-26\text{V} \leq V_{in} \leq -20\text{V}$, $I_o = 500\text{mA}$		150 mV
Load Regulation	ΔV_{O5}	$T_j = 25^\circ\text{C}$	$5.0\text{mA} \leq I_o \leq 1.5\text{A}$, $V_{in} = -23\text{V}$		300 mV
	ΔV_{O6}		$250\text{mA} \leq I_o \leq 750\text{mA}$, $V_{in} = -23\text{V}$		150 mV
Quiescent Current	I_Q	$T_j = 25^\circ\text{C}$, $V_{in} = -23\text{V}$, $I_o = 500\text{mA}$		3	mA
Quiescent Current Change	ΔI_{Q1}	$-30\text{V} \leq V_{in} \leq -17.5\text{V}$, $I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$V_{in} = -23\text{V}$, $5\text{mA} \leq I_o \leq 1.5\text{A}$		0.5	mA
Output Noise Voltage	N_o	$V_{in} = -23\text{V}$, $I_o = 500\text{mA}$ $10\text{Hz} \leq f \leq 100\text{kHz}$		180	μV
Ripple Rejection	R_R	$T_j = 25^\circ\text{C}$, $V_i = 1V_{(rms)}$, 120Hz , $I_o = 20\text{mA}$, $-28.5\text{V} \leq V_{in} \leq -18.5\text{V}$	54		dB
Input-Output Voltage Differential	V_d	$T_j = 25^\circ\text{C}$, $I_o = 1.0\text{A}$		1.1(TYP)	V

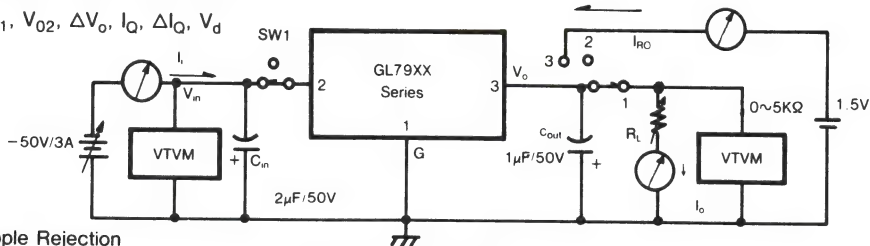
GL7924 Electrical Characteristics ($T_A = 25^\circ\text{C}$)

$$C_{in} = 2\mu\text{F}, C_{out} = 1\mu\text{F}$$

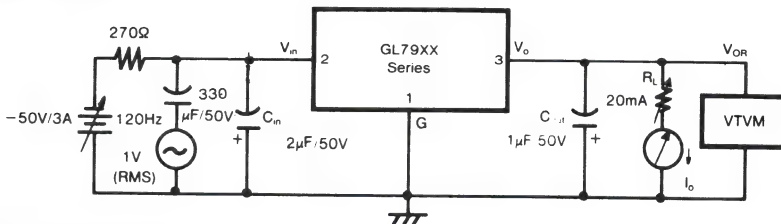
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNIT
			MIN.	MAX.	
Output Voltage (1)	V_{O1}	$T_j = 25^\circ\text{C}, V_{in} = -33\text{V}, I_o = 500\text{mA}$	-25	-23	V
Output Voltage (2)	V_{O2}	$-38\text{V} \leq V_{in} \leq -27\text{V}, 5.0\text{mA} \leq I_o \leq 1.0\text{A}$	-25.2	-22.8	V
Line Regulation	ΔV_{O1}	$T_j = 25^\circ\text{C}$		240	mV
	ΔV_{O2}			120	mV
	ΔV_{O3}			480	mV
	ΔV_{O4}			240	mV
Load Regulation	ΔV_{O5}	$T_j = 25^\circ\text{C}$		480	mV
	ΔV_{O6}			240	mV
Quiescent Current	I_Q	$T_j = 25^\circ\text{C}, V_{in} = -33\text{V}, I_o = 500\text{mA}$		3	mA
Quiescent Current Change	ΔI_{Q1}	$-38\text{V} \leq V_{in} \leq -27\text{V}, I_o = 500\text{mA}$		1.0	mA
	ΔI_{Q2}	$V_{in} = -33\text{V}, 5\text{mA} \leq I_o \leq 1.5\text{A}$		0.5	mA
Output Noise Voltage	N_o	$V_{in} = -33\text{V}, I_o = 500\text{mA}$ $10\text{Hz} \leq f \leq 100\text{kHz}$		270	μV
Ripple Rejection	R_R	$T_j = 25^\circ\text{C}, V_i = 1\text{V}_{(\text{rms})}, 120\text{Hz}, I_o = 20\text{mA}$, $-38\text{V} \leq V_{in} \leq -28\text{V}$	54		dB
Input-Output Voltage Differential	V_d	$T_j = 25^\circ\text{C}, I_o = 1.0\text{A}$		1.1(TYP)	V

*GL79XX Series Test Circuit (AC & DC)

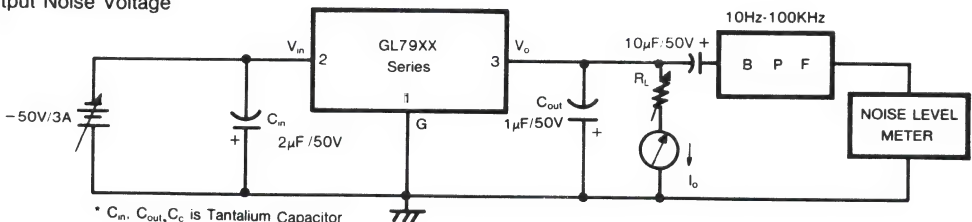
1. $V_{O1}, V_{O2}, \Delta V_o, I_Q, \Delta I_Q, V_d$



2. Ripple Rejection



3. Output Noise Voltage



* C_{in}, C_{out}, C_c is Tantalum Capacitor

TYPICAL CHARACTERISTICS ($T_A = +25^{\circ}\text{C}$ unless otherwise noted.)

FIGURE 1 — AVERAGE CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220)

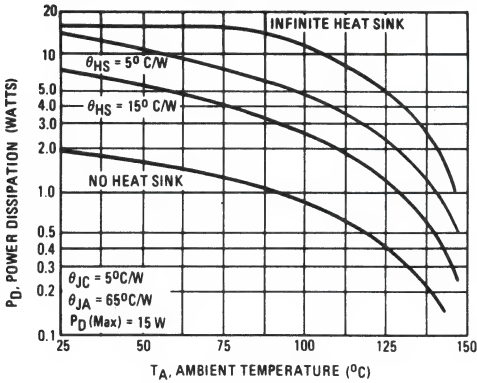


FIGURE 2 — PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

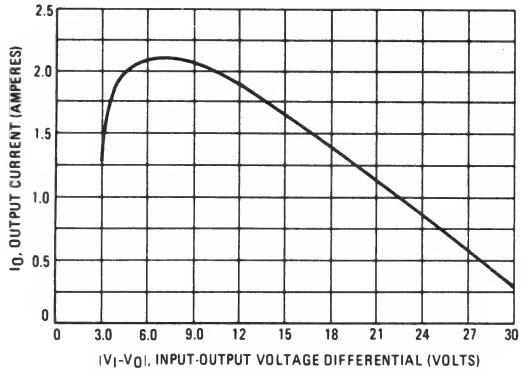


FIGURE 3 — RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

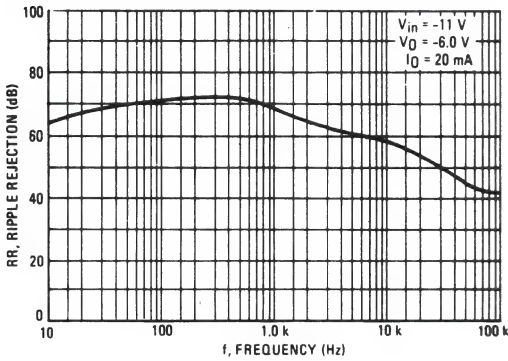


FIGURE 4 — RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

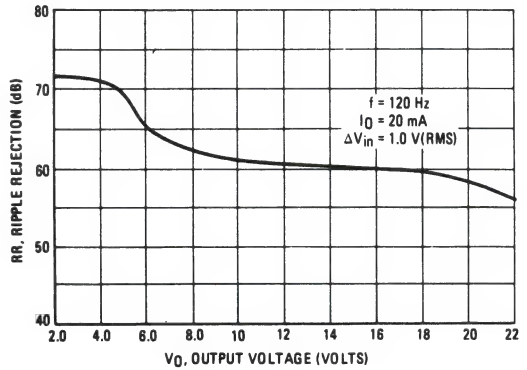
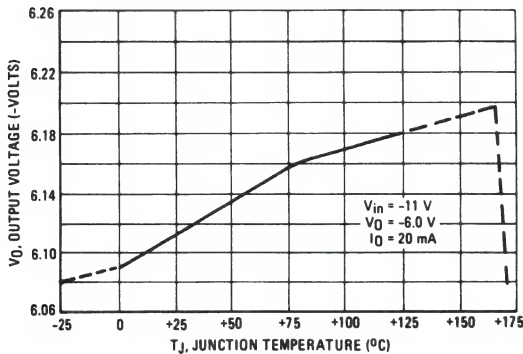


FIGURE 5 — OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



GL7401

BIDIRECTIONAL MOTOR DRIVER WITH BRAKE

Description

The GL7401 is a bidirectional motor driver IC. It is especially suited for use in motor drive applications where the front loading function of VTR's and the auto reverse function of cassette decks are performed.

Feature

- Built-In Braking Function
- Built-In Diode to Absorb dash Current
- Wide Operating Voltage Range (4 ~ 18V)
- Direct Drivable with TTL.

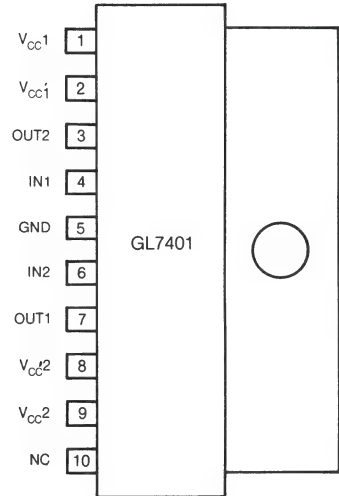
Absolute Maximum Ratings

Supply Voltage	V_{CC}	20	V
Input Voltage	V_{IN}	-0.3 to V_{CC}	V
Output Current	I_O	1.6	A
Power Dissipation		7.0	W
Operating Temperature	T_{opr}	-25 to 75	°C
Storage Temperature	T_{stg}	-55 to 125	°C

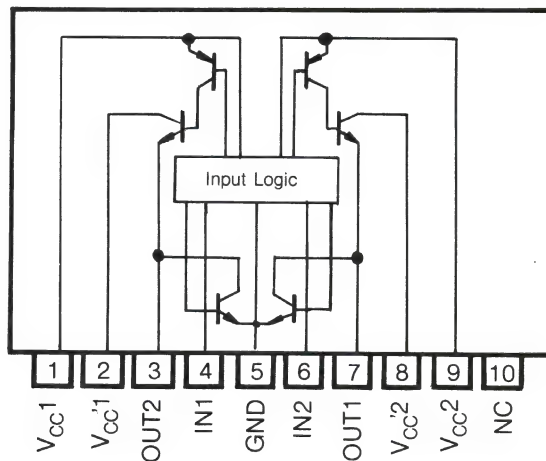
Without Heat Sink 2.5W

With Heat Sink 7.0W (100×100×1.3mm³ Al)

Pin Configuration



Block Diagram



Recomended Operating Conditions at T_A = 25°C

Supply Voltage	V _{CC}	4 to 18	V
“H”-Level Input Voltage	V _{IH}	3 to V _{CC}	V
“L”-Level Input Voltage	V _{IL}	− 0.3 to + 0.4	V
Output Current	I _O	− 500 to + 500	mA
Forward↔Reverse Inhibit Time	T _{OFF}	10 or more	us

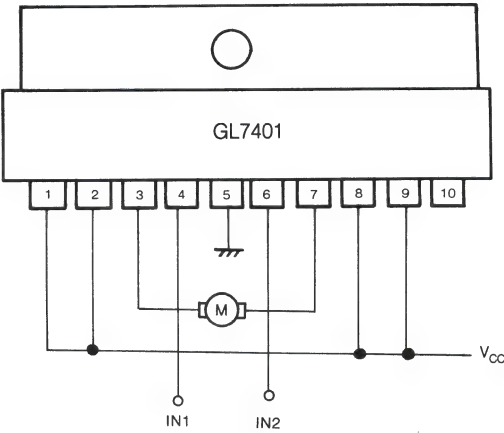
Electrical Characteristics: T_A = 25°C, V_{CC} = V_{CC}' = 12V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Current Dissipation	I _{CC}	V _{I1} or V _{I2} = 3V, R _L = ∞, V _{CC} = V _{CC} ' = 16V			40	mA
“H”-Level Output Voltage 1	V _{OH1}	V _{I1} or V _{I2} = 2V, I _O = − 50mA	10.8			V
“H”-Level Output Voltage 2	V _{OH2}	V _{I1} or V _{I2} = 2V, I _O = − 100mA	10.7			V
“L”-Level Output Voltage 1	V _{OL1}	V _{I1} or V _{I2} = 2V, I _O = 50mA			0.5	V
“L”-Level Output Voltage 2	V _{OL2}	V _{I1} or V _{I2} = 2V, I _O = 100mA			0.65	V
Interoutput Voltage	V _{O1} -V _{O2}	V _{I1} or V _{I2} = 2V, I _O = ± 100mA	10.3			V
Input Voltage	V _I	I _I = 500μA	3			V
Output Leakage Current	I _O Leak	V _{CC} = V _{CC} ' = 18V, V _O = 0V, V _{IN1} = V _{IN2} = 0V, V _O = 18V			± 100	μA

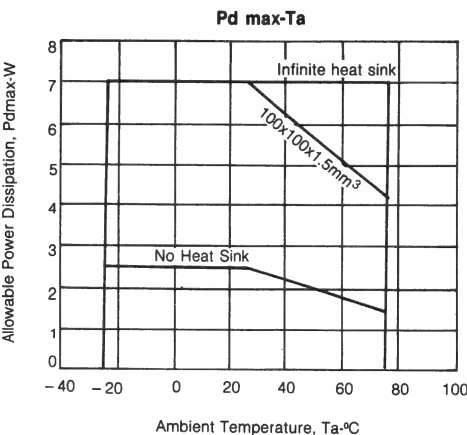
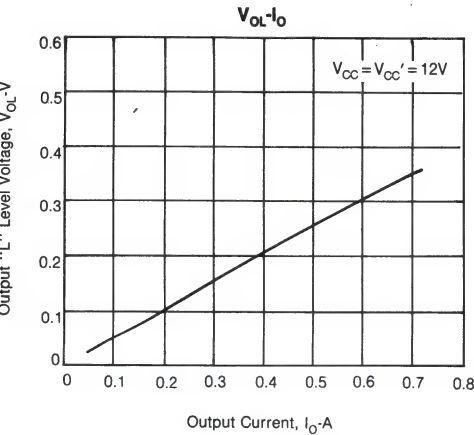
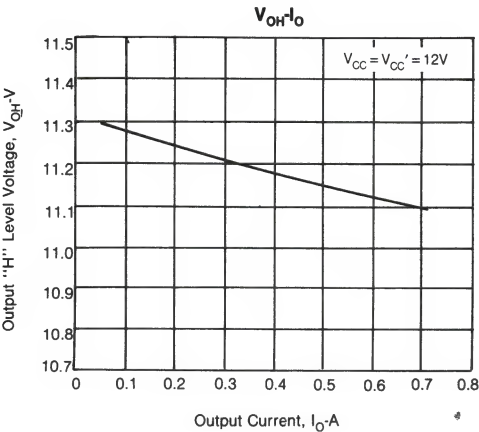
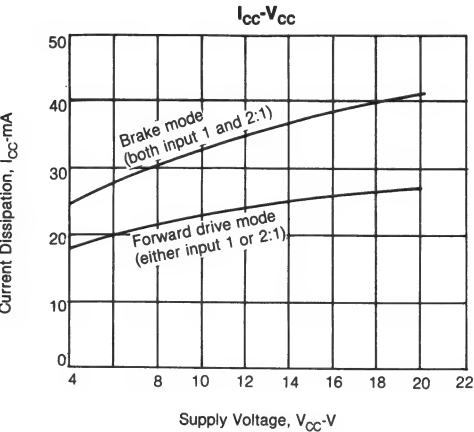
Control Mode

Input		Output		Remarks
1	2	1	2	
0	0	—	—	Open
1	0	1	0	Forward drive
0	1	0	1	Reverse drive
1	1	0	0	Braking

Typical Applications



Typical Performance Curves



DUAL BI-DIRECTIONAL MOTOR DRIVER

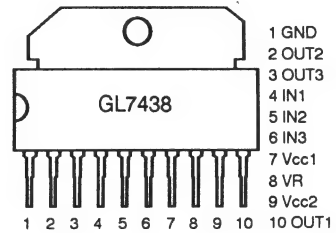
Functions

- Dual Bi-directional Motor Driver
- Elevation/Loading Motor Driver for VTR

Features

- Required Simple External Parts
- Possible to Control Three Mode (Forward Drive, Backward Drive and Brake)
- There are Diodes to Protect Surge
- Possible to Interface with CMOS Output

Pin Configuration



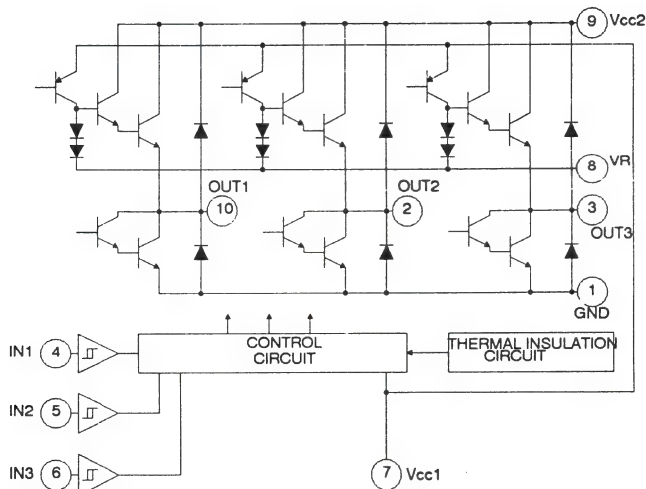
Absolute Maximum Ratings : $T_A = 25^\circ\text{C}$

Item	Symbol	Value	Unit
Supply voltage	V_{CC}	20	V
Power Dissipation	P_D	1,900	mW
Operating Temperature	T_{OPR}	$-25 \sim +75$	$^\circ\text{C}$
Storage Temperature	T_{STG}	$-55 \sim +125$	$^\circ\text{C}$
Input Voltage	V_{IN}	$-0.3 \sim +5$	V
Output Current	I_{Omax}	1.6	A

Recommended Operating Conditions

Parameter	Symbol	Range	Unit
IC Operating Voltage	V_{CC1}	$8 \sim 18$	V
Motor Operating Voltage	V_{CC2}	$8 \sim 18$	V
Reference Voltage	V_R	$0 \sim 18$	V
"LOW" Input Voltage	V_{IL}	$0 \sim 1.0$	V
"HIGH" Input Voltage	V_{IH}	$3.5 \sim 5.0$	V

Block Diagram



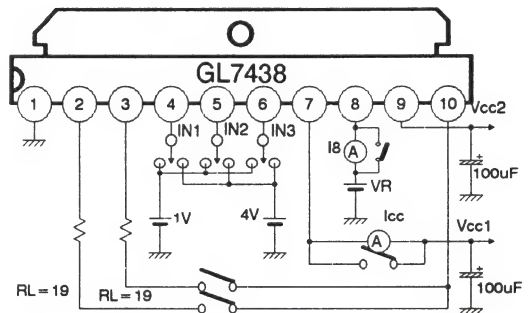
Electrical Characteristics : $T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Circuit Current	I_{CC}	2,3,10pin = open, 4,5,6pin = "L" Level	-	12	24	V
Output "L" Level Voltage	V_{OL}	8pin = open, $I_O = 0.5\text{A}$	-	0.8	1.5	V
Output "H" Level Voltage	V_{OH}	8pin = open, $I_O = 0.5\text{A}$	10	10.5	-	mA
Output Leakage Current	I_{OL}	4,5,6pin = "L" Level, $R_L = \infty$, Inflow Current into 9pin	-	-	1	V
2 Pin Output Offset Voltage	ΔV_2	$V_R = 6.0\text{V}$, 8 Pin base, $I_{O(2)} = 0.5\text{A}$	-0.5	-	0.5	V
3 Pin Output Offset Voltage	ΔV_3	$V_R = 6.0\text{V}$, 8 Pin base, $I_{O(3)} = 0.5\text{A}$	-0.5	-	0.5	V
10 Pin Output Offset Voltage	ΔV_{10}	$V_R = 6.0\text{V}$, 8 Pin base, $I_{O(10)} = 0.5\text{A}$	-0.5	-	0.5	V
8 pin Inflow Current 1	$I_{8(2)}$	2 Pin = "H", $I_{O(2)} = 0.5\text{A}$, $V_R = 6.0\text{V}$	0.2	0.6	1.5	mA
8 pin Inflow Current 2	$I_{8(3)}$	3 Pin = "H", $I_{O(3)} = 0.5\text{A}$, $V_R = 6.0\text{V}$	0.2	0.6	1.5	mA
8 pin Inflow Current 3	$I_{8(10)}$	10 Pin = "H", $I_{O(10)} = 0.5\text{A}$, $V_R = 6.0\text{V}$	0.2	0.6	1.5	mA
Back Rush Current	I_B	4,5,6pin = "L", Inflow Current into 9 Pin with one output terminal of -1V	-	-	0.3	A

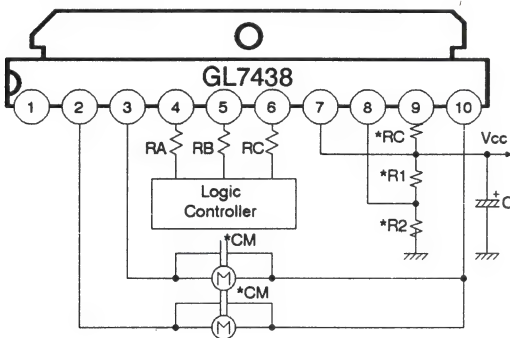
Input/Output Logic Table

4P IN 1	5P IN 2	6P IN 3	10P OUT1	2P OUT2	3P OUT3	REMARKS
L	L	- *	L	L	L	Brake
H	L	L	H	L	OPEN	Current flows from OUT 1 into OUT 2
H	L	H	L	H	OPEN	Current flows form OUT 2 into OUT 1
L	H	L	H	OPEN	L	Current flows form OUT 1 into OUT 3
L	H	H	L	OPEN	H	Current flows form OUT 3 into OUT 1
H	H	- *	L	L	L	Brake (Not used)

Test Circuit



Application Circuit



CM : capacitor to protect parasitic oscillation

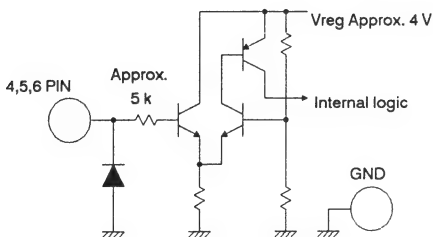
RC : current limiting resistor at output short circuit to reduce collector dissipation

R1, R2 : resistor to set up output voltage,

$$V_{OH} = V_{CC} \times \frac{R2}{R1 + R2}$$

Precautions when Using

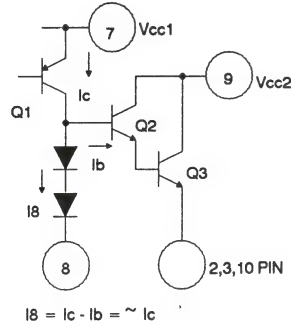
1. Inputting control Signals



The input circuit configuration is illustrated above. The inlet logic level is V_{IL} (0 to 1 V) and V_{IH} (3.5 to 5 V). If the input voltage "H" is 5 volts or more, an unnecessary current will flow in the IC. This is important to remember.

2. Output Voltage Control

The output terminal and Pin 8 circuit configuration is illustrated below.



The current at Pin 8 is obtained by subtracting the base current, I_B from current I_C determined inside the IC. When $I_C > I_B$, however, a nearly constant current flows. The maximum output voltage is available, when Pin 8 is open. It may be expressed as follows:

$$V_{Omax} = V_{CC1} - V_{SAT}(Q1) - V_F(Q2) - V_F(Q3)$$

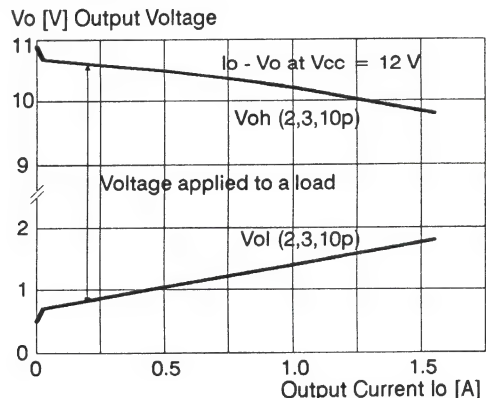
Since V_{Omax} does not exceed V_{CC1} , the inter-motor voltage cannot be effectively raised, when the collector power dissipation only is increased even if V_{CC2} is raised above V_{CC1} .

3. Brake

when the brake is applied, all outputs are at the "L" level. Therefore, the motor not driving may be affected instantaneously. Care should be taken when actually mounting.

4. Package Power

The relation between the output current, I_O , and the output voltage, V_O , is illustrated below.

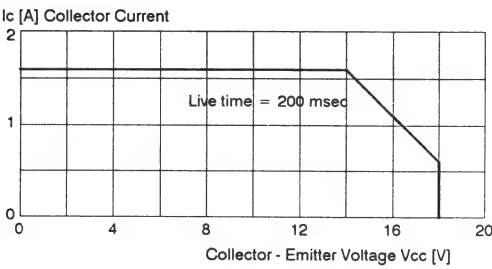


The IC power dissipation, P_d , may be obtained from the following expression:

$$P_d = V_{CC} \times I_{CC} + I_O \times \{ (V_{CC} - V_{OH}) + V_{OL} \}$$

Refer to the power reduction curve and design the heat radiation to allow for P_d .

5. ASO Curve



6. Recommended Operating Conditions

- Power supply voltage : 8 to 18 V
- Instantaneous current : See the ASO Curve above.
- Steady-state current : - 0.5 A (Note the P_d)

7. Thermal Protection

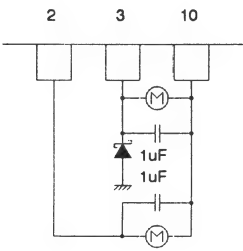
After the thermal protection circuit has functioned, all outputs will be at the "L" level whatever the inputs. When the thermal protection is released, the GL7438 returns to the circuit operation corresponding to the inputs. The thermal protection function operates at an IC chip temperature of 150°C (min. 125°C) and is released at 100°C (max. 125°C). A temperature difference of at least 10°C is required for operation and resetting.

8. Miscellaneous

If Pin 3 (output terminal) turns negative, the input terminal will be affected. This is problematical in operation. To prevent the problem, two countermeasures are shown below.

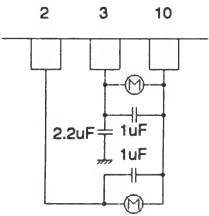
Action a:

A schottky diode is connected between Pin 3 and GND.



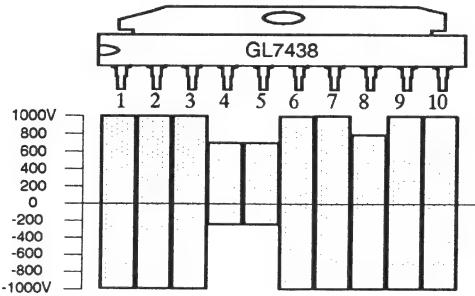
Action b:

A capacitor is connected between Pin 3 and GND.

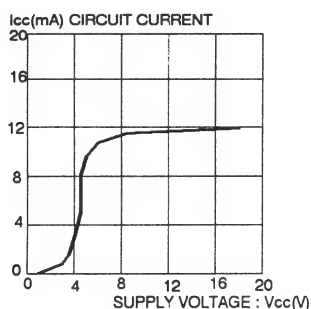
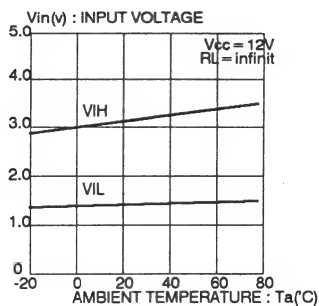
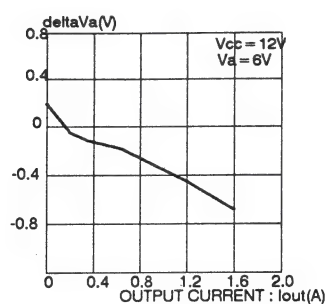
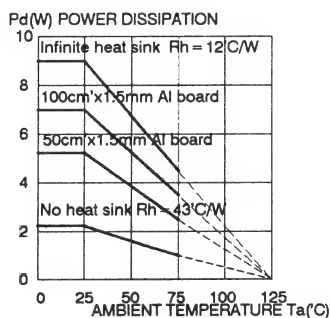
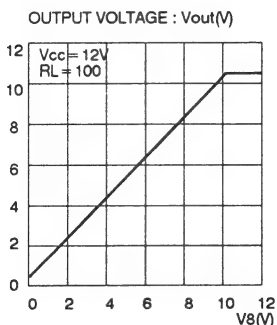
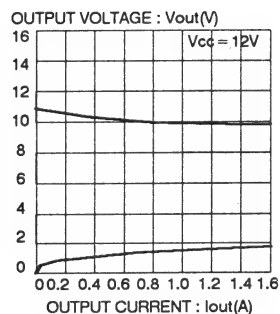
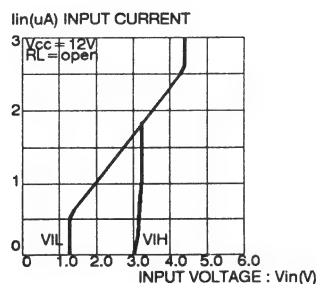
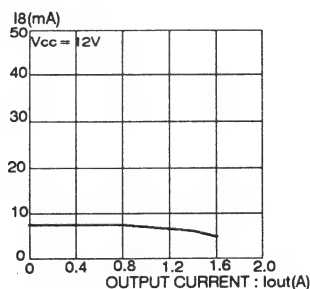


9. Electrostatic Discharge Characteristics

(when C = 200 pF)



Electrical Characteristic Curves

 $I_{CC} - V_{CC}$  $V_{IN} - T_A$  $\Delta V_8 - I_{OUT}$  $P_D - T_A$  $V_{OUT} - V_8$  $V_{OUT} - I_{OUT}$  $I_{IN} - V_{IN}$  $I_8 - I_{OUT}$ 

GL7445

BIDIRECTIONAL MOTOR DRIVER

Description

The GL7445 is a bidirectional motor driver IC. Since it has a 2 input logic circuit and performs the functions of bidirectional driving and braking, it is capable of direct driving 6V, 9V, 12V motors. The output voltage can be varied by using an external zener diode.

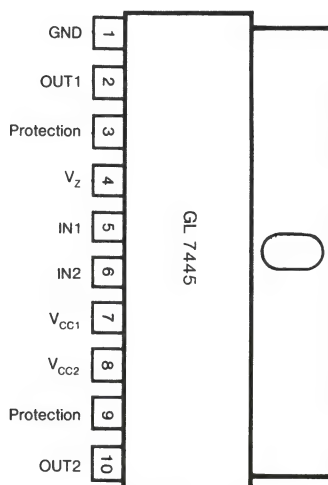
Features

- Built-in Braking Function
- Built-in Element to Absorb Dash Current of Motor
- Input Connectable Direct to MOS LSI
- Output Voltage Variable by Use of External Zener Diode.

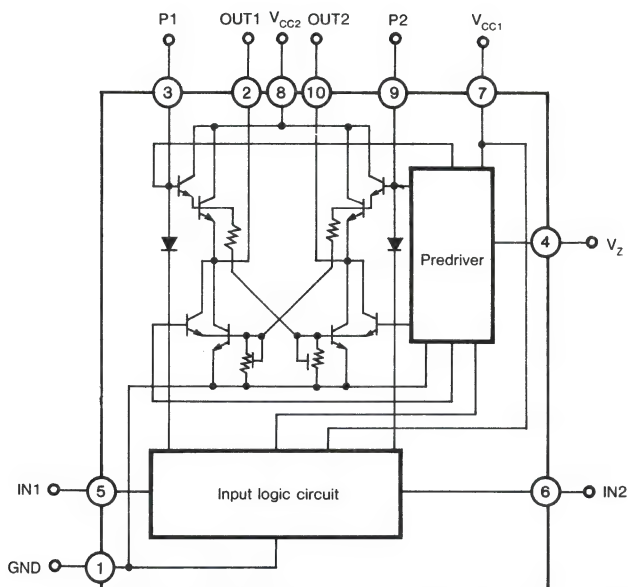
Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage	$V_{CC\text{ max}}$	18	V
Input Voltage	V_{IN}	$-0.3 \sim V_{CC}$	V
Output Current	$I_{out(peak)}$	± 1.6	A
Power Dissipation	P_D	2.2	W
Operating Temperature	T_{OPR}	$-25 \sim 75$	$^\circ\text{C}$
Storage Temperature	T_{STG}	$-55 \sim 125$	$^\circ\text{C}$

Pin Configuration



Block Diagram



Electrical Characteristics: $T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Threshold Voltage	V_{TH}	$R_L = \infty$	1.1	1.3	1.5	V
Input-On Current	I_{IN}	$R_L = \infty$	—	10	15	μA
Output Voltage	V_O	$R_L = 60\Omega$ $V_Z = 7.4\text{V}$	6.6	7.2	7.4	V
Output Leakage Current	I_{OL}	Pin 5,6: GND $R_L = \infty$	—	0.01	1.0	mA
Quiescent Current	I_{CC}	Pin5,6: GND $R_L = \infty$	3	6	10	mA
Saturation Voltage 1 _(UPP)	V_{SU1}	$I_{OUT} = 300\text{mA}$	—	1.9	2.3	V
Saturation Voltage 2 _(UPP)	V_{SU2}	$I_{OUT} = 500\text{mA}$	—	1.9	2.3	V
Saturation Voltage 1 _(LOW)	V_{SL1}	$I_{OUT} = 300\text{mA}$	—	0.25	0.5	V
Saturation Voltage 2 _(LOW)	V_{SL2}	$I_{OUT} = 500\text{mA}$	—	0.4	0.65	V

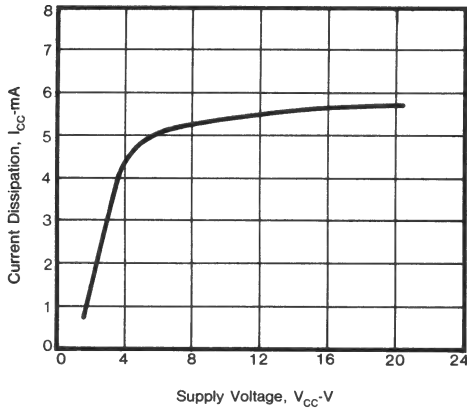
Logic Table

Input		Output		Function
IN1	IN2	OUT1	OUT2	
0	0	0	0	Braking
1	0	1	0	Forward (reverse) drive
0	1	0	1	Reverse (forward) drive
1	1	0	0	Braking

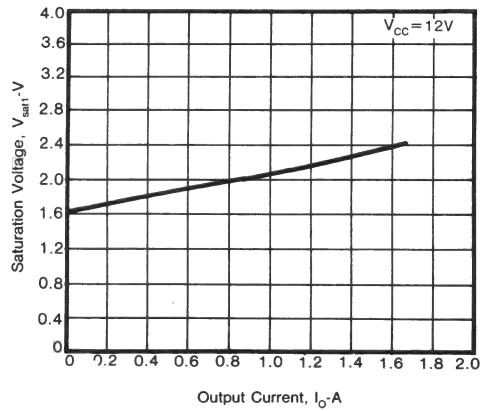
Input level
1: 2.0V or more
0: 0.7V or less

Typical Performance Curves

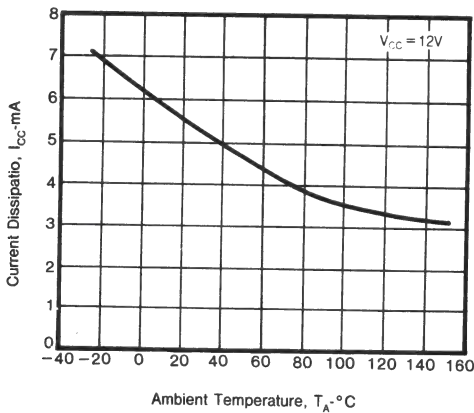
$I_{CC} - V_{CC}$



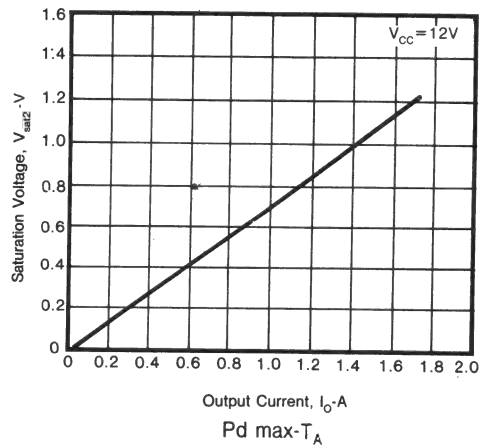
$V_{sat1} - I_O$



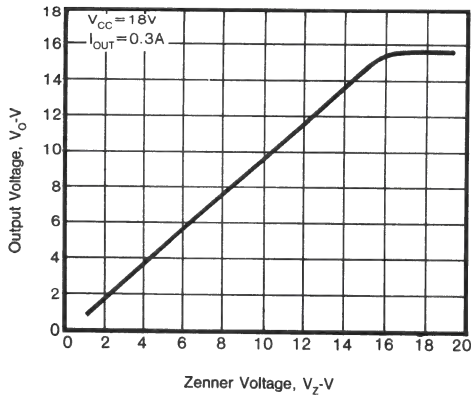
$I_{CC} - T_A$



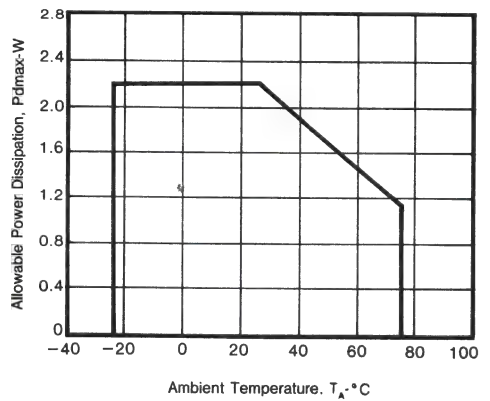
$V_{sat2} - I_O$



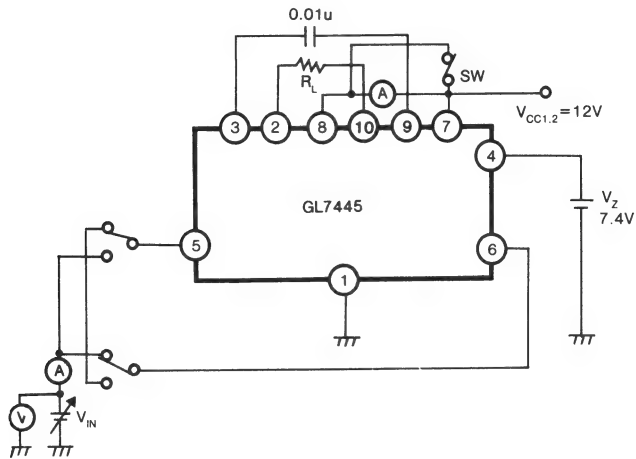
$V_O - V_Z$



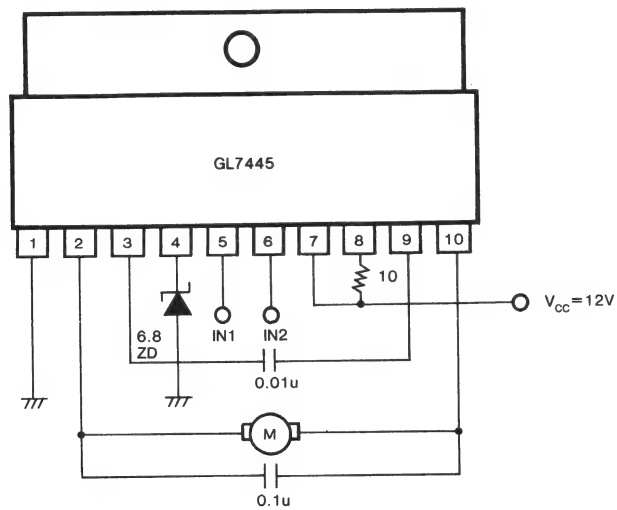
$P_d \text{ max} - T_A$



Test Circuit



Application Circuit



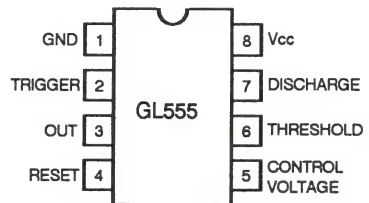
GL555

GENERAL PURPOSE BIPOLAR SINGLE TIMER

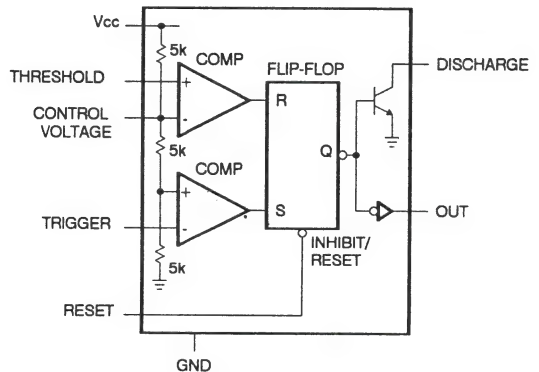
Description

The GL555 Timing Circuit is a very stable controller for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied ending the time-out. The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

Pin Configuration



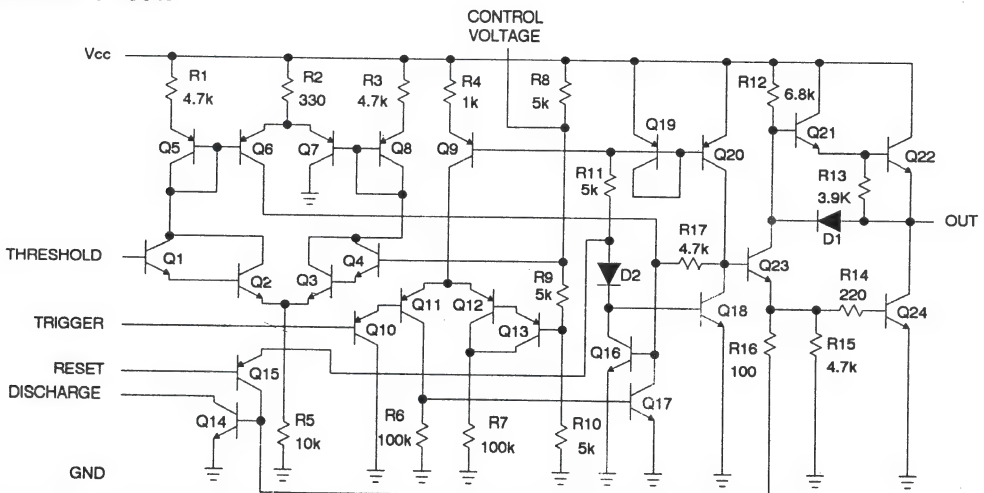
Block Diagram



Feature

- Timing Control, μs to Hours.
- Astable or Monostable Operating Modes
- Adjustable Duty cycle
- 200 mA Sink or Source Output Current
- TTL Output Drive Capability
- Temperature Stability of 0.005% / $^{\circ}\text{C}$ Typ
- Normally On or Normally Off Output
- Direct Replacement For SE555/NE555

Equivalent Circuit



Absolute Maximum Ratings

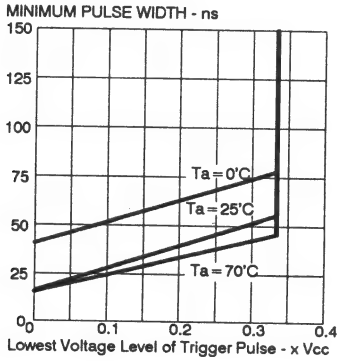
Supply Voltage	V_{CC}	+18	V
Power Dissipation	P_D	0.9	W
Storage Temperature Range	T_{STG}	-65 to +150	°C
Operating Temperature Range	T_{OPR}	0 to 70	°C

Electrical Characteristics : $T_A = 25^\circ\text{C}$, $V^+ = +5.0\text{ V to } +15\text{ V}$ (unless otherwise specified)

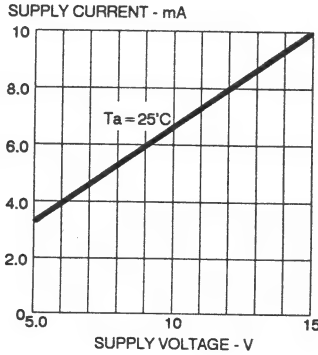
CHARACTERISTIC		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}		4.5		16	V
Supply Current		I_{CC}	$V_{CC} = 5\text{ V}, R_L = \infty$		3.0	6.0	mA
			$V_{CC} = 15\text{ V}, R_L = \infty, \text{LOW State}$		10	15	
Timing Error	Initial Accuracy	t_D	$R1 = 2.0\text{ k}\Omega \text{ to } 100\text{ k}\Omega$ $C = 0.1\text{ }\mu\text{F}$		1.0		%
	Drift With Temperature				50		ppm / °C
	Drift With Supply Voltage				0.1	0.5	% / V
Threshold Voltage		V_{TH}	$V_{CC} = 5.0\text{ V}$	2.6	3.33	4.0	V
			$V_{CC} = 15\text{ V}$	9.0	10	11	
Trigger Voltage		V_{TR}	$V_{CC} = 15\text{ V}$	4.0	5.0	6.0	V
			$V_{CC} = 5.0\text{ V}$	1.1	1.67	2.2	
Trigger Current		I_{TR}			0.5	20	μA
Reset Voltage		V_R		0.4	0.7	1.0	V
Reset Current		I_R			0.1	0.4	mA
Threshold Current		I_{TH}			30	250	nA
Control Voltage Level		V_{CV}	$V_{CC} = 15\text{ V}$	9.0	10	11	V
			$V_{CC} = 5.0\text{ V}$	2.6	3.33	4.0	
Output Voltage LOW		V_{OL}	$V_{CC} = 15\text{ V}, I_O^- = 10\text{ mA}$		0.1	0.25	V
			$I_O^- = 50\text{ mA}, V_{CC} = 15\text{ V}$		0.4	0.75	
			$I_O^- = 100\text{ mA}, V_{CC} = 15\text{ V}$		2.0	2.5	
			$I_O^- = 200\text{ mA}, V_{CC} = 15\text{ V}$		2.5	3.5	
			$V_{CC} = 5.0\text{ V}, I_O^- = 8.0\text{ mA}$		0.3		
			$I_O^- = 5.0\text{ mA}, V_{CC} = 5.0\text{ V}$		0.25	0.35	
Output Voltage HIGH		V_{OH}	$I_O^+ = 200\text{ mA}, V_{CC} = 15\text{ V}$	11.0	12.5		V
			$I_O^+ = 100\text{ mA}, V_{CC} = 15\text{ V}$	12.75	13.3		
			$V_{CC} = 5.0\text{ V}, I_O^+ = 100\text{ mA}$	2.75	3.3		
Rise Time of Output		t_r			100		ns
Fall Time of Output		t_f			100		ns
Discharge Leakage Current		I_{DIS}			20	100	nA

Typical Performance Curves

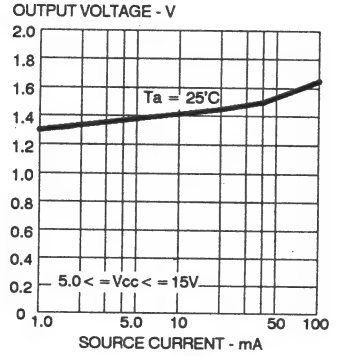
Minimum Pulse Width Required for Triggering



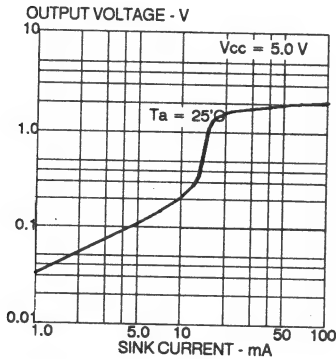
Total Supply Current vs Supply Voltage



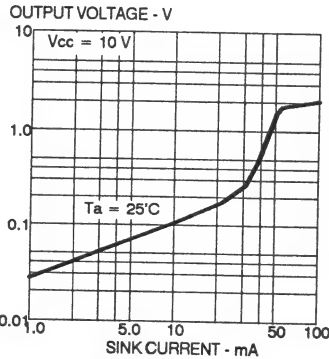
Output Voltage HIGH vs Output Source Current



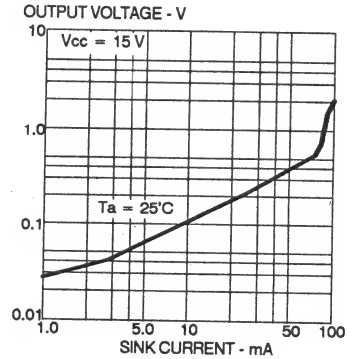
Output Voltage LOW vs Output Sink Current



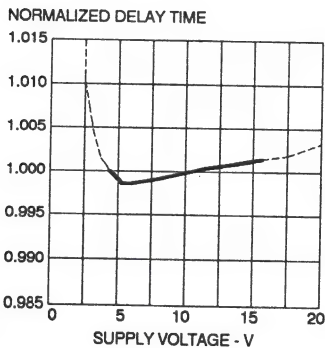
Output Voltage LOW vs Output Sink current



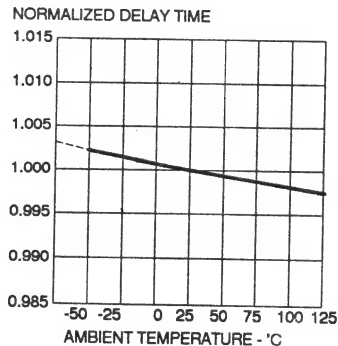
Output Voltage LOW vs Output Sink Current



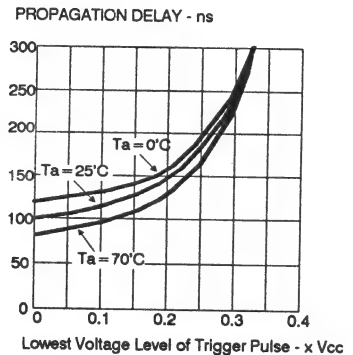
Delay Time vs Supply Voltage



Delay Time vs Ambient Temperature



Propagation Delay vs Voltage Level of Trigger Pulse



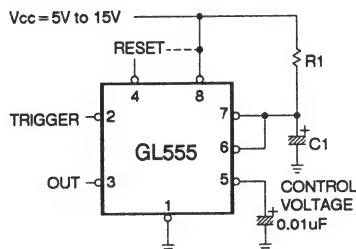
Typical Applications

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one shot. Referring to Figure 1 the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R_1 C_1$. When the voltage across the capacitor equals $\frac{2}{3} V_{CC}$, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 2 shows the actual waveforms generated in this mode of operation.

Figure 1 Monostable Mode



The circuit triggers on a negative going input signal when the level reaches $\frac{1}{3} V_{CC}$. Once triggered, the circuit remains in this state until the set time elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1 R_1 C_1$ and is easily determined by Figure 3. Notice that since the charge rate and the threshold level of the Comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the trigger terminal (lead 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the

reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied HIGH to avoid any possibility of false triggering.

Figure 2 Monostable Waveform

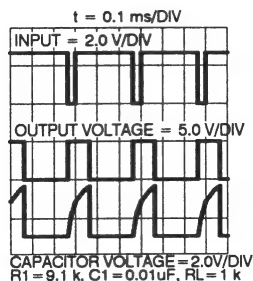
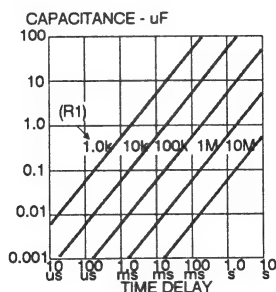


Figure 3 Time Delay vs R_1 and C_1



ASTABLE OPERATION

when the circuit is connected as shown in Figure 4 (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C_1 charges and discharges between $\frac{1}{3} V_{CC}$ and $\frac{2}{3} V_{CC}$. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage. Figure 5 shows actual waveforms generated in this mode of operation. the charge time (output HIGH) is given by:

$$t_1 = 0.693 (R_1 + R_2) C_1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693 (R_2) C_1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693 (R_1 + 2R_2) C_1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2) C_1}$$

and may be easily found by Figure 6.

The duty cycle is given by:

$$DC = \frac{R_2}{R_1 + 2R_2}$$

Figure 4 Astable Mode

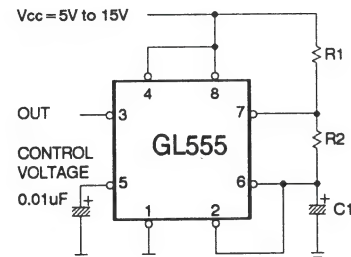


Figure 5 Astable Waveform

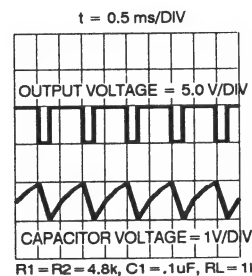
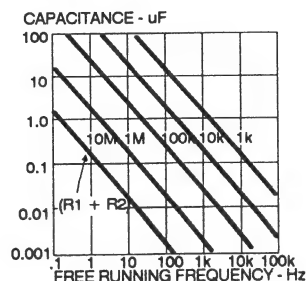


Figure 6 Free Running Frequency vs R_1, R_2 , and C_1



GLC555/556

CMOS GENERAL PURPOSE TIMER

Description

The GLC555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, TRIGGER and RESET currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the GLC555/6 are stable controllers capable of producing accurate time delays or frequencies. The GLC556 is a dual GLC555, with the two timers operating independently of each other, sharing only V* and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and capacitor.

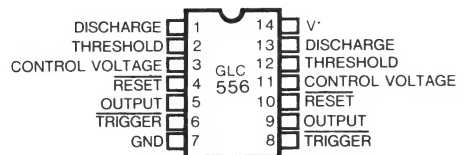
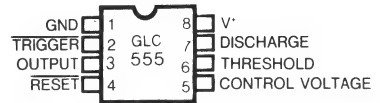
Features

- Exact equivalent in most cases for SE/NE555/556
- Low Supply Current – 80µA/160µA Typ (GLC555/556)
- Extremely low trigger, threshold and reset currents – 20pA Typ.
- High speed operation – 500 kHz guaranteed
- Wide operation supply voltage range – 2 to 18 volts
- Can be used with higher impedance timing elements than regular 555/6 for longer RC time constants.
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS
- Typical temperature stability of 0.005% per °C at 25°C
- Output have very low offsets, HI and LO

Application

- Precision Timing
- Pulse Width Modulation
- Pulse Generation
- Pulse Position Modulation
- Sequential Timing
- Missing Pulse Detector
- Time Delay Generation

Pin Configuration



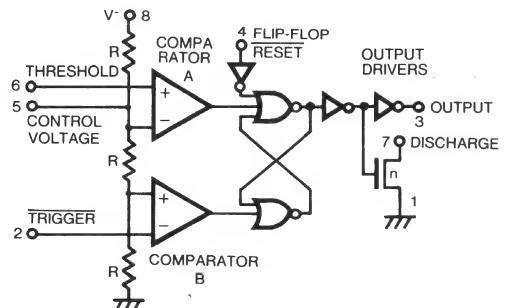
Truth Table

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	RESET	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
$>2/3(V^*)$	$>1/3(V^*)$	HIGH	LOW	ON
$V_{TH} < 2/3$	$1/3 < V_{TR}$	HIGH	STABLE	STABLE
DON'T CARE	$<1/3(V^*)$	HIGH	HIGH	OFF

NOTE: RESET will dominate all other inputs.

TRIGGER will dominate over THRESHOLD.

Block Diagram



This block diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs.

R=100kΩ, ±20% typ.

Absolute Maximum Ratings (Note 1)

Supply Voltage	V_{CC}	+18 Volts
Input Voltage (Trigger, Threshold, $\overline{\text{Reset}}$)	$\leq V^* + 0.3V$ to $\geq V^* - 0.3V$	
Output Current	I_O	100mA
Power Dissipation (GLC555/556 ²)	P_D	200/300 mW
Operating Temperature ²	T_{OPR}	-20° to +85°C
Storage Temperature	T_{STG}	-65° to +150°C
Lead Temperature (60 Seconds):	T_{SOLDER}	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

Operating Characteristics ($T_A = 25^\circ\text{C}$, $V^* = +2$ to $+15$ Volts unless other specified)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
V*	Supply Voltage	-20°C≤T _A ≤+70°C	2		18	V
I*	Supply Current (NOTE 3)	GLC555 V* = 2V V* = 18V		60 120	200 300	μA μA
		GLC556 V* = 2V V* = 18V		120 240	400 600	μA μA
Timing Error		R _A , R _B = 1k to 100K, 5V≤V*≤15V, C = 0.1μF				
Initial Accuracy		Note 4		2.0	5.0	%
Drift with Temperature		Note 4 V* = 5V V* = 10V V* = 15V		50	200 300 600	ppm/°C
Drift with Supply Voltage		V* = 5V		1.0	3.0	%/V
V _{TH}	Threshold Voltage	V* = 5V	0.65	0.67	0.69	V*
V _{TRIG}	Trigger Voltage	V* = 5V	0.31	0.33	0.35	V*
I _{TRIG}	Trigger Current	V* = 18V V* = 5V V* = 2V		50 10 1		pA pA pA
I _{TH}	Threshold Current	V* = 18V V* = 5V V* = 2V		50 10 1		pA pA pA
I _{RST}	Reset Current	V _{RESET} = Ground V* = 18V V* = 5V V* = 2V		100 20 2		pA pA pA
V _{RST}	Reset Voltage	V* = 18V	0.4	0.7	1.0	V
		V* = 2V	0.4	0.7	1.0	V
V _{CV}	Control Voltage Lead		0.65	0.67	0.69	V*
V _O	Output Voltage Drop	Output Lo V* = 15V I _{SINK} = 20 mA V* = 5V I _{SINK} = 3.2mA		0.4 0.2	1.0 0.4	V V
		Output Hi V* = 15V I _{SOURCE} = 0.8mA V* = 5V I _{SOURCE} = 0.8mA	14.3 4.0	14.6 4.3		V
t _r	Rise Time of Output	R _L = 10MΩ C _L = 10pF V* = 5V	35	40	75	ns
t _f	Fall Time of Output	R _L = 10MΩ C _L = 10pF V* = 5V	35	40	75	ns
f _{max}	Guaranteed Max Osc Freq	Astable Operation	500			kHz

NOTE:

- Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than $V^* + 0.3V$ or less than $V^* - 0.3V$ may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the GLC555/6 must be turned on first.
- Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C . Below 125°C power dissipation may be increased to 300mW at 25°C . Derating factor is approximately $3\text{mW}/^\circ\text{C}$ (GLC556) or $2\text{mW}/^\circ\text{C}$ (GLC555).
- The supply current value is essentially independent of the TRIGGER, THRESHOLD and RESET voltages.
- Parameter is not 100% tested. Majority of all units meet this specification.

Application Notes

GENERAL

The GLC555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the GLC555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The GLC555/6 devices produce no such transients. See Figure 2.

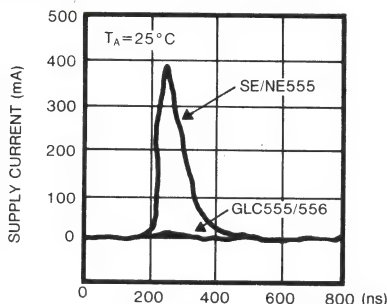


Figure 2. Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The GLC555/556 produces supply current spikes of only 2-3 mA instead of 300-400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using a GLC555 and 3 capacitors with a GLC555.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the GLC555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 3 and 4.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the GLC555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 3. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical.) Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

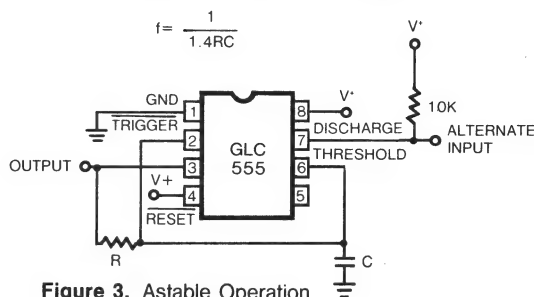


Figure 3. Astable Operation

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative TRIGGER pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_A C$. When the voltage across the capacitor equals $2/3 V^+$, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. TRIGGER must return to a high state before the OUTPUT can return to a low state.

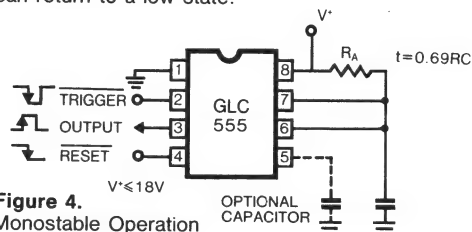


Figure 4. Monostable Operation

CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and TRIGGER internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

RESET

The RESET terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the RESET function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

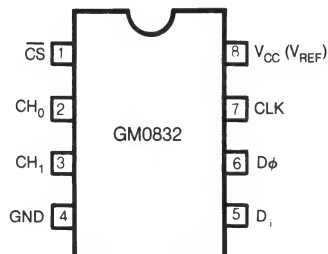
GM0832

8 BIT SERIAL I/O A/D CONVERTER WITH MULTIPLEXER OPTIONS

Description

The GM0832 is a successive approximation A/D converter with a serial I/O and configurable input multiplexers with upto 2 channels. The serial input/output is configured to interface with standard shift registers or microprocessor. The 2 channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment. The differential analog voltage input allows increasing the common mode rejection and offsetting the analog zero input voltage value. The voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the 8 bits of resolution.

Pin Configuration



Feature

- Easy Interface to All Microprocessors, or Operates "Stand-Alone"
- Operates Ratiometrically or with 5V Voltage Reference
- No Zero or Full-Scale Adjust Required
- 2 Channel Multiplexer Options with Address Logic
- 0V to 5V Input Range with Single 5V Power Supply
- Resolution: 8 Bits
- Total Unadjusted Error: ± 1 LSB.
- Single Supply: 5V
- Low Power: 15 mW
- Conversion Time: 32 μ s

Absolute Maximum Ratings

Supply Current	10	mA
Supply Voltage	6.5	V
Logic Input Voltage	-0.3 to 15	V
Analog Input Voltage	-0.3 to $V_{CC} + 0.3$	V
Power Dissipation	0.8	W
Operating Temperature Range	0 to 70	$^{\circ}$ C
Storage Temperature Range	-65 to 150	$^{\circ}$ C

Electrical Characteristics: $V_{CC}=5V$, $f_{CLK}=250\text{ KHz}$ (unless otherwise specified)

MARAMETER	CONDITIONS *1	MIN	TYP *2	MAX	UNIT
High-Level Output Voltage	$V_{CC}=4.75V$, $I_{OH} = -360\mu A$	2.4			V
	$V_{CC}=4.75V$, $I_{OH} = -10\mu A$	4.5			
Low-Level Output Voltage	$V_{CC}=4.75V$, $I_{OL} = 1.6\text{ mA}$			0.4	V
High-Level Input Current	$V_I = V_{CC}$		0.005	1	μA
Low-Level Input Current	$V_I = 0$	-1	-0.005		μA
High-Impedance Output Current (DO)	$V_O = 0.4V$, $T_A = 25^\circ C$		-0.1	-3	μA_{DC}
	$V_O = 5V$, $T_A = 25^\circ C$		0.1	3	
Source Current	$V_O = 0$, $T_A = 25^\circ C$		14		mA
Sink Current	$V_O = V_{CC}$, $T_A = 25^\circ C$		16		mA
Common-Mode Input Range (See Note 1)		-0.05 to $V_{CC} + 0.05$			V
On-Channel Leakage Current (See Note 5)	On Channel = 5V	$T_A = 0 \sim 70^\circ C$		-1	μA
	Off Channel = 0V	$T_A = 25^\circ C$		-200	nA
	On Channel = 0V	$T_A = 0 \sim 70^\circ C$	-1		μA
	Off Channel = 5V	$T_A = 25^\circ C$	-200		nA
Off-Channel Leakage Current (See Note 5)	On Channel = 5V	$T_A = 0 \sim 70^\circ C$	-1		μA
	Off Channel = 0V	$T_A = 25^\circ C$	-50		nA
	On Channel = 0V	$T_A = 0 \sim 70^\circ C$		1	μA
	Off Channel = 5V	$T_A = 25^\circ C$		50	nA
Input Resistance to Reference Ladder		1.9	2.4		k Ω
Input Capacitance (Logic Inputs)	$T_A = 25^\circ C$		5		pF
Output Capacitance	$T_A = 25^\circ C$		5		pF
Supply Current (See Note 2)*3			3	5.2	mA

*1 All parameters are measured under open-loop conditions with zero common-mode input voltage (unless otherwise specified).

*2 All typical values are at $T_A = 25^\circ C$

*3 Includes ladder current.

NOTES:

- For IN - more positive than IN +, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes the will conduct forward current for analog input voltages one diode drop below ground or one diode drop above V_{CC} . Care must be taken during testing at low V_{CC} levels (4.5V) because high-level analog input (5V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full-scale. As long as the analog input voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0-V to 5-V input voltage range requires a minimum V_{CC} of 4.950 volts for all variations of temperature and load.
- An internal zener diode is connected from the V_{CC} input to ground. The breakdown voltage of diode is approximately 7V. When the voltage regulator powers the converter, this diode ensures that the V_{CC} input is less than the zener breakdown votage (6.4V).

Operating Characteristics: $V_{CC}=5V$, $F_{CLK}=250\text{ KHz}$, $t_r=f_t=20\text{ns}$ (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply-Voltage Variation Error				$\pm 1/6$		LSB
Total Unadjusted Error (See Note 3)		Vref Forced to 5V			± 1	LSB
Common-Mode Error		Differential mode		$\pm 1/16$		LSB
Propagation Delay Time, Clock \rightarrow to Output Data (See Note 4)	MSB First	$C_L=100\text{ pF}$, $T_A=25^\circ\text{C}$		650	1000	ns
	LSB First			250	600	
Output Disable Time From $\overline{CS} \uparrow$		$C_L=10\text{ pF}$, $R_L=10\text{ k}\Omega$ $T_A=25^\circ\text{C}$		125	250	ns
Conversion Time		Not Including Multiplexer Addressing Time, $T_A=25^\circ\text{C}$			8	Clock Period
t_h ; Data input Valid after CLK Rising Edge				35	90	ns
t_{su} ; Data input Valid to CLK Edge				100	250	ns

NOTES:

- Total unadjusted error includes offset, full scale, linearity, and multiplexer errors.
- If the MSB from the comparator is used first in the successive-approximation loop, then an additional built-in delay will allow for comparator response time.
- Leakage current is measured with the clock not switching.

Parameter Measurement Data

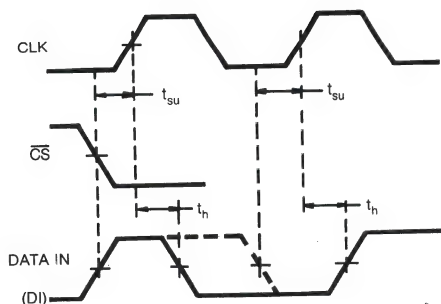


Figure 1. Data Input Timing

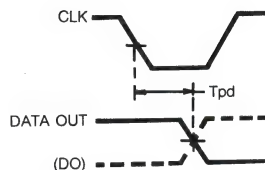


Figure 2. Data Output Timing

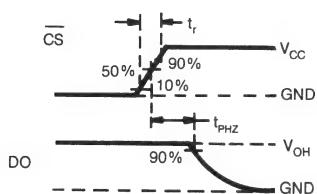


Figure 3. t_{PHZ} Voltage Waveforms

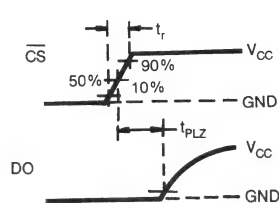


Figure 4. t_{PLZ} Voltage Waveforms

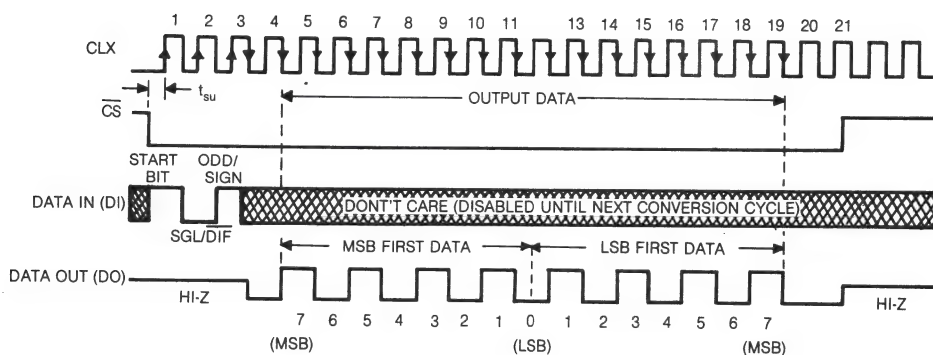
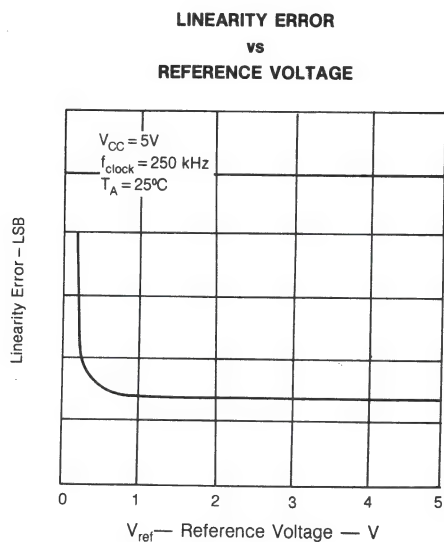
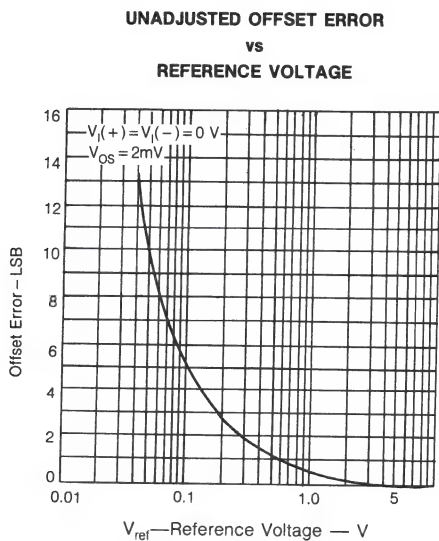
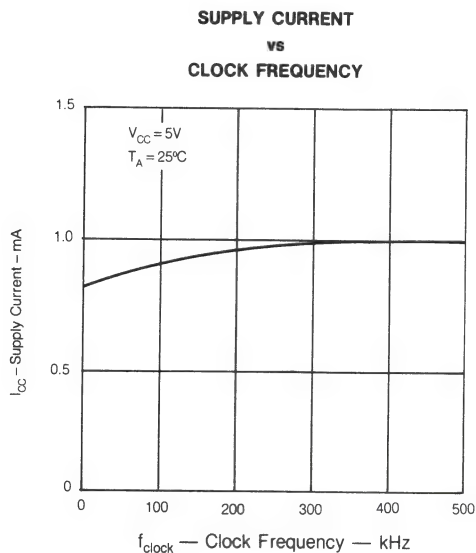


Figure 5 – GM0832 Timing Diagram





MUX Addressing (5-Bit Shift Register) (See Note)

Table 1. Single Ended Mux Mode

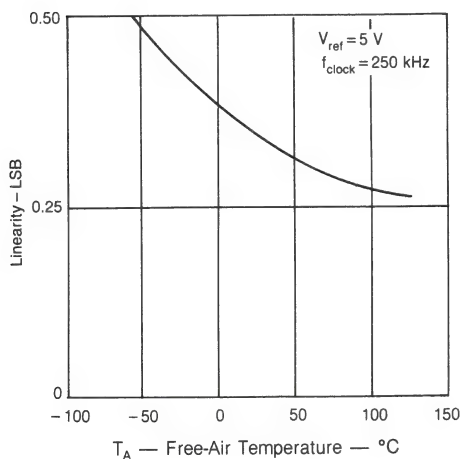
MUX ADDRESS		CHANNEL NO.	
SGL/ \overline{DTF}	ODD/SIGN	0	1
1	0	+	
1	1		+

Table 2. Differential Mux Mode

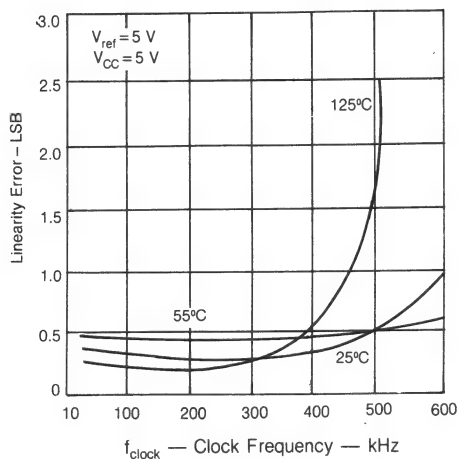
MUX ADDRESS		CHANNEL NO.	
SGL/ \overline{DTF}	ODD/SIGN	0	1
0	0	+	-
0	1	-	+

NOTE . Internally, Select 0 is low, Select 1 is high, COMMON is internally connected to ANLG GND.

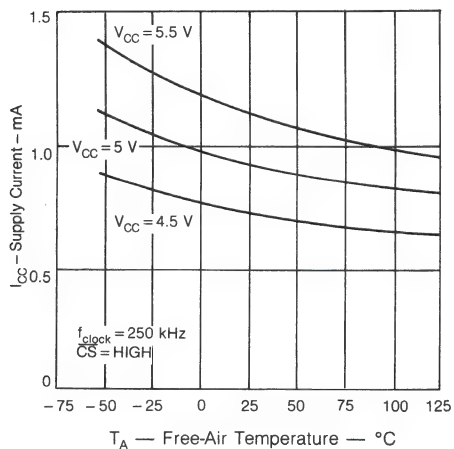
LINEARITY ERROR
vs
FREE-AIR TEMPERATURE



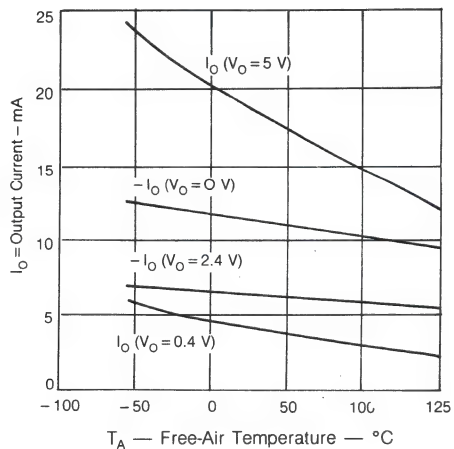
LINEARITY ERROR
vs
CLOCK FREQUENCY



SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE



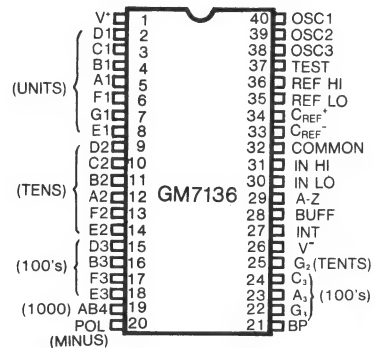
GM7136

3½-DIGIT LOW POWER A/D CONVERTER

Features

- First-reading recovery from overrange gives immediate "OHMS" measurement
- Guaranteed zero reading for 0V input
- True polarity at zero for precise null detection
- 1pA typical input current
- True differential input and reference
- Direct LCD display drive-no external components required
- Low noise—15μVp-p without hysteresis or overrange hangover
- On-chip clock and reference
- Low power dissipation, guaranteed less than 1 mW

Pin Configuration

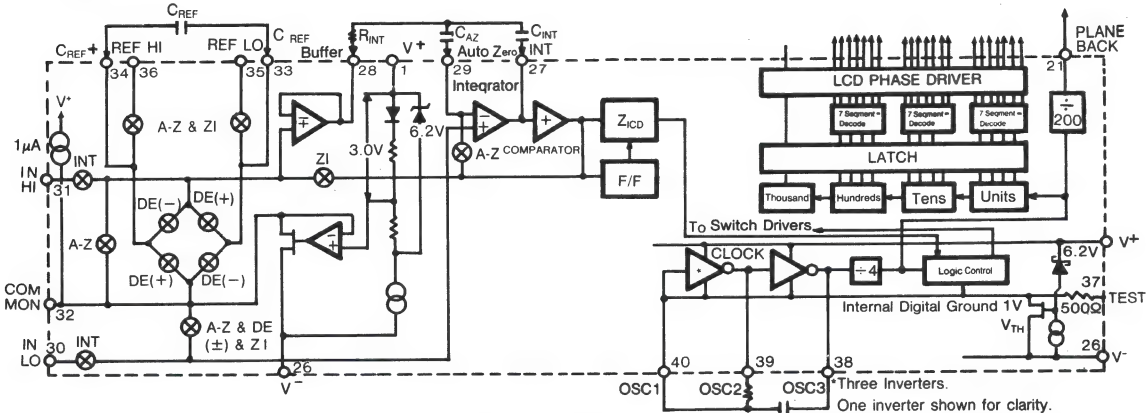


Description

The GM7136 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. GM7136 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is under 100μA, ideally suited for 9V battery operation.

The GM7136 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

Block Diagram



Absolute Maximum Ratings

Supply Voltage (V^+ to V^-)	15V
Analog Input Voltage (either input) (Note 1)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Clock Input	TEST to V^+

Power Dissipation (Note 2)

Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +160°C
Lead Temperature(soldering, 60 sec)	300°C

Note 1: Input voltages may exceed the supply voltage, provided the input current is limited to $\pm 100\mu\text{A}$.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	$V_{IN}=0.0\text{V}$ Full-Scale=200.0mV	-000.0	± 000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN}=V_{REF}$, $V_{REF}=100\text{mV}$	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN}=+V_{IN}\approx 200.0\text{mV}$	-1	± 0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale=200mV or Full-Scale=2.000V	-1	± 0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	$V_{CM}=\pm 1\text{V}$, $V_{IN}=0\text{V}$ Full-Scale=200.0mV		50		$\mu\text{V/V}$
Noise (Pk-Pk value not exceeded 95% of time)	$V_{IN}=0\text{V}$, Full-Scale=200.0mV		15		μV
Leakage Current @ Input	$V_{IN}=0\text{V}$		1	10	pA
Zero Reading Drift	$V_{IN}=0\text{V}$, $0^\circ\text{C}<T_A<+70^\circ\text{C}$		0.2	1	$\mu\text{V}/^\circ\text{C}$
Scale Factor Temperature Coefficient	$V_{IN}=199.0\text{mV}$, $0^\circ\text{C}<T_A<+70^\circ\text{C}$ (Ext. Ref. 0ppm/ $^\circ\text{C}$)		1	5	ppm/ $^\circ\text{C}$
Supply Current (Does not include COMMON current)	$V_{IN}=0\text{V}$ (Note 6)		70	100	μA
Analog COMMON Voltage (With respect to positive supply)	250k Ω between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250k Ω between Common and Positive Supply		150		ppm/ $^\circ\text{C}$
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- =9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- =9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at $T_A=25^\circ\text{C}$, $f_{\text{clock}}=16\text{kHz}$ and are tested in the circuit of Figure 1.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: 48kHz oscillator, Figure 2, increases current by 20 μA (typ).

Note 7: Extra capacitance of CERP package changes oscillator resistor value to 470k Ω or 150k Ω (1 reading/sec or 3 readings/sec).

Test Circuits

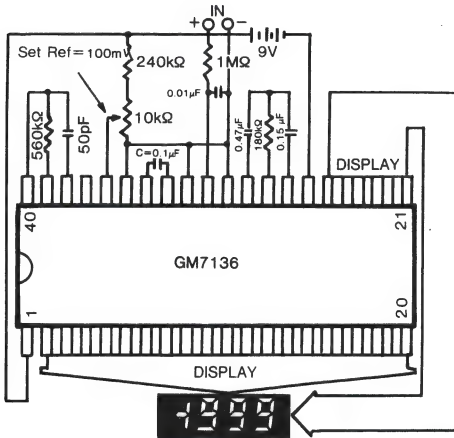


Fig. 1. Clock Frequency 16kHz (1 reading/sec)

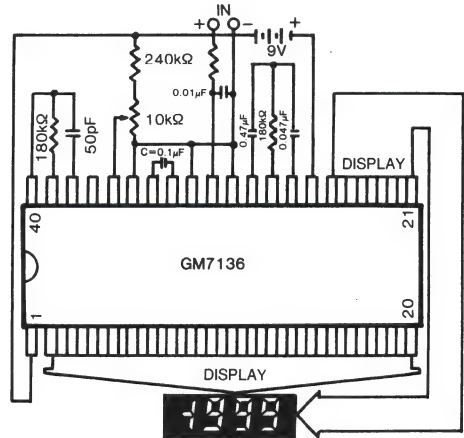


Fig. 2. Clock Frequency 48kHz (3 readings/sec)

Typical Applications

The GM7136 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

1. **Using the Internal Reference.** Values shown are for 200.0mV full-scale, 3 readings/sec, floating supply voltage (9V battery).

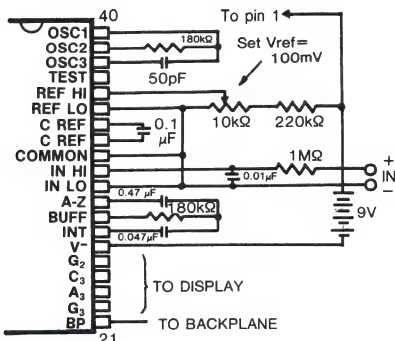


Fig. 3.

2. **External Band-Gap Reference (1.2V Type).** IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

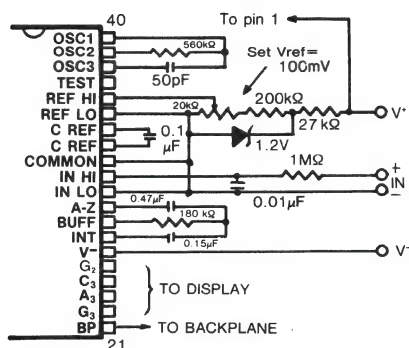


Fig. 4.

Typical Applications (Continued)

3. **Recommended Component Values for 2.000V Full-Scale, 3, Readings/Sec.** For 1 reading/sec, change C_{INT} , R_{OSC} to values of Fig. 5.

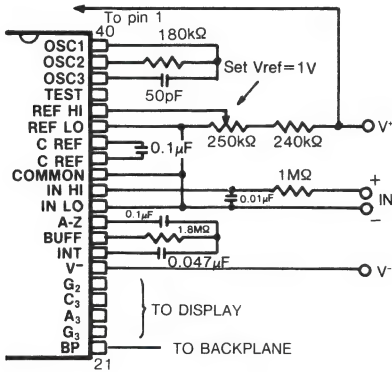


Fig. 5.

5. **Operated from Single +5V Supply.** An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

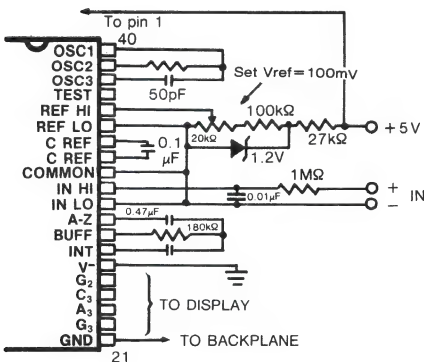


Fig. 7.

4. **Zener Diode Reference.** Since low TC zeners have breakdown voltages $-6.8V$, diode must be placed across the total supply (10V). As in the case of Fig. 6, IN LO may be tied to COMMON.

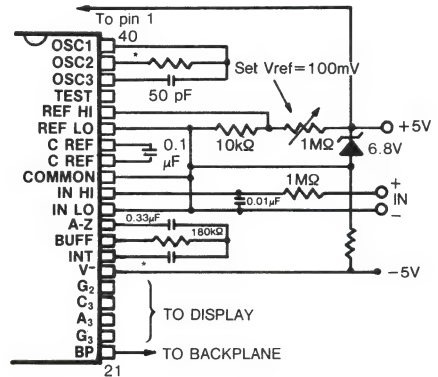
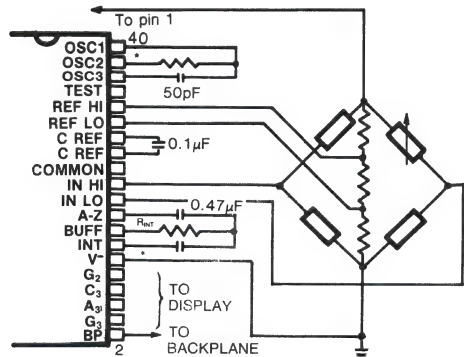


Fig. 6.

6. **Measuring Ratiometric Values of Quad Load Cell.** The resistor values within the bridge are determined by the desired sensitivity.



* Values depend on clock frequency. See figures 3,4,5.

Fig. 8.

7. **Digital Centigrade Thermometer.** A silicon diode-connected transistor has a temperature coefficient of about $-2\text{mV}/^\circ\text{C}$. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

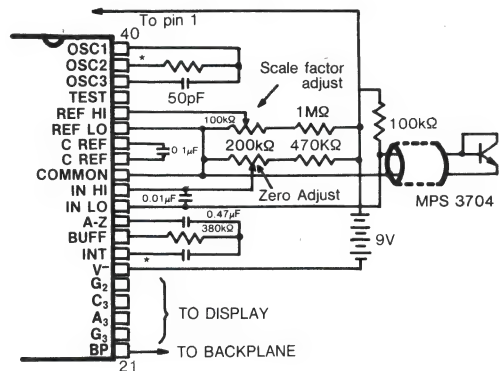


Fig. 9.

8. **Circuit for Developing Underrange and Overrange Signals from GM7136 Outputs.**

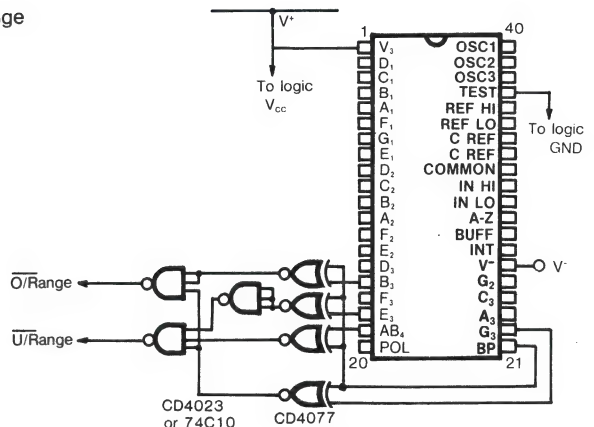


Fig. 10.

9. **AC to DC Converter with GM7136.** Test is used as a common-mode reference level to ensure compatibility with most op amps.

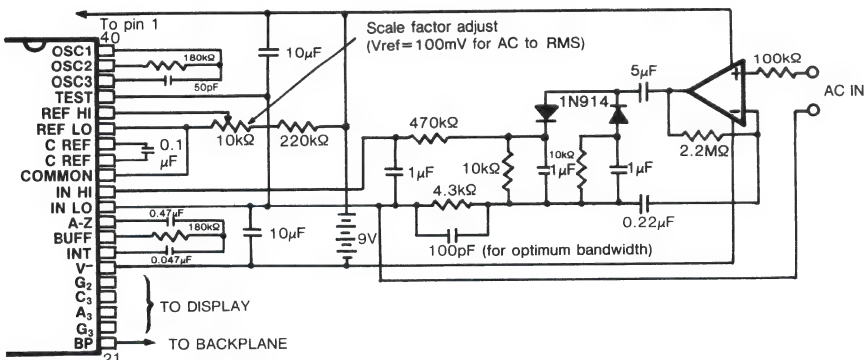


Fig. 11.

Detailed Description—Analog Section

CONVERSION CYCLE

Figure 12 shows the Block Diagram of the Analog Section for the GM7136. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

1. Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ} , to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10 μ V.

2. Singal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-Integrate Phase

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is 1000 (V_{IN}/V_{REF}).

4. Zero Integrator Phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "Heavy" overrange conversion, it is extended to 740 clock pulses.

5. Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

6. Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection).

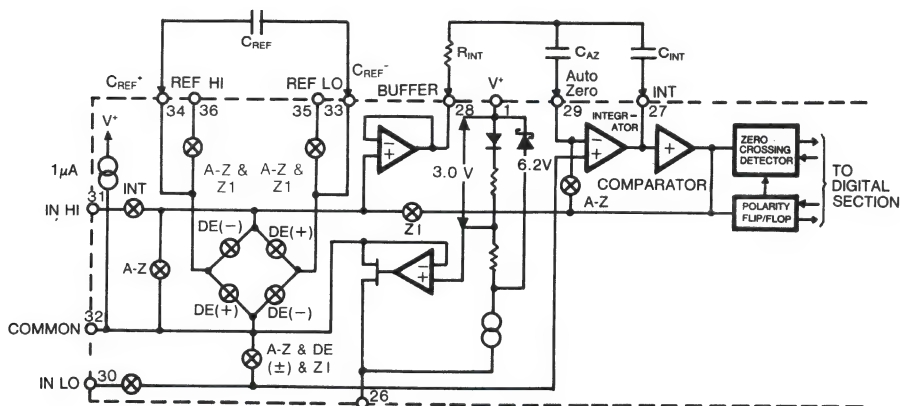


Fig. 12. Analog Section of GM7136

7. Analog Common

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate ($>7V$), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance ($\approx 35\Omega$), and a temperature coefficient typically less than 80ppm/ $^{\circ}C$.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of $2^{\circ}C$ to $8^{\circ}C$, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate ($<7V$). These problems are eliminated if an external reference is used, as shown in Figure 13.

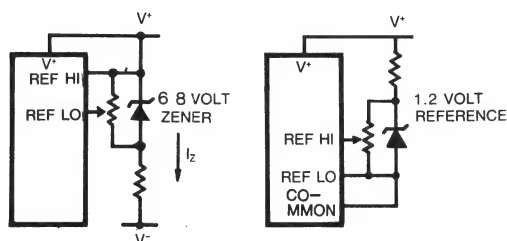


Fig. 13. Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink $100\mu A$ or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only $1\mu A$ of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

8. Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus, it can be used as the negative supply for external segment drivers such as for decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read 1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant DC

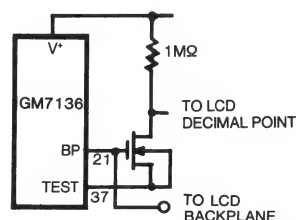


Fig. 14. Simple Inverter for Fixed Decimal Point

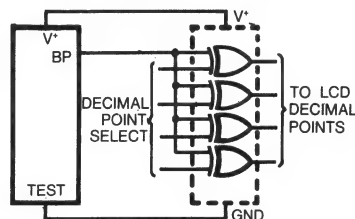


Fig. 15. Exclusive "OR" Gate for Decimal Point Drive

voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

Detailed Description—Digital Section

Figure 16 shows the digital section for the GM7136. An internal digital ground is generated from a 6V Zener diode and a large P channel source follower. This supply is made stiff to absorb the relatively large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

SYSTEM TIMING

Figure 17 shows the clock oscillator provided in the GM7136.

Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

* After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

Display Font

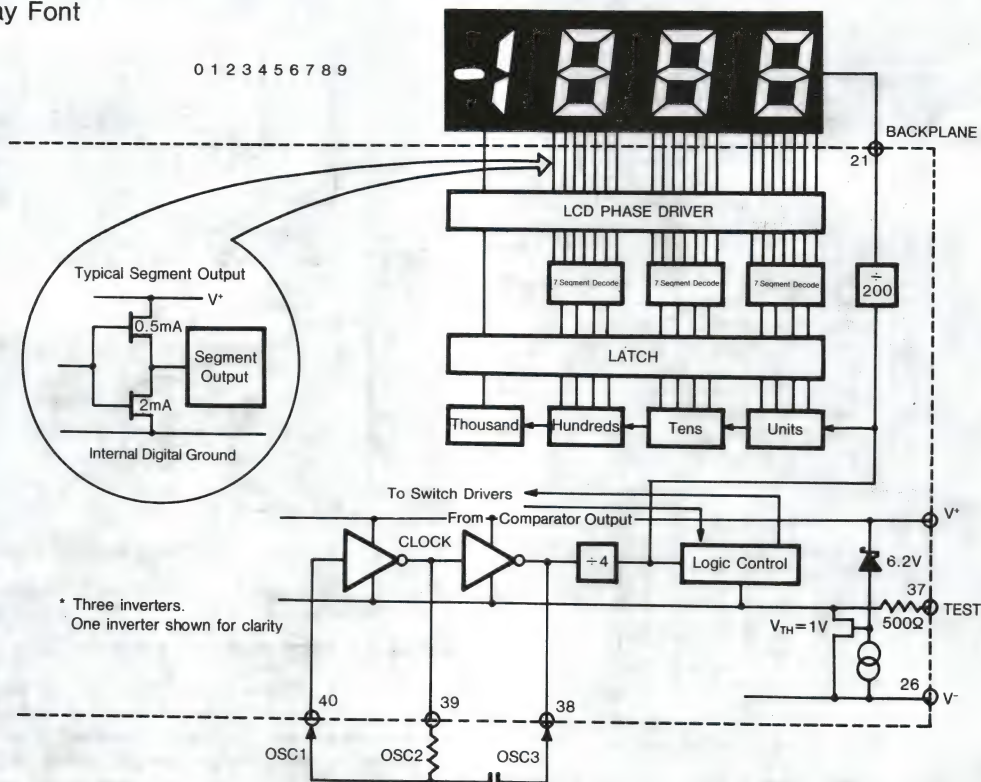


Figure 16. Digital Section

Component Value Selection

INTEGRATING CAPACITOR

Both the buffer amplifier and the integrator have a class A output stage with $6\mu\text{A}$ of quiescent current. They can supply $\sim 1\mu\text{A}$ of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, $1.8\text{M}\Omega$ is near optimum, and similarly $180\text{k}\Omega$ for a 200.0mV scale.

INTEGRATING CAPACITOR

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal $\pm 2\text{V}$ full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are $0.047\mu\text{F}$, for 1 reading/sec (16kHz) $0.15\mu\text{F}$. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing. The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

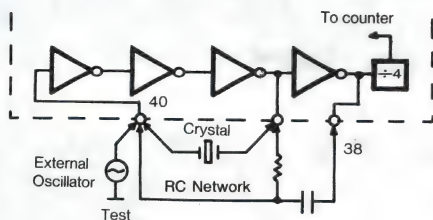


Figure 17. Clock Circuit

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 48kHz, 40kHz, $33\frac{1}{3}\text{kHz}$, etc. should be selected. For 50Hz rejection, oscillator frequencies of $66\frac{2}{3}\text{kHz}$, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

GL574

VOLTAGE STABILIZER FOR ELECTRONIC TUNER

Description

The GL574 is a monolithic integrated voltage stabilizer especially designed as voltage supplier for varactor diode.

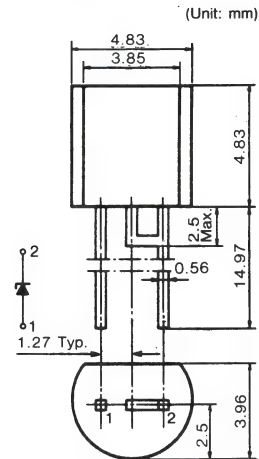
Features

- Low temperature coefficient
- Low dynamic resistance
- Typical reference voltage of 33V

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Zener Current	10	mA
Power Dissipation	200 ($T_A = 75^\circ\text{C}$)	mW
Operating Ambient Temperature Range	-20 to +75	$^\circ\text{C}$
Storage Temperature Range	-40 to +125	$^\circ\text{C}$

Package Dimensions

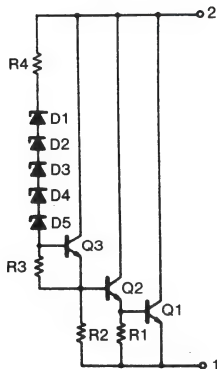


Pin Connection

1. Anode
2. Cathode

* All Values Indicate Maximum Values

Schematic Diagram



Electrical Characteristics ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Stabilized Voltage	V_Z	31		35	V	$I_Z = 5 \text{ mA}$
Stabilized Voltage Temperature Drift	$\Delta V_Z / \Delta T$	-1.0	0	1.0	mV/ $^\circ\text{C}$	$I_Z = 5 \text{ mA}$ $T_A = -20 \text{ to } +75^\circ\text{C}$
Dynamic Resistance	r_z		10	25	Ω	$I_Z = 5 \text{ mA}$ $f = 1 \text{ kHz}$ $I_{AC} = 0.5 \text{ mA}$

Typical Performance Curves

Figure 1 - Power Dissipation vs. Ambient Temperature

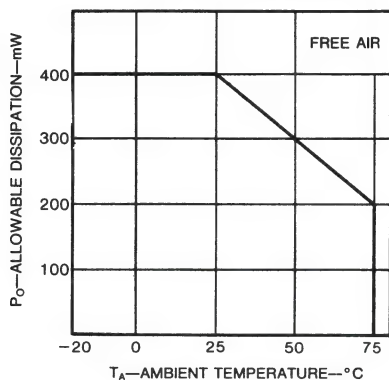


Figure 2 - Dynamic Resistance vs. Zener Current

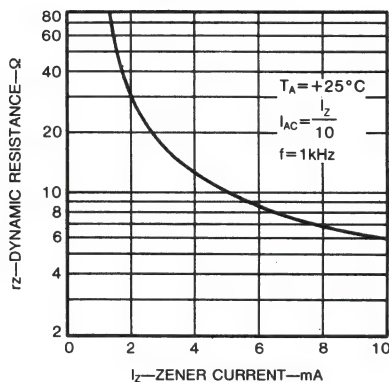


Figure 3 - Stabilized Voltage Temperature Drift vs. Zener Current

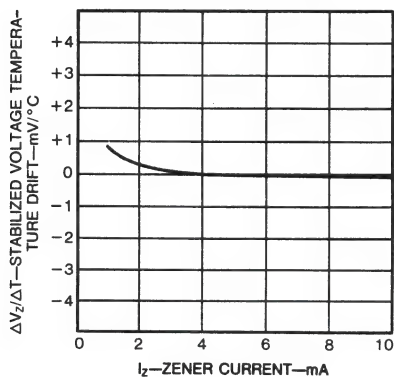


Figure 4 - Stabilized Voltage Variation vs. Time

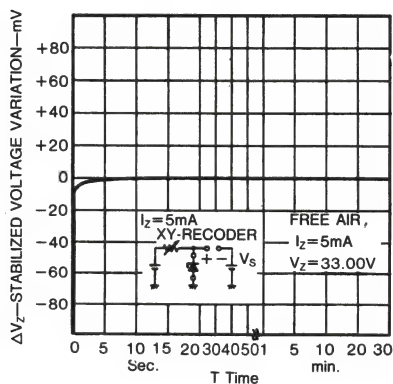
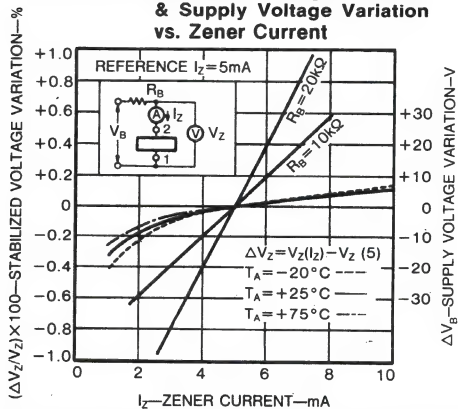
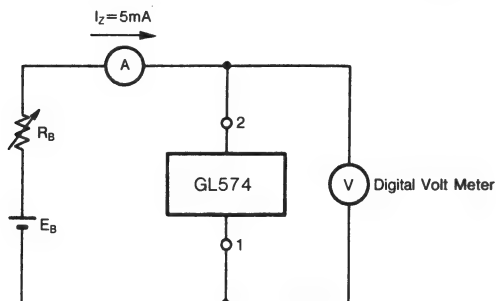


Figure 5 - Stabilized Voltage Variation & Supply Voltage Variation vs. Zener Current

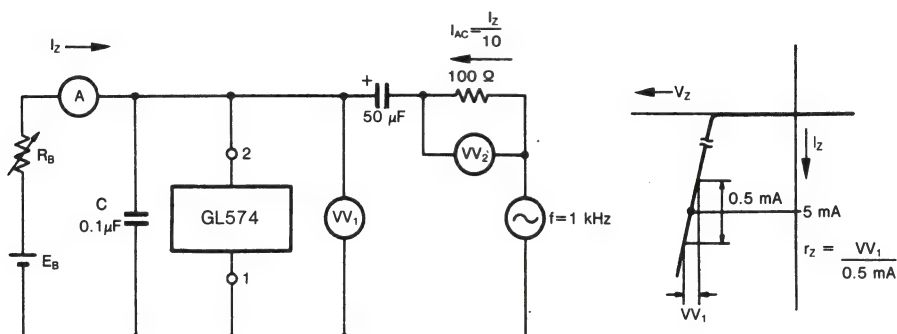


Measuring Circuits

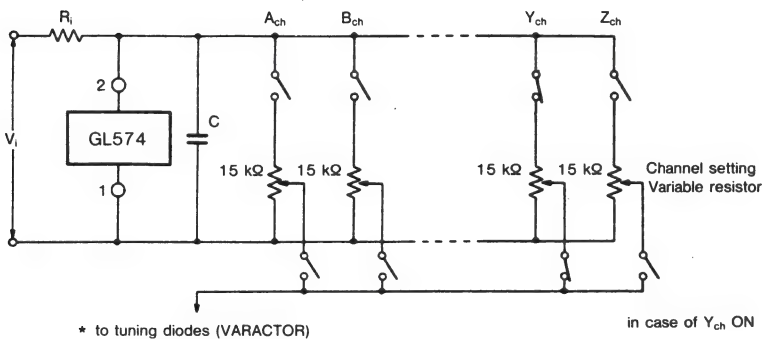
Measuring Circuit for Stabilized Voltage V_Z



Measuring Circuit for Dynamic Resistance r_z



Typical Application



GL7101

EARTH LEAKAGE CURRENT DETECTOR

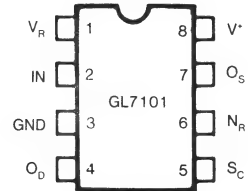
Description

The GL7101 is designed for use in earth leakage circuit interrupters for operation directly off the AC Line in breakers.

It contains pre regulator, main regulator, after regulator, differential amplifier, level comparator, latch circuit. The input in the differential amplifier is connect to the secondary node of zero current transformer.

The level comparator generates high level when earth leakage current is greater than some level.

Pin Configuration (Top View)



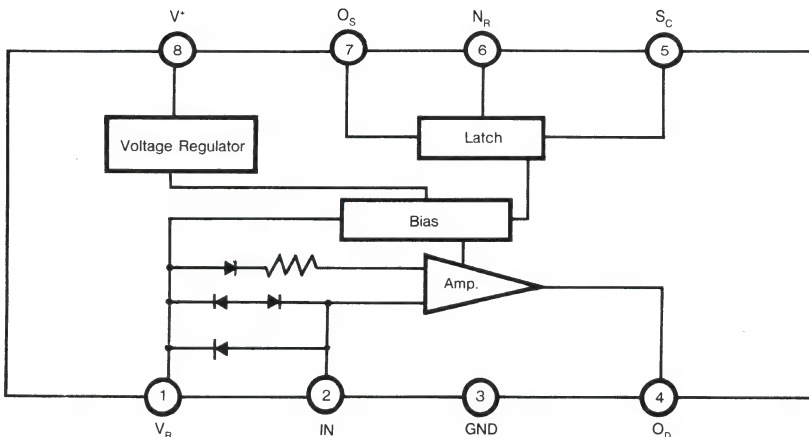
Feature

- Low Power Consumption ($P_D = 5\text{mW}$) 100V/200V
- 100V/200V Common Built-in Voltage Regulator
- High Gain Differential Amplifier
- High Input Sensitivity
- Minimum External Parts
- Large Surge Margin
- Wide Operating Temperature Range ($T_A = -30$ to 85°C)
- High Noise Immunity

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage	20	V
Supply Current	8	mA
Power Dissipation	200	mW
Operating Temperature	-30 to 85	$^\circ\text{C}$
Storage Temperature	-55 to 125	$^\circ\text{C}$

Block Diagram



Recommended Operating Condition: $T_A = -30^{\circ}\text{C}$ to 80°C

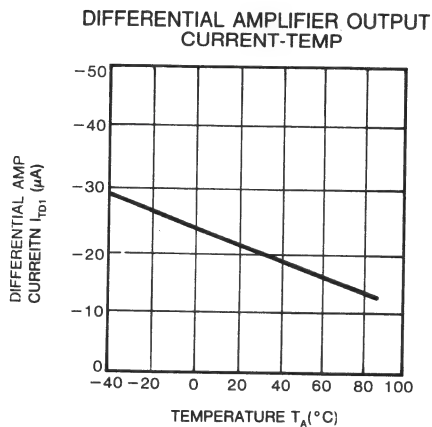
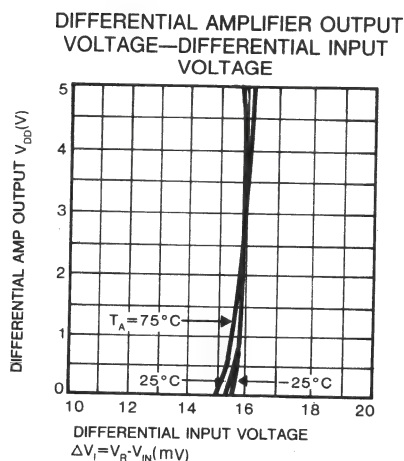
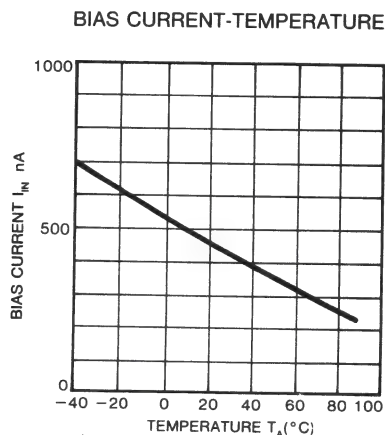
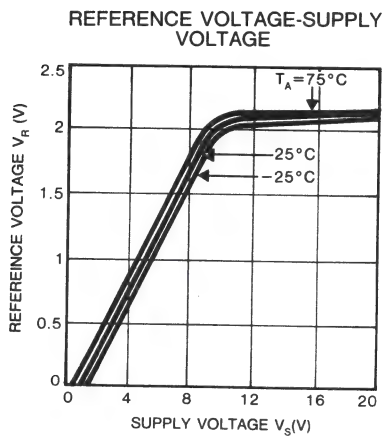
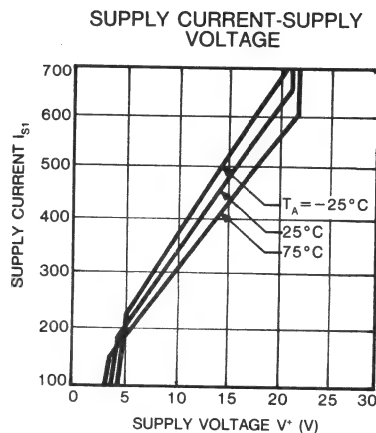
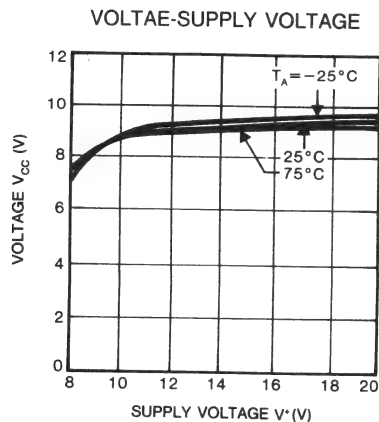
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^*	12			V
V_S -GND Capacitor	C_{VS}	1			μF
O_S -GND Capacitor	C_{OS}			1	μF

Electrical Characteristics

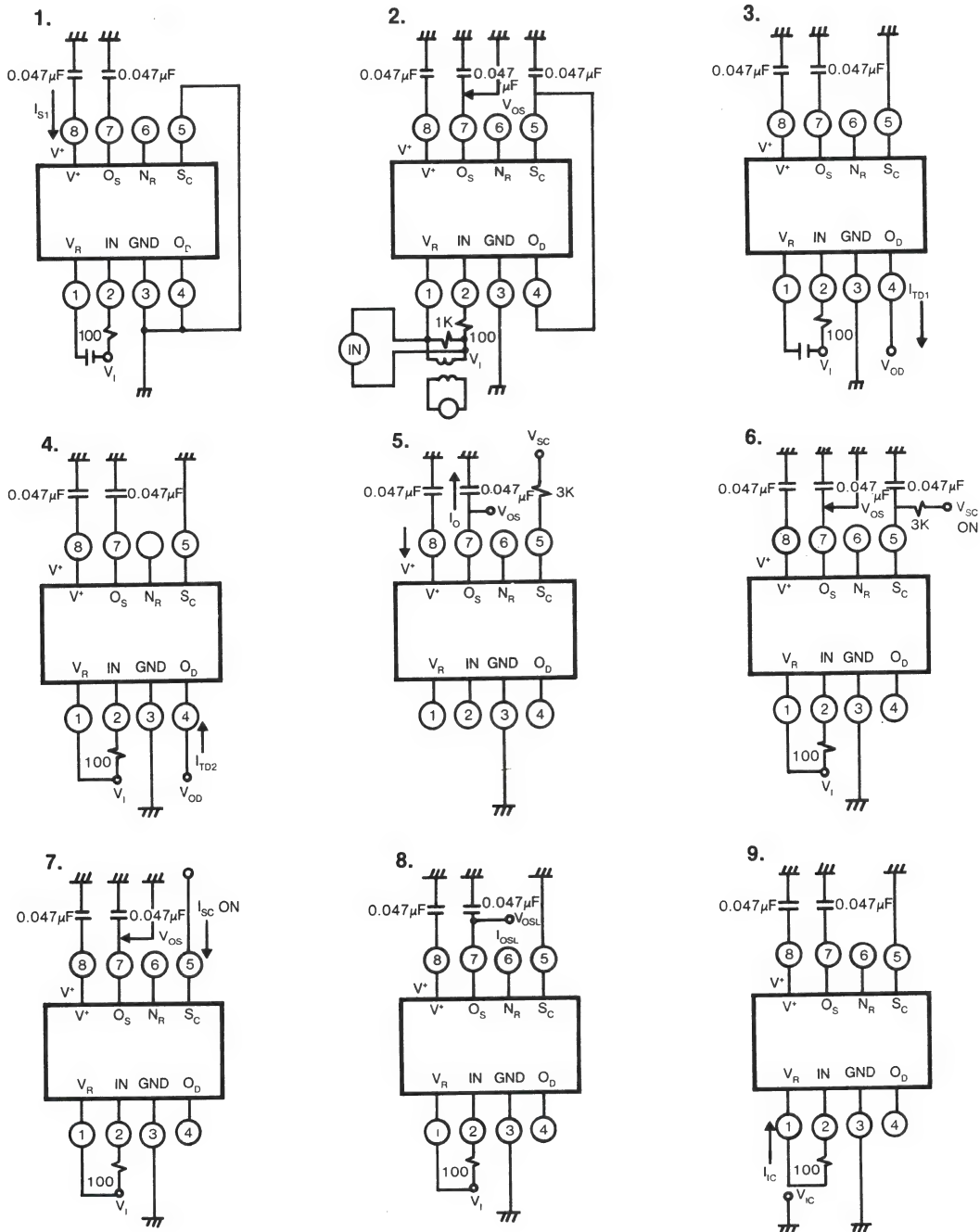
PARAMETER	SYMBOL	CONDITIONS	TEMP. ($^{\circ}\text{C}$)	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT
Supply Current 1	I_{S1}	$V^* = 12\text{V}$, $V_R - V_I = 30\text{mV}$	-30	—	—	580	μA	1
			25	—	400	530		
			85	—	—	480		
* Trip Voltage	V_T	$V^* = 16\text{V}$, $V_R - V_I = X$	-30 85	9	13.5	18	$\text{mV}_{(\text{rms})}$	2
Differential Amplifier Output Current 1	I_{TD1}	$V^* = 16\text{V}$, $V_R - V_I = 30\text{mV}$ $V_{OD} = 1.2\text{V}$	25	-12	—	-30	μA	3
Differential Amplifier Output current 2	I_{TD2}	$V^* = 16\text{V}$, $V_R - V_I$ short $V_{OD} = 0.8\text{V}$	25	17	—	37	μA	4
Output Current	I_O	$V_{SC} = 1.4\text{V}$ $V_{OS} = 0.8\text{V}$	$I_{SI} = 580\mu\text{A}$	-30	-200	—	μA	5
			$I_{SI} = 530\mu\text{A}$	25	-100	—		
			$I_{SI} = 480\mu\text{A}$	85	-75	—		
S_C On Voltage	$V_{SC \text{ ON}}$	$V^* = 16\text{V}$	25	0.7	—	1.4	V	6
S_C Input Current	$I_{SC \text{ ON}}$	$V^* = 12\text{V}$	25	—	—	5	μA	7
Output "L" Current	I_{OSL}	$V^* = 12\text{V}$, $V_{OSL} = 0.2\text{V}$	-30 85	200	—	—	μA	8
Input Clamp Voltage	V_{IC}	$V^* = 12\text{V}$, $I_{IC} = 20\text{mA}$	-30 85	4.3	—	6.7	V	9
Differential Input Clamp Voltage	V_{IDC}	$I_{IDC} = 100\text{mA}$	-30 85	0.4	—	2	V	10
Max. Current Voltage	V_{SM}	$I_{SM} = 7\text{mA}$	25	20	—	28	V	11
Supply Current 2	I_{S2}	$V_{OS} = 0.5\text{V}$, $V_R - V_I = X$	-30 85	—	—	900	μA	12
Latch Circuit Off Supply Voltage	$V_S \text{ OFF}$		25	0.5	—	—	V	13
Response Time	T_{ON}	$V^* = 16\text{V}$, $V_R - V_I = 0.3\text{V}$	25	1	—	4	ms	14

* A: 9~12.5 B: 11.5~15.5 C: 14.5~18

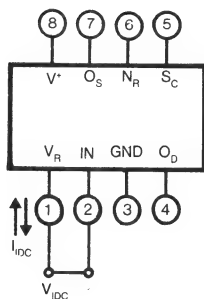
Typical Performance Curves



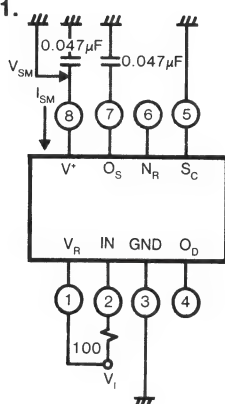
Test Circuit



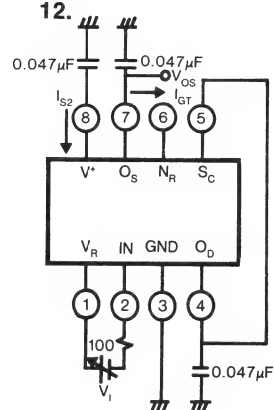
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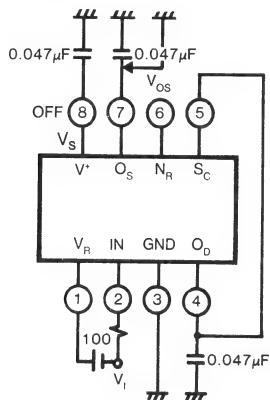
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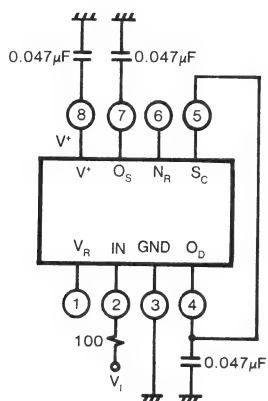
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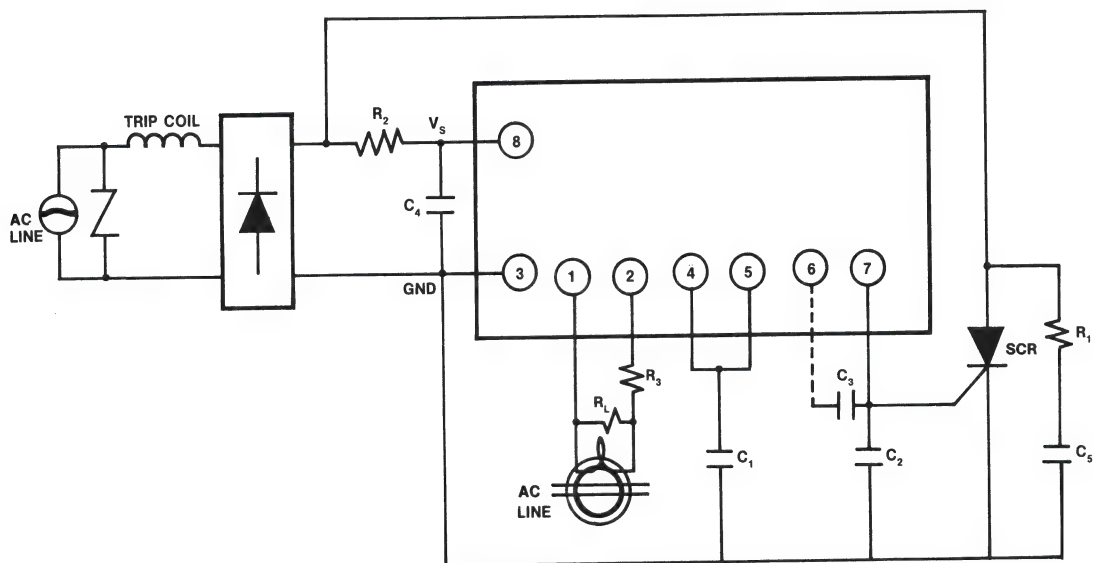
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14.



Typical Application



GM6845S

CRTC (CRT Controller)

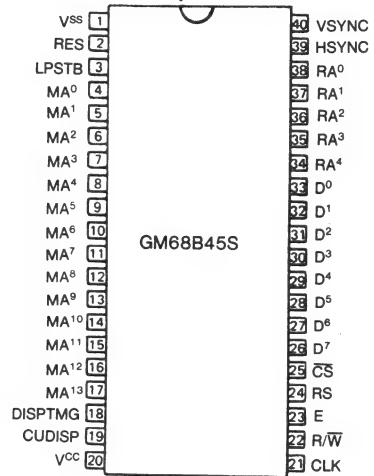
Description

The CRTC is a LSI controller which is designed to provide an interface for microcomputers to raster scan type CRT displays. Its primary function is to generate timing signal which is necessary for raster scan type CRT display according to the specification programmed by MPU. The CRTC is also designed as a programmable controller, so applicable to wide-range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

Feature

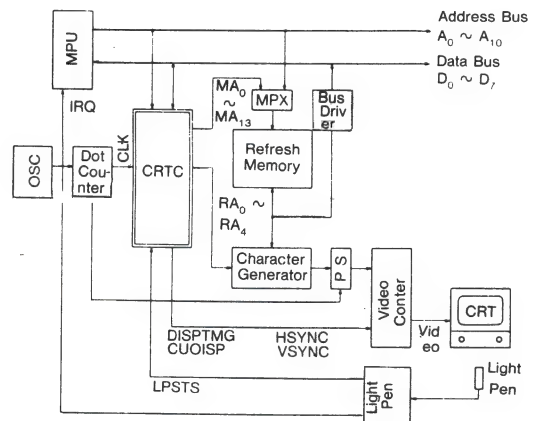
- Number of displayed characters on the screen, vertical dot format of one character, horizontal and vertical sync signal, display timing signal are programmable
- 3.7 MHz high speed display operation
- Line buffer-less refreshing
- 14-bit refresh memory address output (16K words max. Access)
- Programmable interlace/ non-interlace scan mode
- Built-in cursor control function
- Programmable cursor height and its blink
- Built-in light pen detection function
- Paging and scrolling capability
- TTL compatible
- Single +5V power supply

Pin Configuration



(Top View)

Block Diagram



Device Classification

CRTS	Bus Timing	CRT Display Timing
GM6845S	1.0 MHz	3.7 MHz max.
GM68A45S	1.5 MHz	
GM68B45S	2.0 MHz	

Absolute Maximum Ratings

SYMBOL	PARAMETER	VALUE	UNIT
V_{CC}^*	Supply Voltage	$-0.3 \sim +7.0$	V
V_{IN}^*	Input Voltage	$-0.3 \sim +7.0$	V
T_{opr}	Operating Temperature	$-20 \sim +75$	°C
T_{stg}	Storage Temperature	$-55 \sim +150$	°C

* With respect to V_{SS} (SYSTEM GND)

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}^*	Supply Voltage	4.75	5.0	5.25	V
V_{IL}^*	Input Voltage	-0.3	—	0.8	V
V_{IH}^*		2.0	—	V_{CC}	V
T_{opr}	Operating Temperature	-20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

Electrical Characteristics

DC Characteristics ($V_{CC}=5V \pm 5\%$, $V_{SS}=0V$, $T_A=-20 \sim +75^\circ\text{C}$, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V _{IH}	Input “High” Voltage			2.0	—	V _{CC}	V
V _{IL}	Input “Low” Voltage			−0.3	—	0.8	V
I _{IN}	Input Leakage Current	V _{IN} =0~5.25V (Except D ₀ ~D ₇)		−2.5	—	2.5	μA
I _{TSI}	Three-State Input Current (off-state)	V _{IN} =0.4~2.4V V _{CC} =5.25V (D ₀ ~D ₇)		−10	—	10	μA
V _{OH}	Output “High” Voltage	I _{LOAD} =−205μA (D ₀ ~D ₇)		2.4	—	—	V
		I _{LOAD} =−100μA (Other Outputs)					
V _{OL}	Output “Low” Voltage	I _{LOAD} =1.6mA		—	—	0.4	V
C _{IN}	Input Capacitance	V _{IN} =0 T _A =25 °C f=1.0 MHz	D ₀ ~D ₇	—	—	12.5	pF
			Other Inputs	—	—	10.0	pF
C _{out}	Output Capacitance	V _{IN} =0V, T _A =25 °C, f=1.0 MHz		—	—	10.0	pF
P _D	Power Dissipation			—	600	1000	mW

AC Characteristics ($V_{CC}=5V\pm5\%$, $V_{SS}=0V$, $T_A=-20\sim+75^\circ C$, unless otherwise noted.)

1. Timing of CRTC Signal

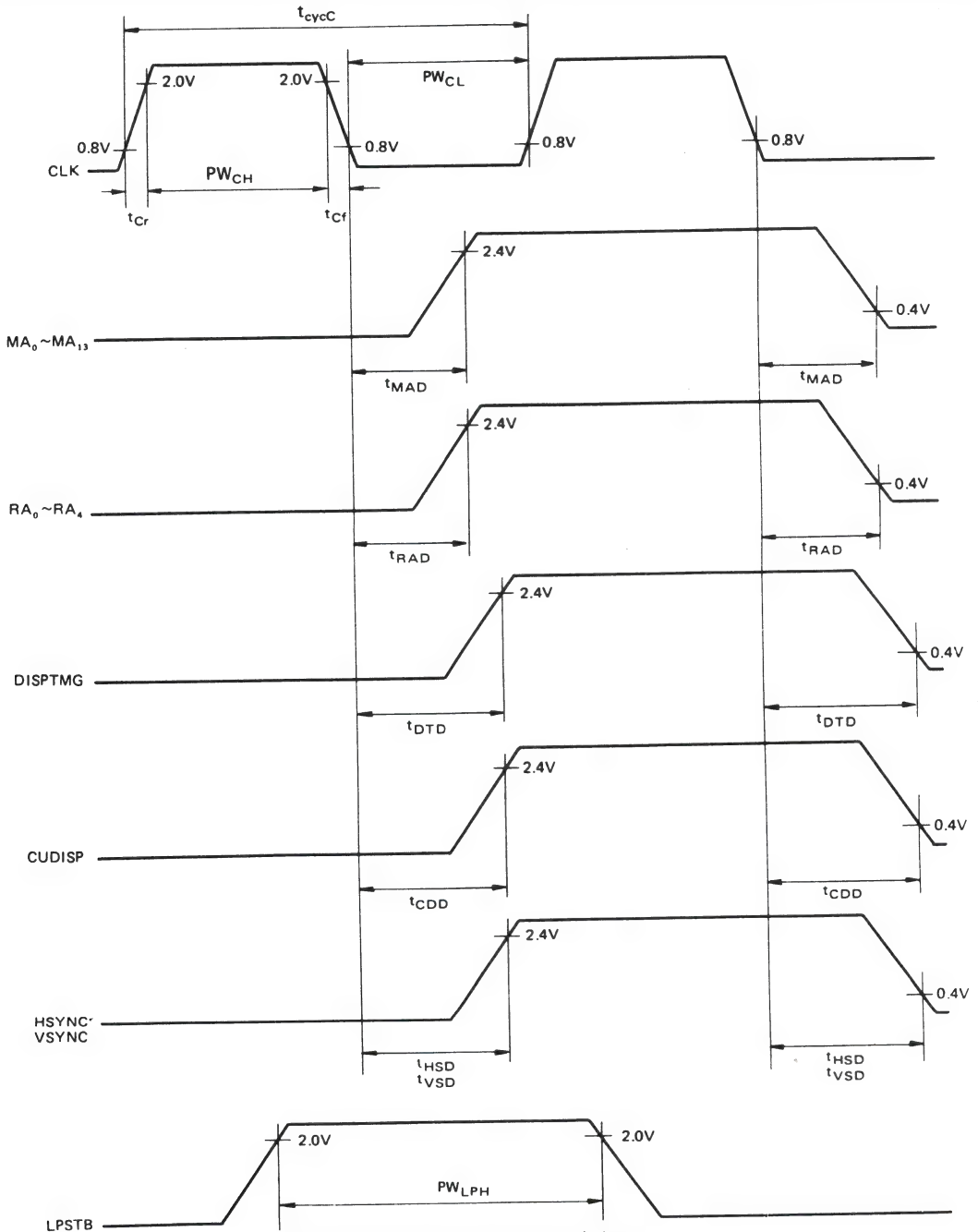
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{cycC}	Clock Cycle Time	Fig. 1	270	—	—	ns
PW_{CH}	Clock "High" Pulse Width		130	—	—	ns
PW_{CL}	Clock "Low" Pulse Width		130	—	—	ns
t_{Cr} , t_{Cf}	Rise and Fall Time for Clock Input		—	—	20	ns
t_{MAD}	Memory Address Delay Time		—	—	160	ns
t_{RAD}	Raster Address Delay Time		—	—	160	ns
t_{DTD}	DISPTMG Delay Time		—	—	250	ns
t_{CDD}	CUDISP Delay Time		—	—	250	ns
t_{HSD}	Horizontal Sync Delay Time		—	—	200	ns
t_{VSD}	Vertical Sync Delay Time		—	—	250	ns
PW_{LPH}	Light Pen Strobe Pulse Width		60	—	—	ns
t_{LPD1}	Light Pen Strobe	Fig. 2	—	—	70	ns
t_{LPD2}	Uncertain Time of Acceptance		—	—	0	ns

2. MPU Read Timing

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{cycE}	Enable Cycle Time	Fig. 3	0.22	—	—	μs
PW_{EH}	Enable "High" Pulse Width		0.22	—	—	μs
PW_{EL}	Enable "Low" Pulse Width		0.21	—	—	μs
t_{Er} , t_{Ef}	Enable Rise and Fall Time		—	—	25	ns
t_{AS}	Address Set Up Time		70	—	—	ns
t_{DDR}	Data Delay Time		—	—	180	ns
t_H	Data Hold Time		10	—	—	ns
t_{AH}	Address Hold Time		10	—	—	ns
t_{ACC}	Data Access Time		—	—	250	ns

3. MPU Write Timing

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{cycE}	Enable Cycle Time	Fig. 4	0.5	—	—	μs
PW_{EH}	Enable "High" Pulse Width		0.22	—	—	μs
PW_{EL}	Enable "Low" Pulse Width		0.21	—	—	μs
t_{Er} , t_{Ef}	Enable Rise and Fall Time		—	—	25	ns
t_{AS}	Address Set Up Time		70	—	—	ns
t_{DSW}	Data Set Up Time		60	—	—	ns
t_H	Data Hold Time		10	—	—	ns
t_{AH}	Address Hold Time		10	—	—	ns



This Figures shows the relation in time between CLK signal and each output signals. Output sequence is shown in Figs. 10~15.

Figure 1. Time Chart of the CRTC

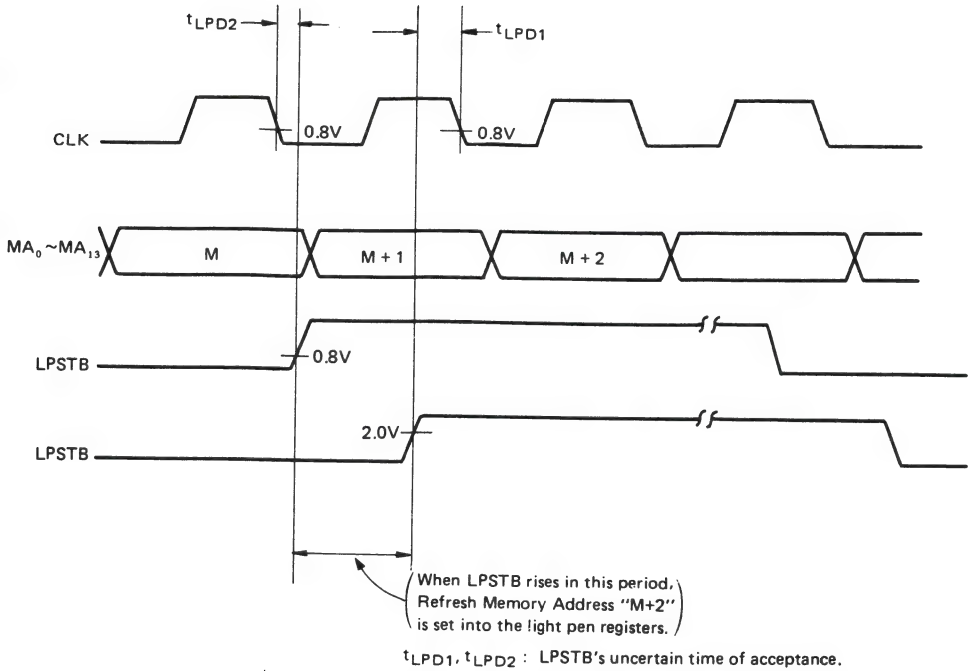


Figure 2. LPSTB Input Timing & Refresh Memory Address that is set into the light pen registers.

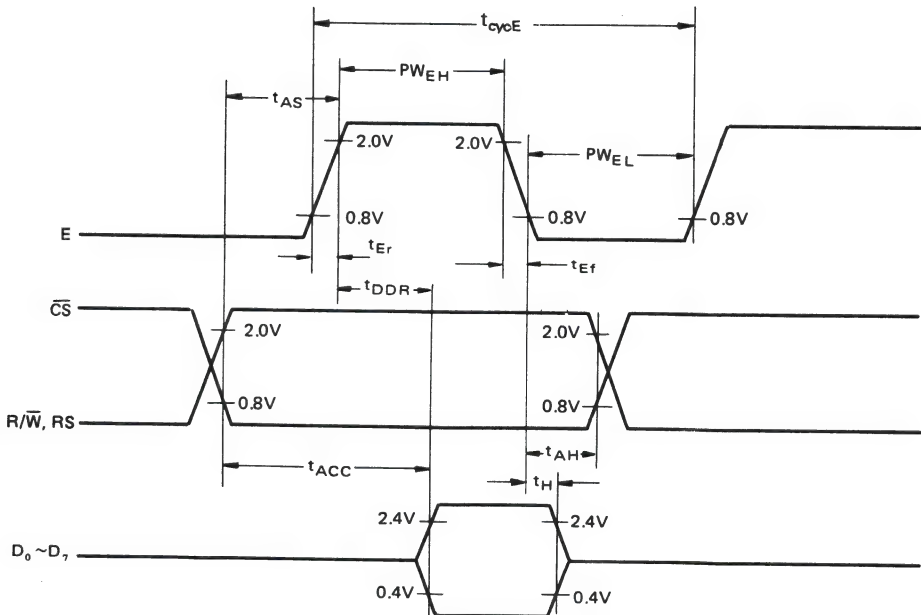


Figure 3. Read Sequence

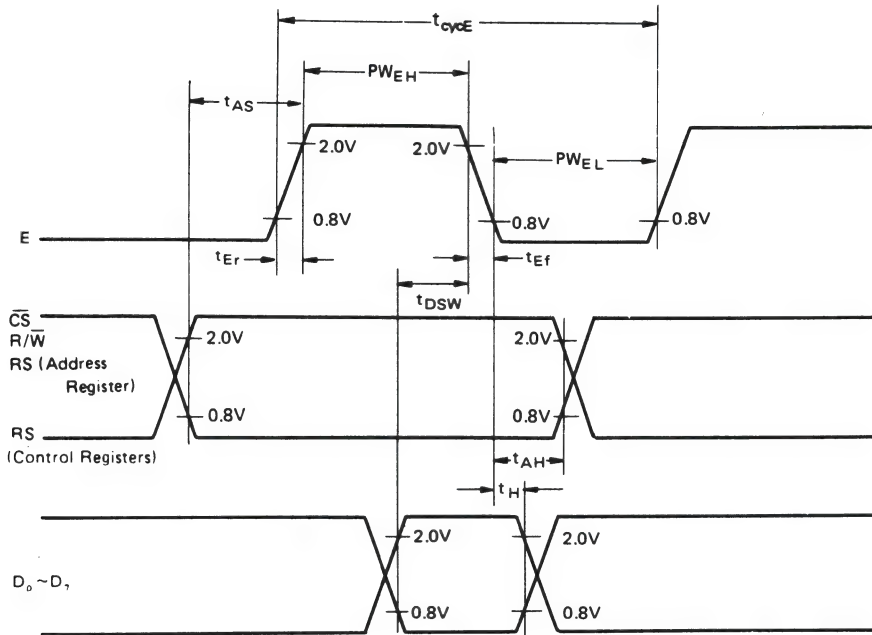


Figure 4. Write Sequence

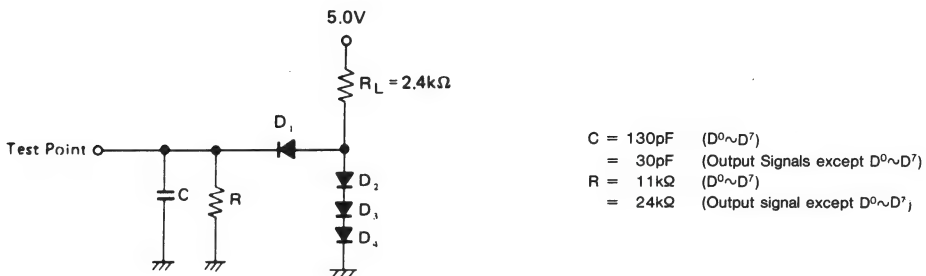


Figure 5. Test Loads

SYSTEM DESCRIPTION

The CRTC is a LSI which is connected with MPU and CRT display device to control CRT display. The CRTC consists of internal register group, horizontal and vertical timing circuits, linear address generator, cursor control circuit, and light pen detection circuit. Horizontal and vertical timing circuit generate $RA_0 \sim RA_4$, DISPTMG, HSYNC, and VSYNC. $RA_0 \sim RA_4$ are raster address signals and used as input signals are received by video control circuit. This horizontal and vertical timing circuit consists of internal counter and comparator circuit. Linear address generator

generates refresh memory address $MA_0 \sim MA_{13}$ to be used for refreshing the screen. By these address signals, refresh memory is accessed periodically. As 14 refresh memory address signals are prepared, 16K words max are accessible. Moreover, the use of start address register enables paging and scrolling. Light pen detection circuit detects light pen position on the screen. When light pen strobe signal is received, light pen register memorizes linear address generated by linear address generator in order to memorize where light pen is on the screen. Cursor control circuit controls the position of cursor, its height, and its blink.

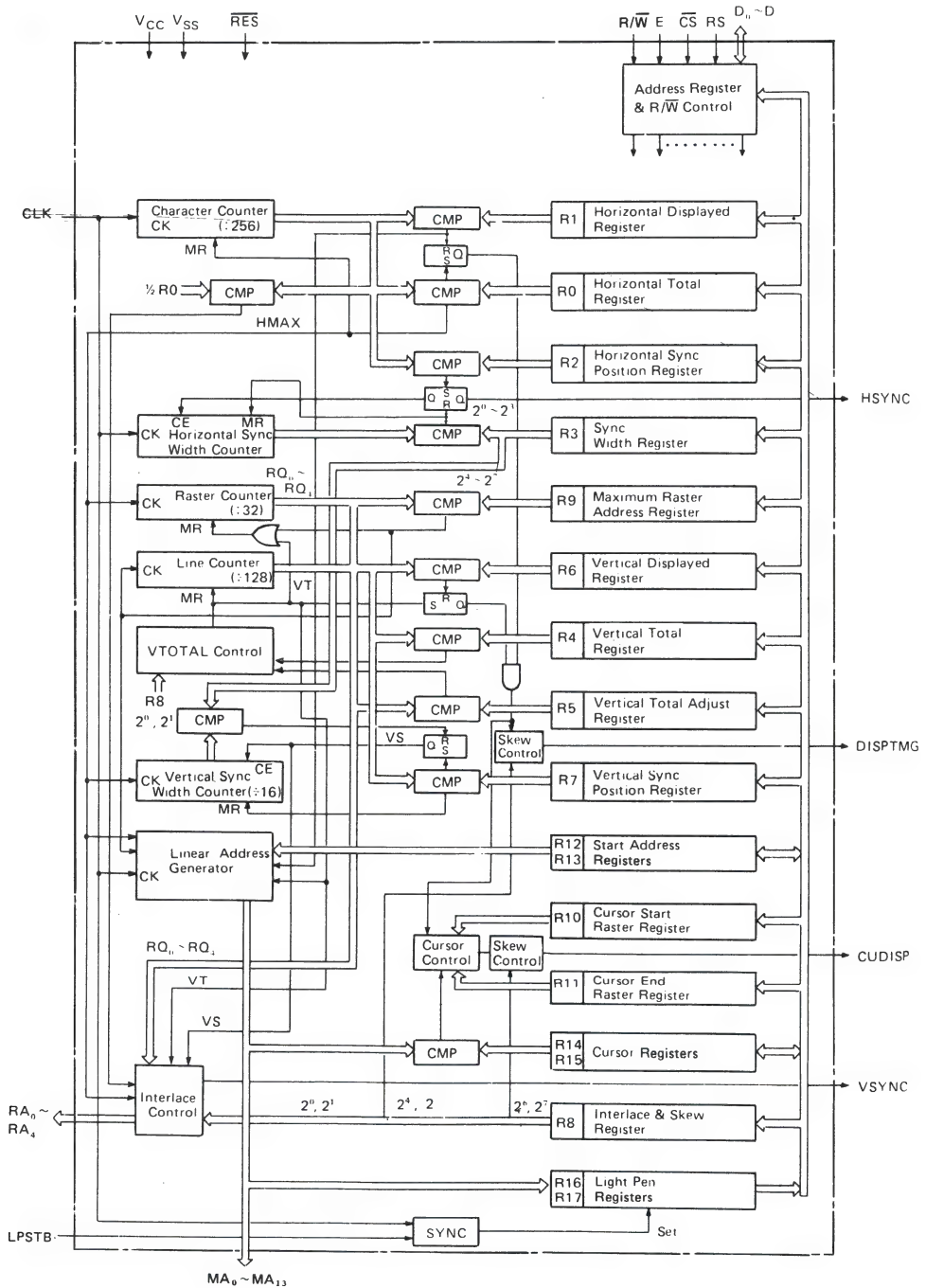


Figure 6. Internal Block Diagram of the CRTC

■ FUNCTION OF SIGNAL LINE

The CRTC provides 13 interface signals to MPU and 25 interface signals to CRT display.

• Interface Signals to MPU

Bi-directional Data Bus ($D_0 \sim D_7$)

Bi-directional data bus ($D_0 \sim D_7$) are used for data transfer between the CRTC and MPU. The data bus outputs are 3-state buffers and remain in the high-impedance state except when MPU performs a CRTC read operation.

Read/Write (R/W)

Read/Write signal (R/W) controls the direction of data transfer between the CRTC and MPU. When R/W is at "High" level, data of CRTC is transferred to MPU. When R/W is at "Low" level, data of MPU is transferred to CRTC.

Chip Select (CS)

Chip Select signal (CS) is used to address the CRTC. When CS is at "Low" level, it enables Read/Write operation to CRTC internal registers. Normally this signal is derived from decoded address signal of MPU under the condition that VMA of MPU is at "High" level.

Register Select (RS)

Register Select signal (RS) is used to select the address register and 18 control registers of the CRTC. When RS is at "Low" level, the address register is selected and when RS is at "High" level, control registers are selected. This signal is normally a derivative of the lowest bit (A0) of MPU address bus.

Enable(E)

Enable signal (E) is used as strobe signal in MPU Read/Write operation with the CRTC internal registers. This signal is normally a derivative of the processor MPU clock.

Reset (RES)

Reset signal (RES) is an input signal used to reset the CRTC.

When RES is at "Low" level, it forces the CRTC into the following status.

- 1) All the counters in the CRTC are cleared and the device stops the display operation.
- 2) All the outputs go down to "Low" level.
- 3) Control registers in the CRTC are not affected and remain unchanged.

This signal is different from other HMCS6800[®] parts in the following functions and has restrictions for usage.

- 1) RES has capability of reset function only when LPSTB is at "Low" level.
- 2) The CRTC starts the display operation immediately after RES Goes "High" level.

• Interface Signals to CRT Display Device

Character Clock (CLK)

CLK is a standard clock input signal which defines character timing for the CRTC display operation. CLK is normally derived from the external high-speed dot timing logic.

Horizontal Sync (HSYNC)

HSYNC is an active "High" level signal which provides horizontal synchronization for display device.

Vertical Sync (VSYNC)

VSYNC is an active "High" level signal which provides vertical synchronization for display device.

Display Timing (DISPTMG)

DISPTMG is an active "High" level signal which defines the display period in horizontal and vertical raster scanning. It is necessary to enable video signal only when DISPTMG is at "High" level.

Refresh Memory Address ($MA_0 \sim MA_{13}$)

$MA_0 \sim MA_{13}$ are refresh memory address signals which are used to access to refresh memory in order to refresh the CRT screen periodically. These outputs enable 16k words max. refresh memory access. So, for instance, these are applicable up to 2000 characters/screen and 8-page system.

Raster Address ($RA_0 \sim RA_4$)

$RA_0 \sim RA_4$ are raster address signals which are used to select the raster of the character generator or graphic pattern generator etc.

Cursor Display (CUDISP)

CUDISP is an active "High" level video signal which is used to display the cursor on the CRT screen. This output is inhibited while DISPTMG is at "Low" level. Normally this output is mixed with video signal and provided to the CRT display device.

Light Pen Strobe (LPSTB)

LPSTB is an active "High" level input signal which accepts strobe pulse detected by the light pen and control circuit. When this signal is activated the refresh memory address ($MA_0 \sim MA_{13}$) which are shown in Fig. 2 are stored in the 14-bit light pen register. The stored refresh memory address need to be corrected in software, taking the delay time of the display device, light pen, and light pen control circuits into account.

REGISTER DESCRIPTION

Table 1 Internal Registers Assignment

CS	RS	Address Register	Register #	Register Name	Program Unit	READ	WRITE	Data Bit							
		4 3 2 1 0						7	6	5	4	3	2	1	0
1	x	x x x x x			—	—	—								
0	0	x x x x x	AR	Address Register	—	x	o								
0	1	0 0 0 0 0	R0	Horizontal Total*	Character	x	o								
0	1	0 0 0 0 1	R1	Horizontal Displayed	Character	x	o								
0	1	0 0 0 1 0	R2	Horizontal Sync* Position	Character	x	o								
0	1	0 0 0 1 1	R3	Sync Width	Vertical-Raster, Horizontal Character	x	o	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0 0 1 0 0	R4	Vertical Total	Line	x	o								
0	1	0 0 1 0 1	R5	Vertical Total Adjust	Raster	x	o								
0	1	0 0 1 1 0	R6	Vertical Displayed	Line	x	o								
0	1	0 0 1 1 1	R7	Vertical Sync Position	Line	x	o								
0	1	0 1 0 0 0	R8	Interlace & Skew	—	x	o	C1	C0	D1	D0			V	S
0	1	0 1 0 0 1	R9	Maximum Raster Address	Raster	x	o								
0	1	0 1 0 1 0	R10	Cursor Start Raster	Raster	x	o		B	P					
0	1	0 1 0 1 1	R11	Cursor End Raster	Raster	x	o								
0	1	0 1 1 0 0	R12	Start Address(H)	—	o	o								
0	1	0 1 1 0 1	R13	Start Address(L)	—	o	o								
0	1	0 1 1 1 0	R14	Cursor(H)	—	o	o								
0	1	0 1 1 1 1	R15	Cursor(L)	—	o	o								
0	1	1 0 0 0 0	R16	Light Pen(H)	—	o	x								
0	1	1 0 0 0 1	R17	Light Pen(L)	—	o	x								

(NOTE) 1. The Registers marked *: (Written Value) = (Specified Value) - 1

2. Written Value of R9 is mentioned below.

1) Non-interlace Mode
Interlace Sync Mode } (Written Value) = (Specified Value) - 12) Interlace Sync
Video Mode } (Written Value) = (Specified Value) - 2

3. C0 and C1 specify skew of CUDISP.

D0 and D1 specify skew of DISPTMG.

When S is "1", V specifies video mode. S specifies the Interlace Sync Mode.

4. B specifies the cursor blink. P specifies the cursor blink period.

5. wv0~wv3 specify the pulse width of Vertical Sync Signal.

wh0~wh3 specify the pulse width of Horizontal Sync Singla.

6. R0 is ordinarily programmed to be odd number in interlace mode.

7. o: Yes, x: No

■ FUNCTION OF INTERNAL REGISTERS

• Address Register (AR)

This is a 5-bit register used to select 18 internal control registers ($R_0 \sim R_{17}$). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to $R_0 \sim R_{17}$ requires, first of all to write the address of corresponding control register into this register. When RS and \overline{CS} and at "Low" level, this register is selected.

• Horizontal Total Register (R0)

This is a register used to program total number of horizontal characters per line including the retrace period. The data is 8-bit and its value should be programmed according to the specification of the CRT. When M is total number of characters, M-1 shall be programmed to this register. When programming for interlace mode, M must be even.

• Horizontal Displayed Register (R1)

This is a register used to program the number of horizontal displayed characters per line. Data is 8-bit and any number that is smaller than that of horizontal total characters can be programmed.

• Horizontal Sync Position Register (R2)

This is a register used to program horizontal sync position as multiples of the character clock period. Data is 8-bit and any number that is lower than the horizontal total number can be programmed. When H is character number of horizontal Sync Position, H-1 shall be programmed to this register. When programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

• Sync Width Register (R3)

This is a register used to program the horizontal sync pulse width and the vertical sync pulse width. The horizontal sync pulse width is programmed in the lower 4-bit as multiples of the character clock period. "0" can't be programmed. The vertical sync pulse width is programmed in higher 4-bit as multiples of the raster period. When "0" is programmed in higher 4-bit, 16 raster period (16H) is specified.

• Vertical Total Register (R4)

This is a register used to program total number of lines per frame including vertical retrace period. The data is within 7-bit and its value should be programmed according to the specification of the CRT. When N is total number of lines, N-1 shall be programmed to this register.

• Vertical Total Adjust Register (R5)

This is a register used to program the optimum number of adjust total number of rasters per field. This register enables to decide the number of vertical deflection frequency more strictly.

• Vertical Displayed Register (R6)

This is a register used to program the number of displayed character rows on the CRT screen. Data is 7-bit and any number that is smaller than that of vertical total characters can be programmed.

Table 2 Pulse Width of Vertical Sync Signal

VSW				Pulse Width
2^7	2^6	2^5	2^4	
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

H: Raster period

Table 3 Pulse Width of Horizontal Sync Signal

HSW				Pulse Width
2^3	2^2	2^1	2^0	
0	0	0	0	—(Note)
0	0	0	1	1 CH
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CH: Character clock period

(Note) HSW "0" can't be used.

• **Vertical Sync Position Register (R7)**

This is a register used to program the vertical sync position on the screen as multiples of the horizontal character line period. Data is 7-bit and any number that is equal to or less than vertical total characters can be programmed. When V is character number of vertical sync position, V-1 shall be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

• **Interlace and Skew Register (R8)**

This is a register used to program raster scan mode and skew (delay) of CUDISP and DISPTMG.

Raster Scan Mode Program Bit (V, S)

Raster scan mode is programmed in the V, S bit.

Table 4 Raster Scan Mode ($2^1, 2^0$)

V	S	Raster Scan Mode.
0	0	Non-interlace Mode
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

In the non-interlace mode, the rasters of even number field and odd number field are scanned duplicatedly. In the interlace sync mode, the rasters of odd number field are scanned in the middle of even number field. Then it is controlled to display the same character pattern in two fields. In the interlace sync & video mode, the raster scan method is the same as the interlace sync mode, but it is controlled to display different character pattern in two field.

Skew Program Bit (C1, C0, D1, D0)

These are used to program the skew (delay) of CUDISP and DISPTMG.

Skew of these two kinds of signals are are programmed separately.

Table 5. DISPTMG Skew Bit ($2^5, 2^4$)

D1	D0	DISPTMG
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Table 6. CUDISP Skew Bit ($2^7, 2^6$)

C1	C0	CUDISP
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Skew function is used to delay the output timing of CUDISP and DISPTMG in LSI for the time to access refresh memory, character generator or pattern generator, and to make the same phase with serial video signal.

• **Maximum Raster Address Register (R9)**

This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including line space. This register is programmed as follows.

Non-interlace Mode, Interlace Sync Mode

When total number of rasters is RN, RN-1 shall be programmed.

Interlace Sync & Video Mode

When total number of rasters is RN, RN-2 shall be programmed.

This manual defines total number of rasters in non-interlace mode, interlace sync mode and interlace sync & video mode as follows:

Non-interlace Mode

0 _____ Total Number of Rasters:5
 1 _____ Programmed Value:Nr=4
 2 _____ (The same as displayed
 3 _____ total number of rasters)
 4 _____
 Raster Address

Interlace Sync Mode

0 _____ Total Number of Rasters:5
 1 0 Programmed Value:Nr=4
 2 1 In the interlace sync mode,
 3 2 total number of rasters in
 4 3 both the even and odd fields
 4 is ten. On programming,
 Raster Address the half of it is defined as
 total number of rasters.

Interlace Sync & Video Mode

0 _____ Total Number of Rasters:5
 1 1 Programmed Value:Nr=3
 2 3 Total number of rasters
 4 _____ displayed in the even field
 Raster Address and the odd field.

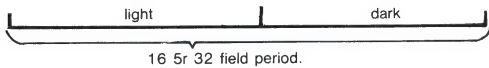
• **Cursor Start Raster Register (R10)**

This is a register used to program the cursor start raster address by lower 5-bit ($2^0 \sim 2^4$) and the cursor display mode by higher 2-bit ($2^5, 2^6$).

Table 7. Cursor Display Mode (2^5 , 2^5)

B	P	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink 16 Field Period
1	1	Blink 32 Field Period

Brink Period



• **Cursor End Raster Register (R11)**

This register is used to program the cursor end raster address.

• **Start Address Register (R12, R13)**

These are used to program the first address of refresh memory to read out.

Paging and scrolling is easily performed using this register. This register can be read but the higher 2-bit ($2^6, 2^7$) of R12 are always "0".

• **Cursor Register (R14, R15)**

These two read/write registers store the cursor location. The higher 2-bit ($2^6, 2^7$) of R14 are always "0".

• **Light Pen Register (R16, R17)**

These read-only registers are used to catch the detection address of the light pen. The higher 2-bit ($2^6, 2^7$) of R16 are always "0". Its value needs to be corrected by software because there is time delay from address output of the CRTC to signal input LPSTB pin of the CRTC in the process that raster is lit after address output and light pen detects it. Moreover, delay time shown in Fig. 2 needs to be taken into account.

Restriction on Programming Internal Register

- 1) $0 < Nhd < Nht + 1 \leq 256$
- 2) $0 < Nvd < Nvt + 1 \leq 128$
- 3) $0 \leq Nhsp \leq Nht$
- 4) $0 \leq Nvsp \leq Nvt^*$
- 5) $0 \leq N_{CSTART} \leq N_{CEND} \leq Nr$ (Non-interlace, Interlace sync mode)
 $0 \leq N_{CSTART} \leq N_{CEND} \leq Nr + 1$ (Interlace sync & video mode)
- 6) $2 \leq Nr \leq 30$ (Interlace Sync & Video mode)
- 7) $3 \leq Nht$ (Except non-interlace mode)
 $5 \leq Nht$ (Non-interlace mode only)

* In the interlace mode, pulse width is changed $\pm 1/2$ raster time when vertical sync signal extends over two fields.

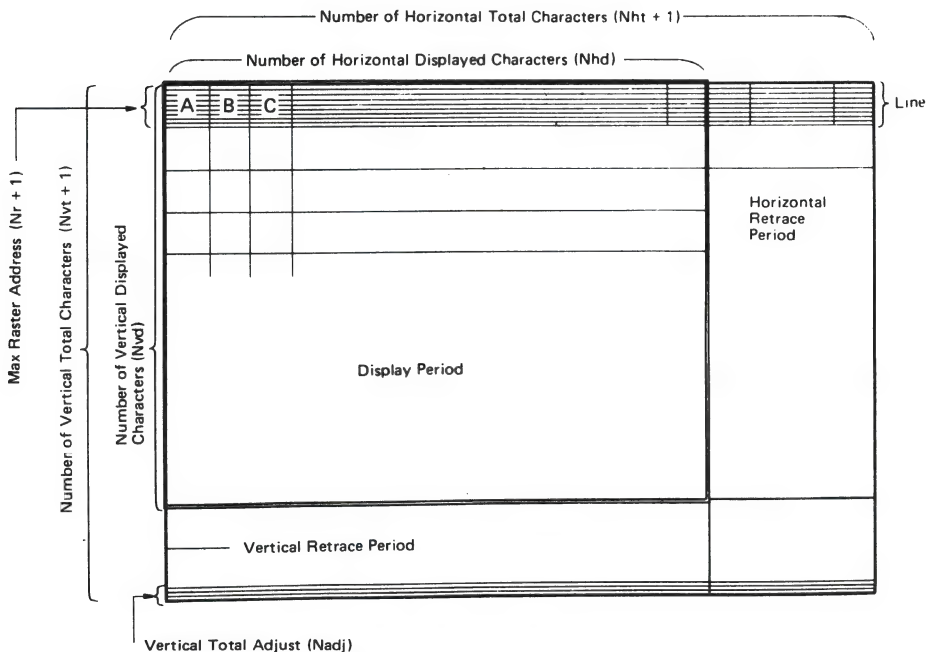


Figure 7. CRT Screen Format

Notes for Use

(1) The method of directly using the value programmed in the internal register of LSI for controlling the CRT is adopted. Consequently, the display may flicker on the screen when the contents of the registers are changed from bus side asynchronously with the display operation.

Cursor Register

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace period.

Start Address Register

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display period.

It is desirable to avoid programming other registers during display operation.

(2) The RES assertion at power-on does not define the internal registers of the GM68B45S. For a proper operation based on the system specification, all the internal registers are requested to be programmed by users after power is supplied.

■ OPERATION OF THE CRTC

• Time Chart of CRT interface Signals

The following example shows the display operation in which values of Table 8 are programmed to the CRTC internal registers. Fig. 7 shows the CRT screen format. Fig. 10 shows the time chart of signals output from the CRTC.

The relation between values of Refresh Memory Address ($MA_0 \sim MA_{13}$) and Raster Address ($RA_0 \sim RA_4$) and the display position on the screen is shown in Fig. 16. Fig. 16 shows the case where the value of Start Address is 0.

• Interface Control

Fig. 8 shows an example where the same character is displayed in the non-interface mode, interlace sync mode, and interlace sync & video mode.

Non-interface Mode Control

In non-interface mode, each field is scanned duplicatedly. The values of raster addresses ($RA_0 \sim RA_4$) are counted up one from 0.

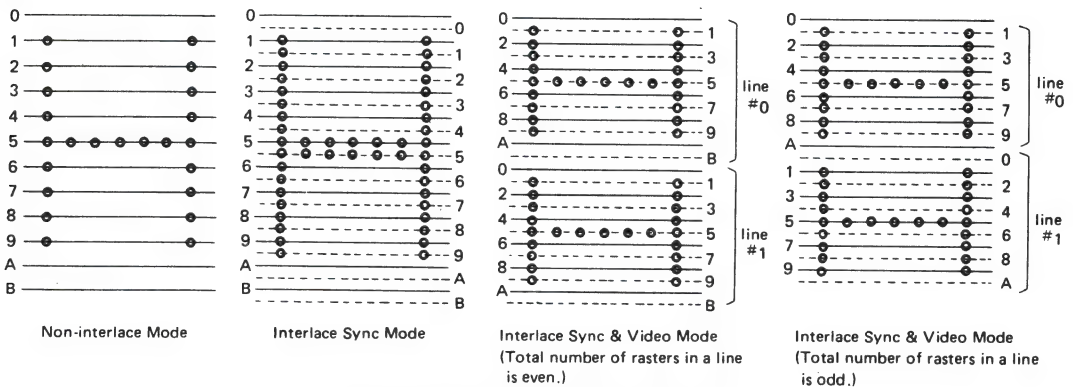


Figure 8. Example of Raster Scan Display

Table 8. Programmed Values into the Registers

Register	Register Name	Value	Register	Register Name	Value
R0	Horizontal Total	Nht	R9	Max Raster Address	Nr
R1	Horizontal Displayed	Nhd	R10	Cursor Start Raster	
R2	Horizontal Sync Position	Nhsp	R11	Cursor End Raster	
R3	Sync Width	Nvsw, Nhsw	R12	Start Address (H)	0
R4	Vertical Total	Nvt	R13	Start Address (L)	0
R5	Vertical Total Adjust	Nadj	R14	Cursor (H)	
R6	Vertical Displayed	Nvd	R15	Cursor (L)	
R7	Vertical Sync Position	Nvsp	R16	Light Pen (H)	
R8	Interlace & Skew		R17	Light Pen (L)	

(NOTE) Nhd<Nht, Nvd<Nvt

Interlace Sync Mode Control

In the interlace sync mode, raster addressed in the even field and the odd field are the same as addressed in the non-interlace mode. One character pattern is displayed mutually and its displayed position in the odd field is set at 1/2 raster space down from that in the even field.

Interlace Sync & Video Mode Control

In interlace sync & video mode, the output raster address when the number of rasters is even is different from that when the number of rasters is odd.

Table 9. The Output of Raster Address in Interlace Sync & Video Mode

Field		Even Field	Odd Field
Total Number of Rasters in a Line			
Even		Even Address	Odd Address
Odd	Even Line*	Even Address	Odd Address
	Odd Line*	Odd Address	Even Address

1) Total number of rasters in a line is even;
 When number of rasters is programmed to be even, even raster address is output in the even field and odd raster address is output in the odd field.

2) Total number of rasters in a line is odd;
 When the total number of rasters is programmed to be odd, odd and even addresses are reversed according to the odd and even lines in each field. In this case, the difference in numbers of dots displayed between even field and odd field is usually smaller than the case of 1). Then interlace can be displayed more stably.

(NOTE) The wide disparity of dots between number of dots between even field and odd field influences beam current of CRT. CRT, which has a stable high-voltage part, can make interlace display normal. On the contrary, CRT, which has unstable high-voltage part, moves deflection angle of beam current and also dots displayed in the even and odd fields, may be shifted. Characters appear distorted on a border of the screen. So 2) programming has an effect to decrease such evil influences as mentioned above. Fig. 13 shows fine chart in each mode when interlace is performed.

• **Cursor Control**

Fig. 9 shows the display patterns where each value is programmed to the cursor start raster register and the cursor end raster register. Programmed values to the cursor start raster register and the cursor end raster register need to be under the following condition.

Cursor Start Raster Register ≤ Cursor End Raster Register ≤ Maximum Raster Address.

Time chart of CUDISP is shown in Fig. 14 and Fig. 15

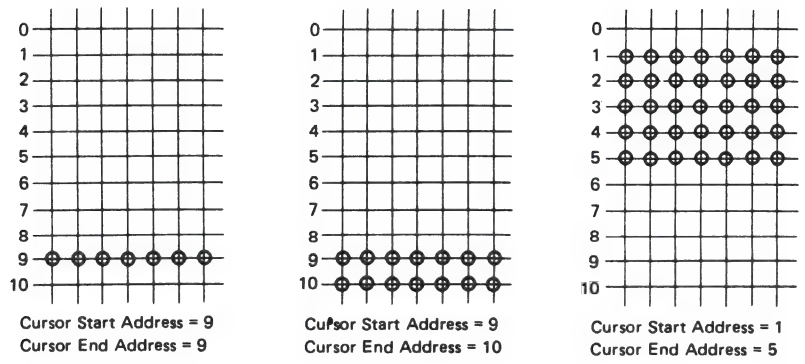


Figure 9. Cursor Control

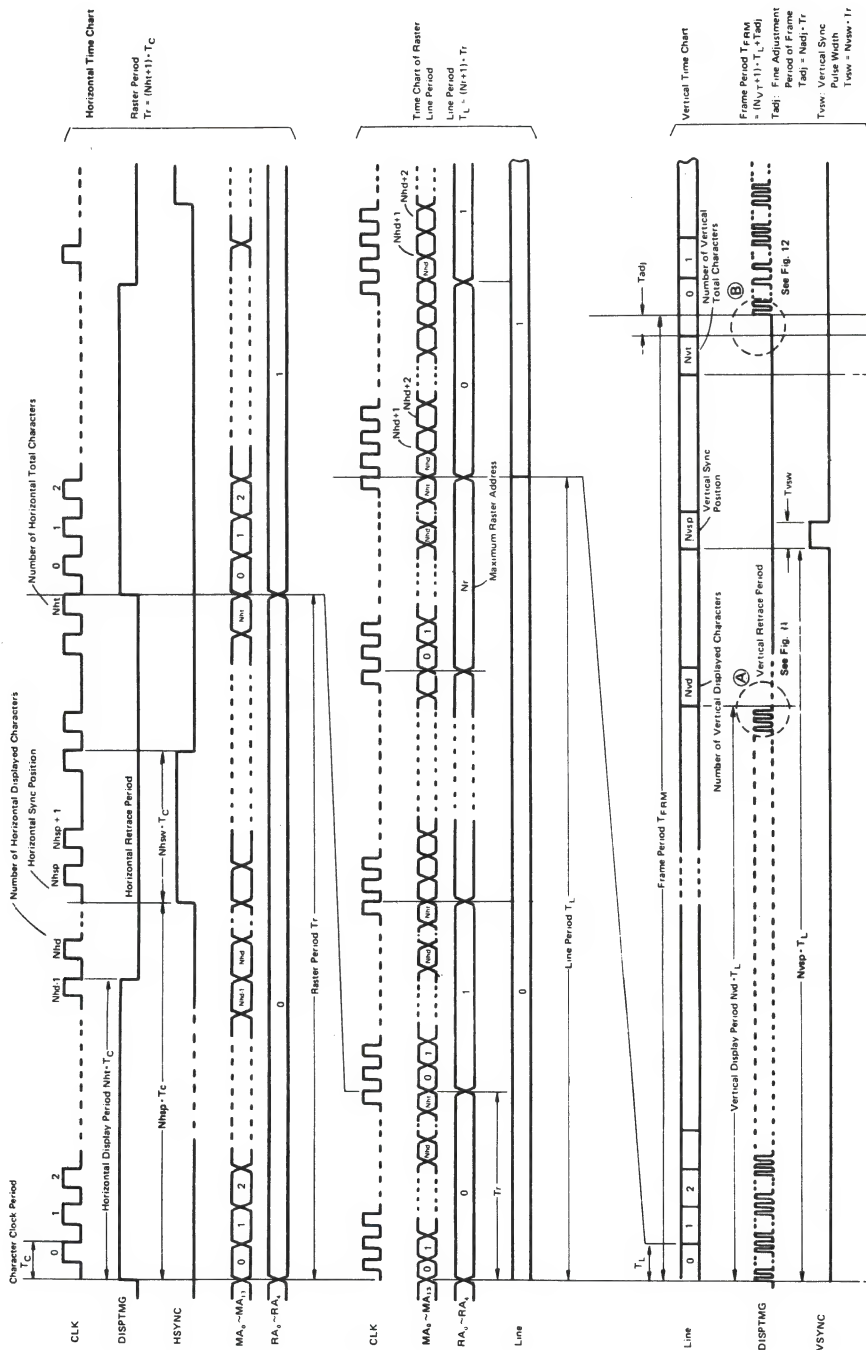


Figure 10. CRTC Time Chart

Output waveform of horizontal & vertical display in the case where values shown in Table 8 are Programmed to each register.

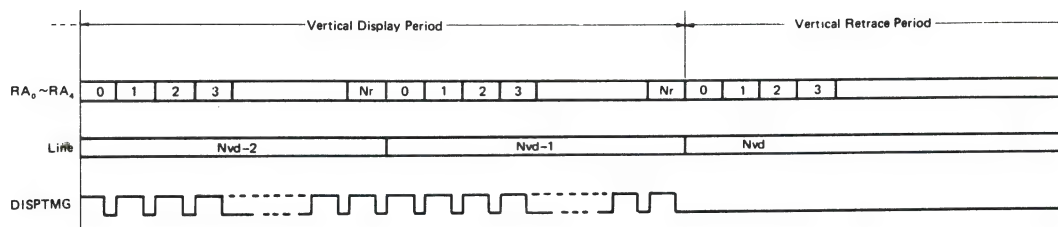


Figure 11 Switching from Vertical Display Period over to Vertical Retrace Period (Expansion of Fig. 10-A)

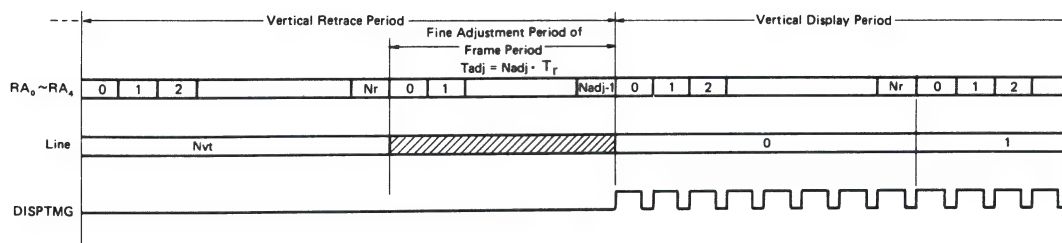


Figure 12 Fine Adjustment Period of Frame in Vertical Display (Expansion of Fig. 10-B)

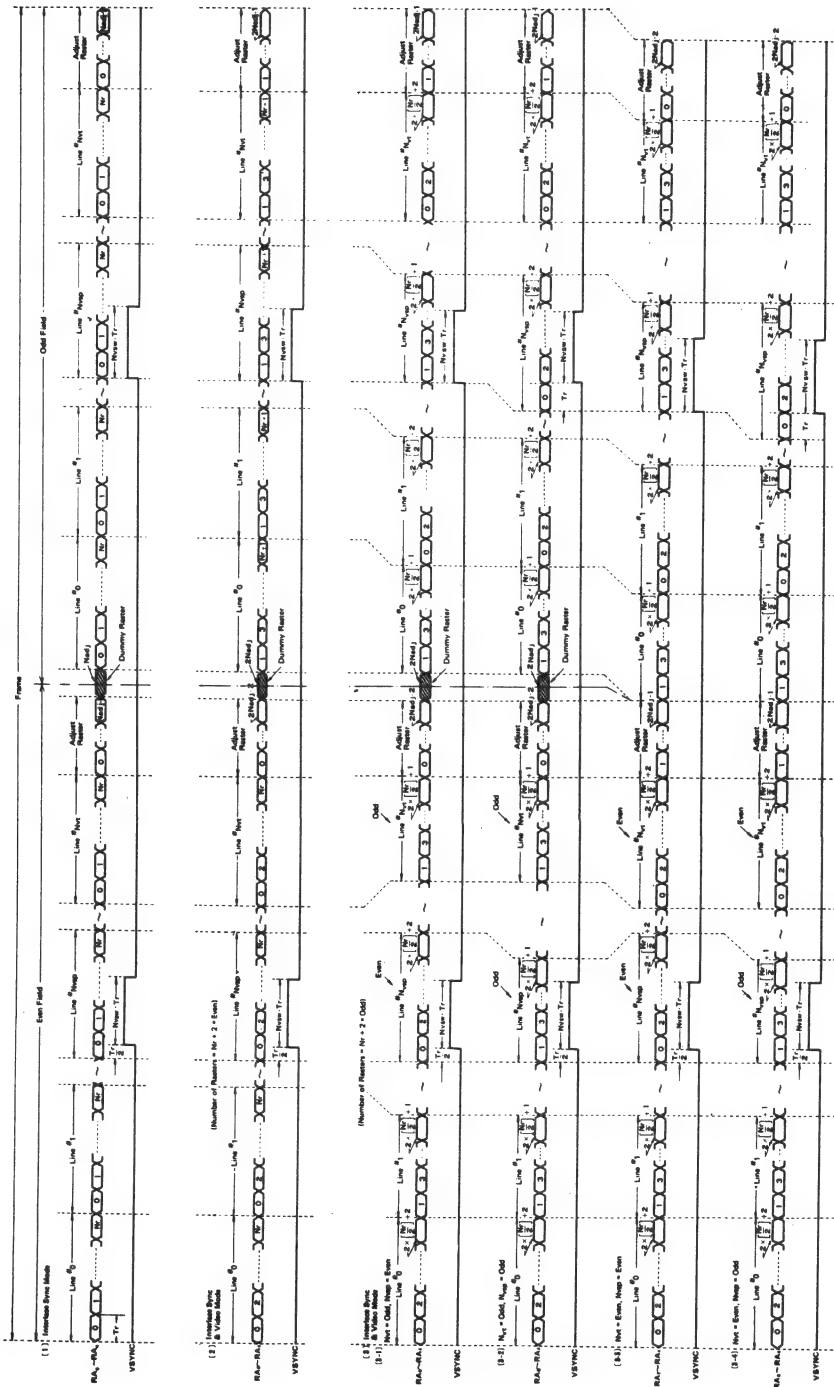


Figure 13. Fine chart in each mode when interlace is performed.

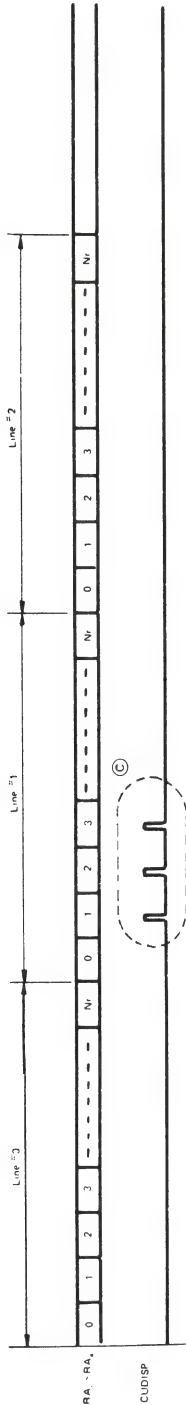
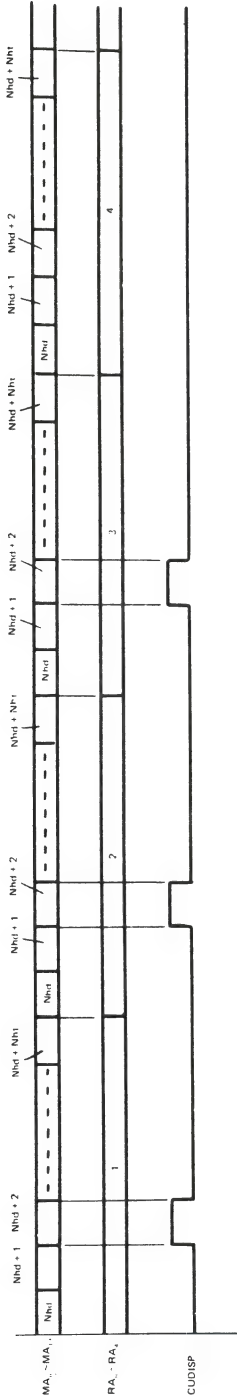


Figure 14 Relation between Line • Raster and CUDISP



(NOTE)
 Cursor register = $Nhd + 2$
 Cursor Start
 Raster Register = 1
 Cursor End
 Raster Register = 3
 are Programmed in cursor display mode.

In blink mode, it is changed into display or non-display mode when field period is 16 or 32-time period.

Figure 15 CUDISP Timing (Expansion of Fig. 14 C)

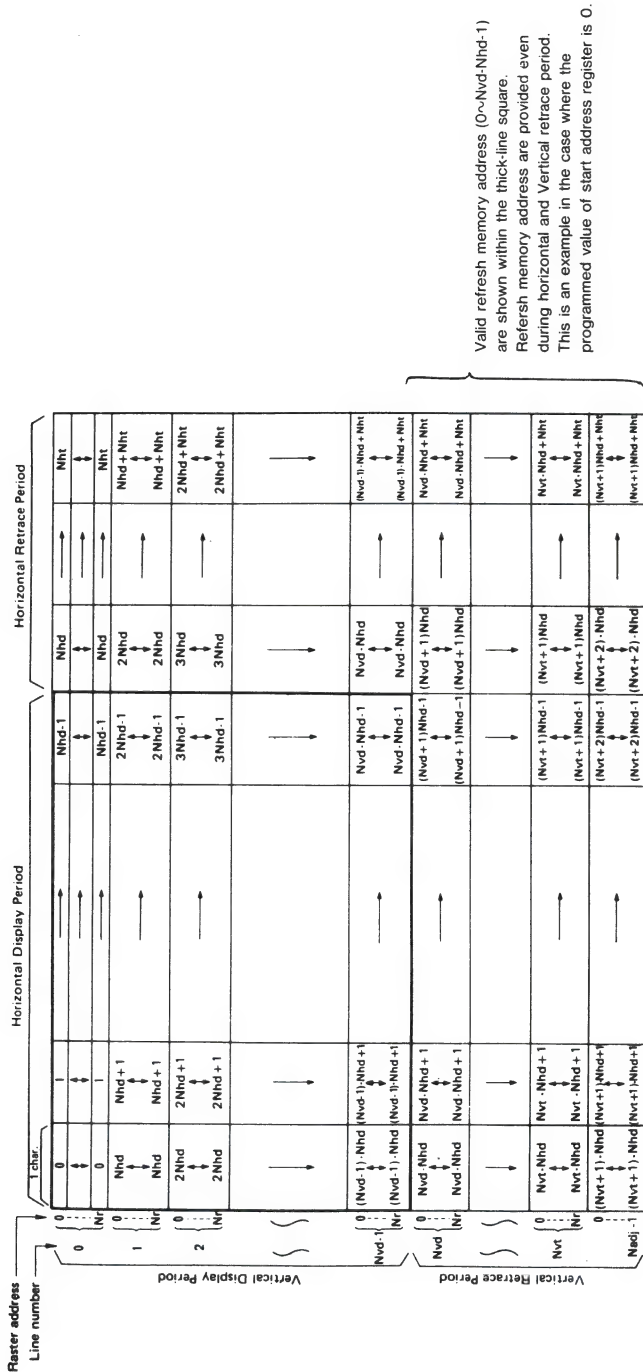


Figure 16 Refresh Memory Address (MA₀~MA₁₃)

■ HOW TO USE THE CRTC

• Interface to MPU

As shown in Fig. 17, the CRTC is connected with the standard bus of MPU to control the data transfer between them. The CRTC address is determined by \overline{CS} and RS, and the Read/Write operation is controlled in R/W and E. When \overline{CS} is "Low" and RS is also "Low", the CRTC address register is selected. When \overline{CS} is "Low" and RS is "High", one of 18 internal registers is selected.

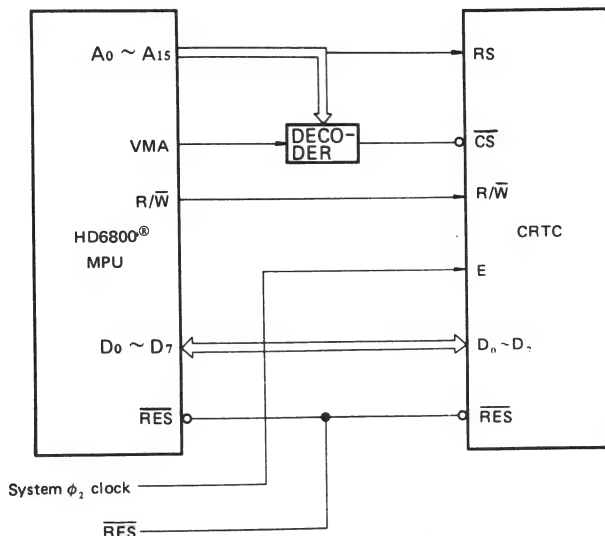


Figure 17 Interface to MPU

• Dot Timing Generating Circuit

CRTC's CLK input (21 pin) is provided with CLK which defines horizontal character time period from the outside. This CLK is generated by dot counter shown in Fig. 18. Fig. 18 shows a example of circuit where horizontal dot number of the character is "9". Fig. 19 shows the opera-

tion time chart of dot counter shown in Fig. 18. As this example shows explicitly, CLK is at "Low" level in the former half of horizontal character time and at "High" level in the latter half. It is necessary to be careful so as not to mistake this polarity.

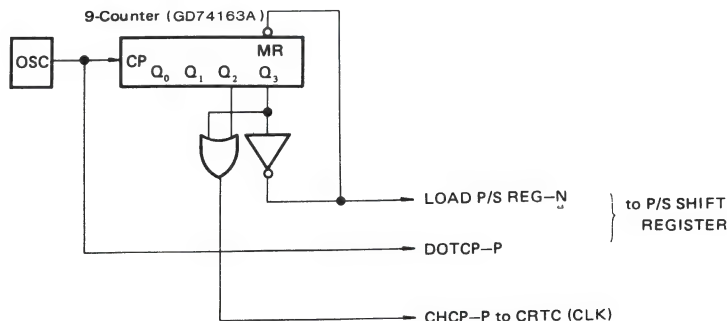


Figure 18 Example of Dot Counter

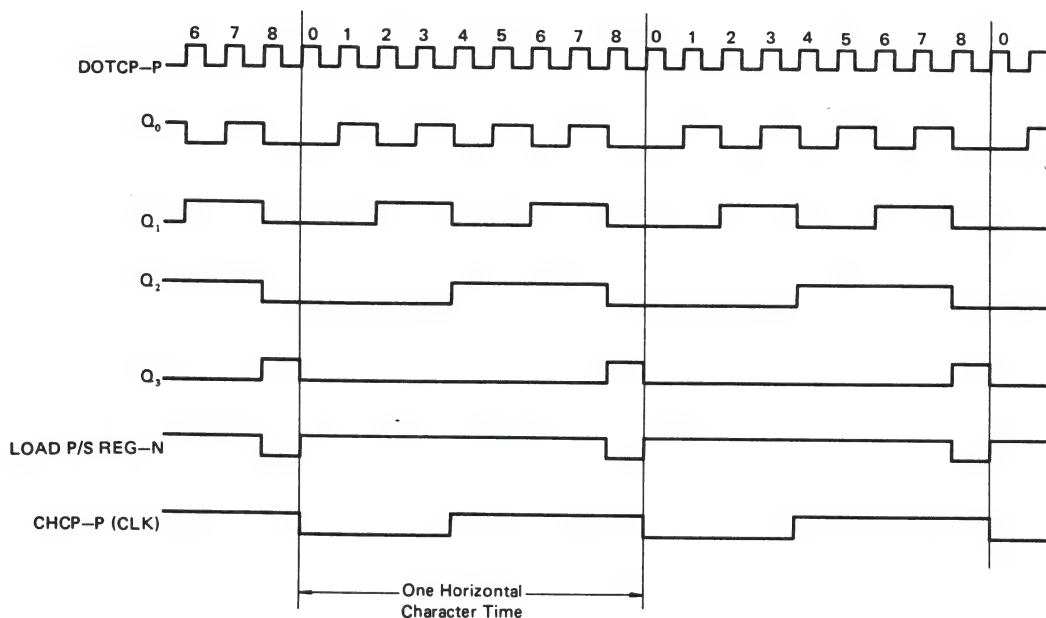


Figure 19 Time Chart of Dot Counter

■ INTERFACE TO DISPLAY CONTROL UNIT

Fig. 20 shows the interface between the CRTC and display control unit. Display control unit is mainly composed of Refresh Memory, Character Generator, and Video Control circuit. For refresh memory, 14 Memory Address line (0~16383) max are provided and for character generator, 5 Raster Address line (0~31) max are provided. For video control circuit, DISPTMG, CUDISP, HSYNC, and VSYNC are sent out. DISPTMG is used to control the blank period of video signal. CUDISP is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

Outputs from video control circuit, (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, thus characters are displayed on the screen.

Fig. 21 shows detailed block diagram of display control unit. This shows how to use CUDISP and DISPTMG. CUDISP and DISPTMG should be used being latched at least one time at external flip-flop F1 and F2. Flip-flop F1 and F2 function to make one-character delay time so as to synchronize them with video signal from parallel-serial converter. High-speed D type flip-flop as TTL is used for this purpose. After being delayed at F1 and F2 DISPTMG is AND-ed with character video signal, and CUDISP is Or-ed with output from AND gate. By using this circuitry, blanking of horizontal and vertical retrace time is controlled. And cursor video is mixed with character video signal.

Fig. 21 shows the example in the case that both refresh memory and Character Generator can be accessed for horizontal one character time. Time chart for this case is shown in Fig. 24. This method is used when a few character needed to be displayed in horizontal direction on the screen.

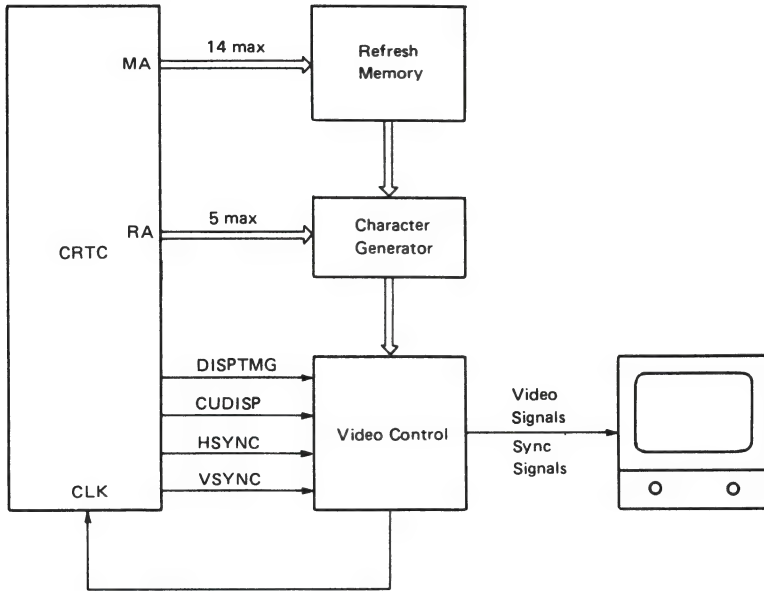


Figure 20 Interface to Display Control Unit

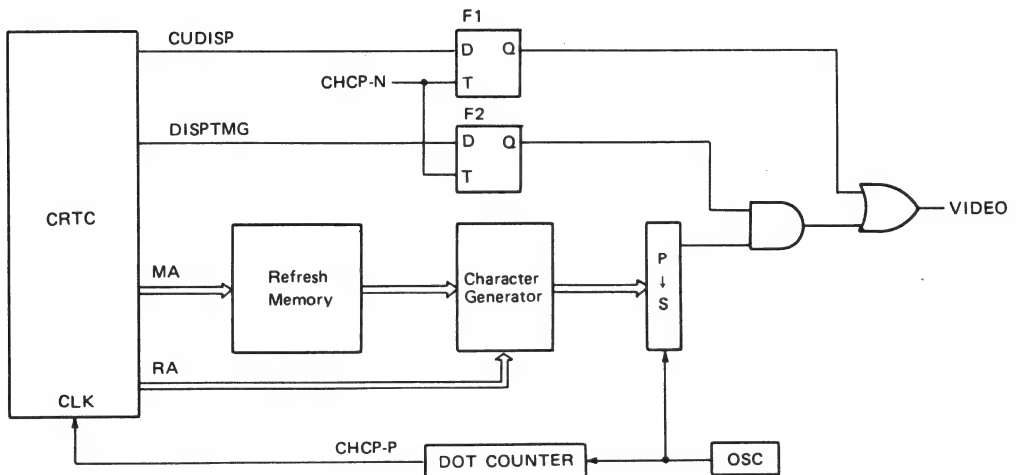


Figure 21 Display Control Unit (1)

When many characters are displayed in horizontal direction on the screen, and horizontal one-character time is so short that both refresh memory and Character Generator cannot be accessed, the circuitry shown in Fig. 22 should be used. In this case refresh memory output shall be latched and Character Generator shall be accessed at the next cycle. The time chart in this case is shown in Fig. 25. CUDISP and DISPTMG should be provided after being delayed by one-character time by using skew bit of interlace & skew register (R8). Moreover, when there are some

troubles about delay time of MA during horizontal one-character time on high-speed display operation, system shown in Fig. 23 is adopted. The time chart in this case is shown in Fig. 26. Character video signal is delayed for two-character time because each MA outputs and refresh memory outputs are latched, and they are made to be in phase with CUDISP and DISPTMG by delaying for two-character time. Table 10 shows the circuitry selection standard of display units.

Table 10 Circuitry Standard of Display Control Unit

Case	Relation among t_{CH} Refresh Memory and Character Generator	Block Diagram	Interlace & Skew Register Bit Programming			
			C1	C0	D1	D0
1	$t_{CH} > \text{RM Access} + \text{CG Access} + t_{MAD}$	Fig. 21	0	0	0	0
2	$\text{RM Access} + \text{CG Access} + t_{MAD} \geq t_{CH} > \text{RM Access} + t_{MAD}$	Fig. 22	0	1	0	1
3	$\text{RM Access} + t_{MAD} \geq t_{CH} > \text{RM Access}$	Fig. 23	1	0	1	0

t_{CH} : CHCP Period; t_{MAD} : MA Delay

RM: Refresh Memory CG: Character Generator

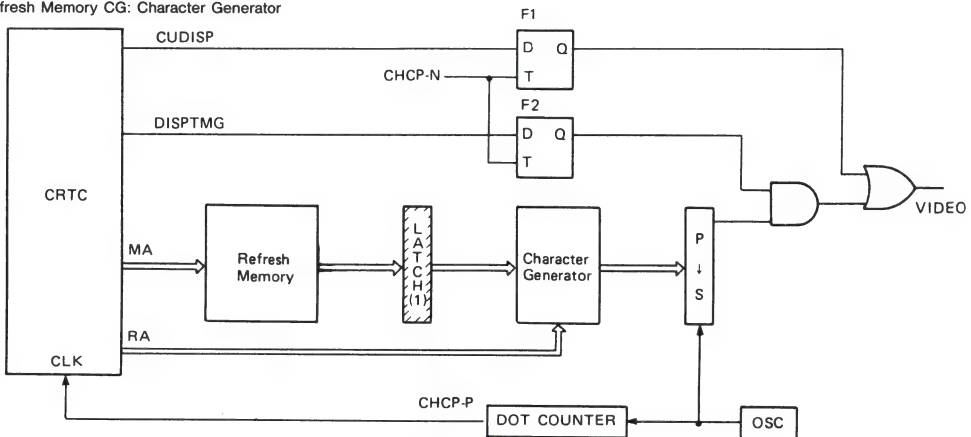


Figure 22 Display Control Unit(2)

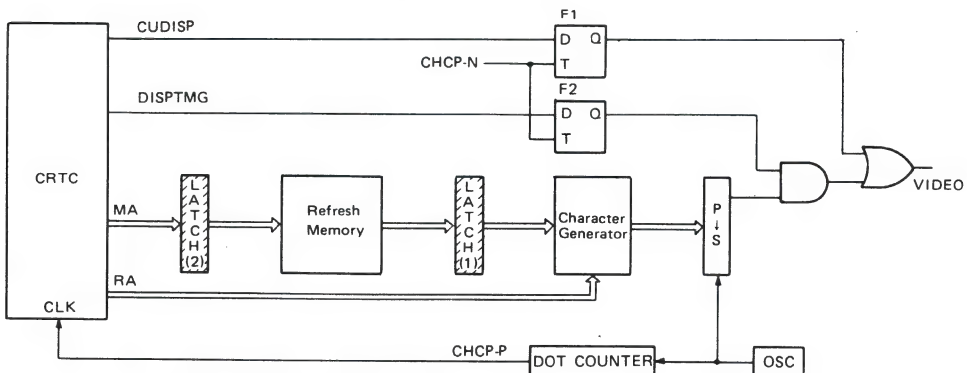


Figure 23 Display Control Unit (For high-speed display operation) (3)

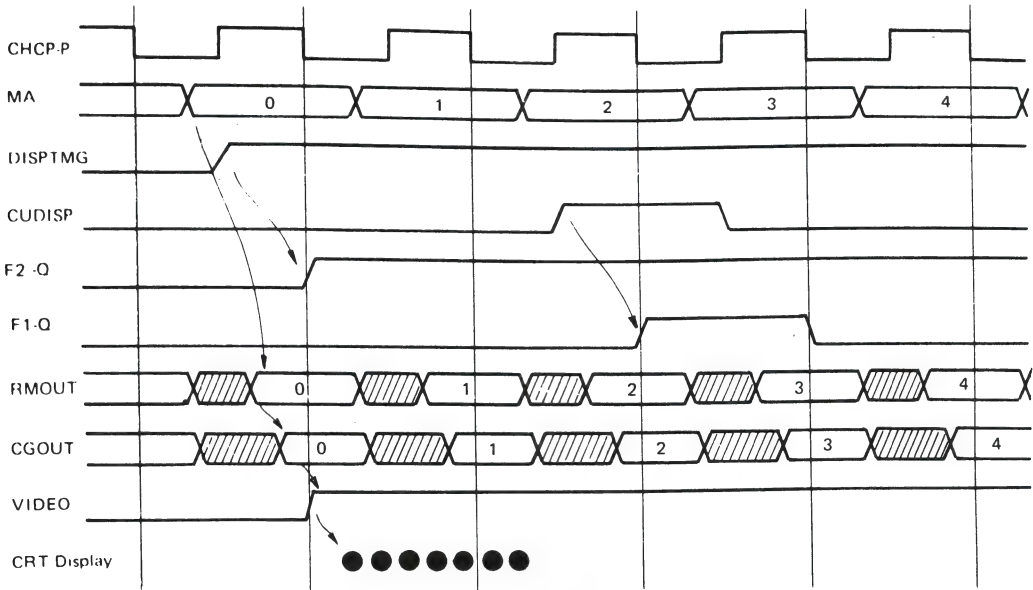


Figure 24 Time Chart of Display Control Unit (1)

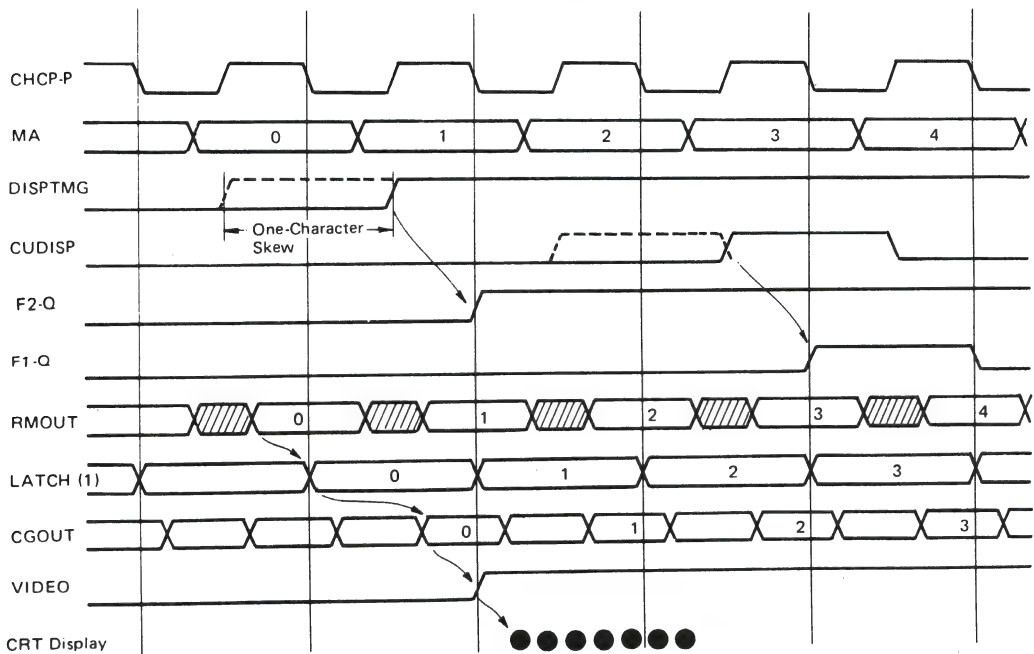


Figure 25 Time Chart of Display Control Unit (2)

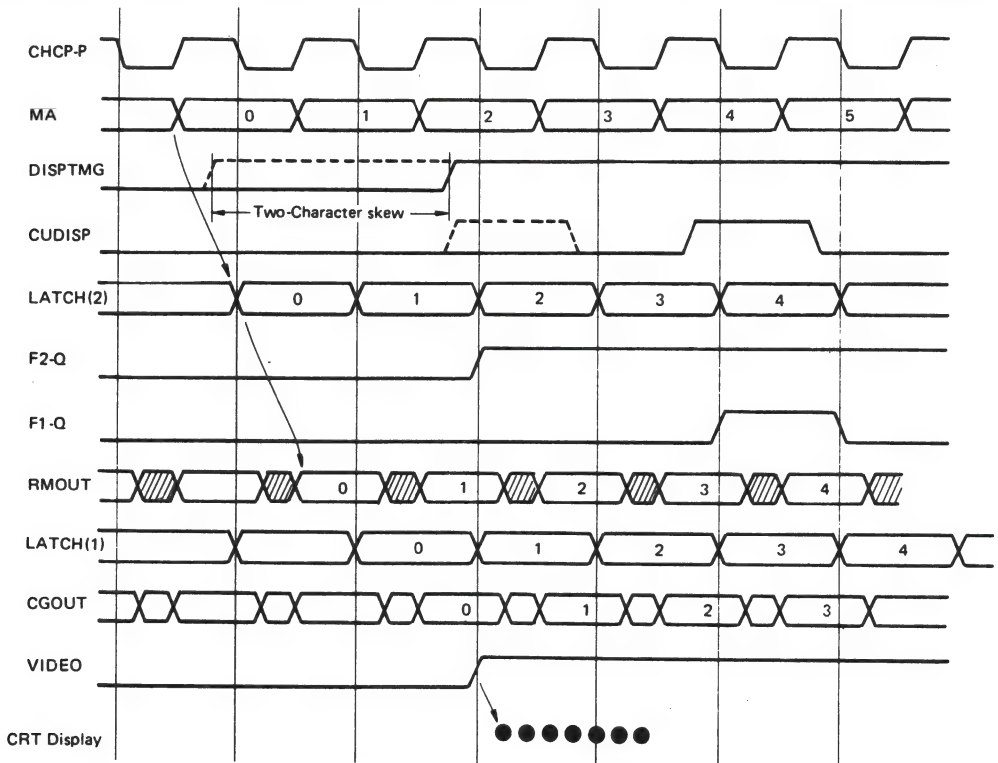


Figure 26 Time Chart of Display Unit (3)

■ HOW TO DECIDE PARAMETERS SET ON THE CRTC

• How to Decide Parameters Based on Specification of CRT Display Unit (Monitor)

Horizontal deflection frequency f_h is given by specification of CRT display unit. Number of horizontal total characters is determined by the following equation.

$$f_h = \frac{1}{t_c(Nht+1)}$$

where,

t_c : Cycle Time of CLK (Character Clock)

Nht: Programmed Value of Horizontal Total Register (R0)

Number of Vertical Total Characters

Vertical deflection frequency is given by specification of CRT display unit. Number of vertical Total characters is determined by the following equation.

1) Non-interlace Mode

$$Rt = (Nvt+1)(Nr+1) + Nadj$$

2) Interlace Sync Mode

$$Rt = (Nvt+1)(Nr+1) + Nadj + 0.5$$

3) Interlace Sync & Video Mode

$$Rt = \frac{(Nvt+1)(Nr+2) + 2Nadj}{2} \quad (a)$$

$$Rt = \frac{(Nvt+1)(Nr+2) + 2Nadj + 1}{2} \quad (b)$$

(a) is applied when both total numbers of vertical characters (Nvt+1) and that of rasters in line (Nr+2) are odd.

(b) is applied when total number of rasters (Nr+2) is even, or when (Nr+2) is odd and total number of vertical characters (Nvt+1) is even.

where,

Rt : Number of Total Rasters per frame
(Including retrace period)

Nvt : Programmed Value of Vertical Total Register (R4)

Nr : Programmed Value of Maximum Raster Address Register (R9)

Nadj : Programmed Value of Vertical Total Adjust Register (R5)

Horizontal Sync Pulse Width

Horizontal sync pulse width is programmed to low order 4-bit of horizontal sync width register (R3) in unit of horizontal character time. Programmed value can be selected within from 1 to -15.

Horizontal Sync Position

As shown in Fig. 27, horizontal sync position is normally selected to be in the middle of horizontal retrace period. But there are some cases where its optimum sync position is not located in the middle of horizontal retrace period according to specification of CRT. Therefore, horizontal sync position should be determined by specification of CRT. Horizontal sync pulse position is programmed in unit of horizontal character time.

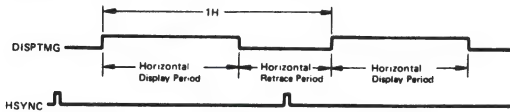


Figure 27 Time Chart of HSYNC

Vertical Sync Pulse Width

Vertical Sync Pulse Width is programmed to high order 4-bit of vertical sync pulse width register (R3) in unit of

raster period. Programmed value can be selected within from 1 to 16.

Vertical Sync Position

As shown in Fig. 28, vertical sync position is normally selected to be in the middle of vertical retrace period. But there are some cases where its optimum sync position is not located in the middle of vertical retrace period according to specification of CRT. Therefore, vertical sync position should be determined by specification of CRT. Vertical sync pulse position is programmed to vertical sync position register (R7) in unit of line period.

• How to Decide Parameters Based on Screen Format Dot Number of Characters (Horizontal)

Dot number of characters (horizontal) is determined by character font and character space. An example is shown in Fig. 29. More strictly, dot number of characters (horizontal) N is determined by external N-counter. Character space is set by means shown in Fig. 30.

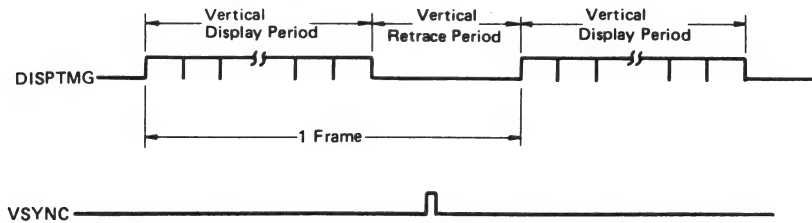


Figure 28 Time Chart of VSYNC

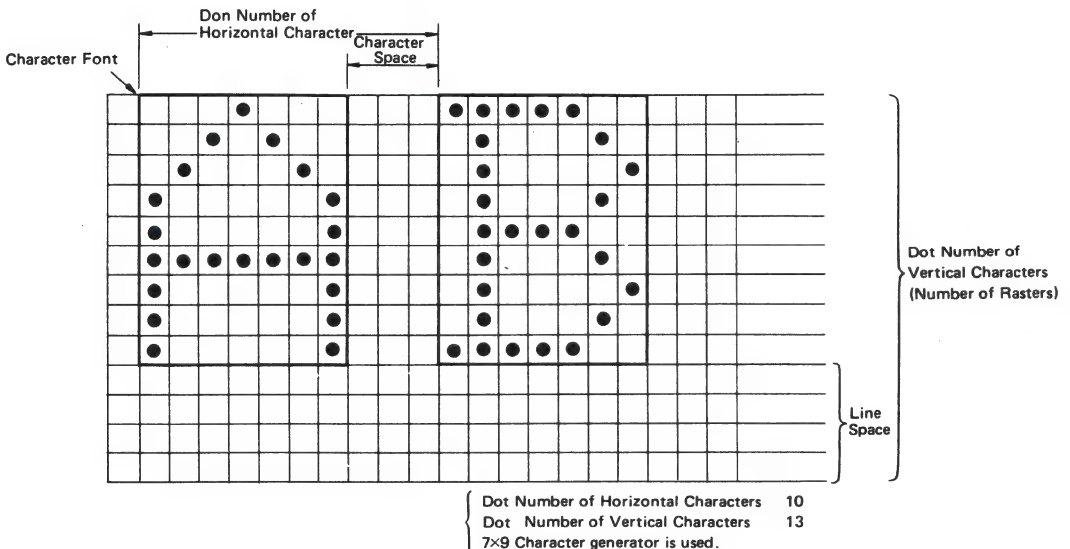


Figure 29 Dot Number of Horizontal and Vertical

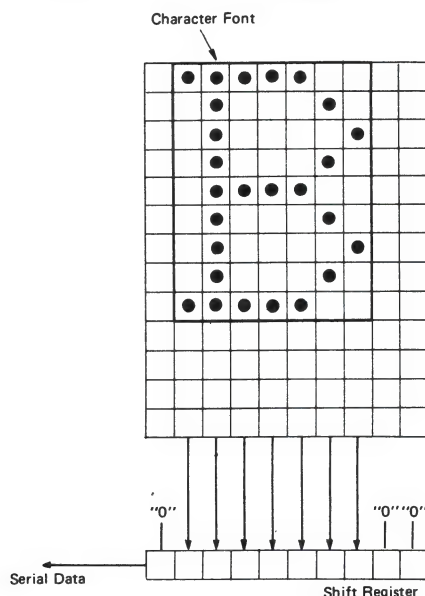


Figure 30 How to Make Character Space

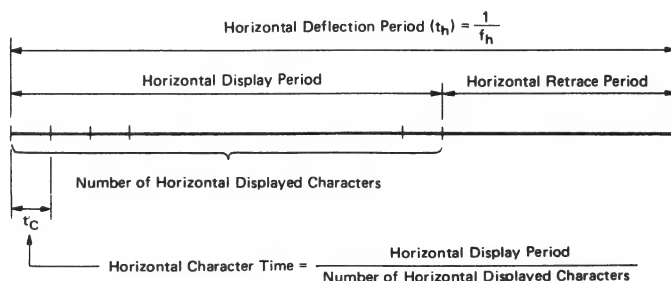


Figure 31 Number of Horizontal Displayed Characters

Dot Number of Characters (Vertical)

Dot number of characters (vertical) is determined by characters font and line space. An example is shown in Fig. 29. Dot number of characters (vertical) is programmed to maximum raster address (R9) of CRT.

Number of Horizontal Displayed Characters

Number of horizontal displayed characters is programmed to horizontal displayed register (R1) of the CRT. Programmed value is based on screen format. Horizontal display period, which is given by specification of horizontal deflection frequency and horizontal retrace period of CRT display unit, determines horizontal character time, being divided by number of horizontal displayed characters. Moreover, its cycle time and access time which are necessary for CRT display system are determined by horizontal character time.

Number of Vertical Displayed Characters

Number of vertical displayed characters is programmed to vertical displayed register (R6). Programmed value is based on screen format. As specification of vertical deflection frequency of CRT determines number of total rasters (R_t) including vertical retrace period and the relation between number of vertical displayed character and total number of rasters on a screen is as mentioned above, CRT which is suitable for desired screen format should be selected.

For optimum screen format, it is necessary to adjust number of rasters per line, number of vertical displayed characters, and total adjust raster (Nadj) within specification of vertical deflection frequency.

Scan Mode

The CRTC can program three-scan modes shown in Table 11 to interlace mode register (R8). An example of character display in each scan mode is shown in Fig. 8.

Table 11. Program of Scan Mode

V	S	Scan Mode	Main Usage
0	0	Non-interlace	Normal Display of Characters & Figures
1	0		
0	1	Interlace Sync	Fine Display of Characters & Figures
1	1	Interlace Sync & Video	Display of Many Characters & Figures Without Using High-resolution CRT

(NOTE) In the interlace mode, the number of times per sec. in raster scanning on one spot on the screen is half as many as that in non-interlace mode. Therefore, when persistence of luminescence is short, flickering may happen. It is necessary to select optimum scan mode for the system, taking characteristics of CRT, raster scan speed, and number of displayed characters and figures into account.

Cursor Display Method

Cursor start raster register and cursor end raster register (R10, R11) enable programming the display modes shown in Table 7 and display patterns shown in Fig. 9. Therefore, it is possible to change the method of cursor display dynamically according to the system conditions as well as to realize the cursor display that meets the system requirements.

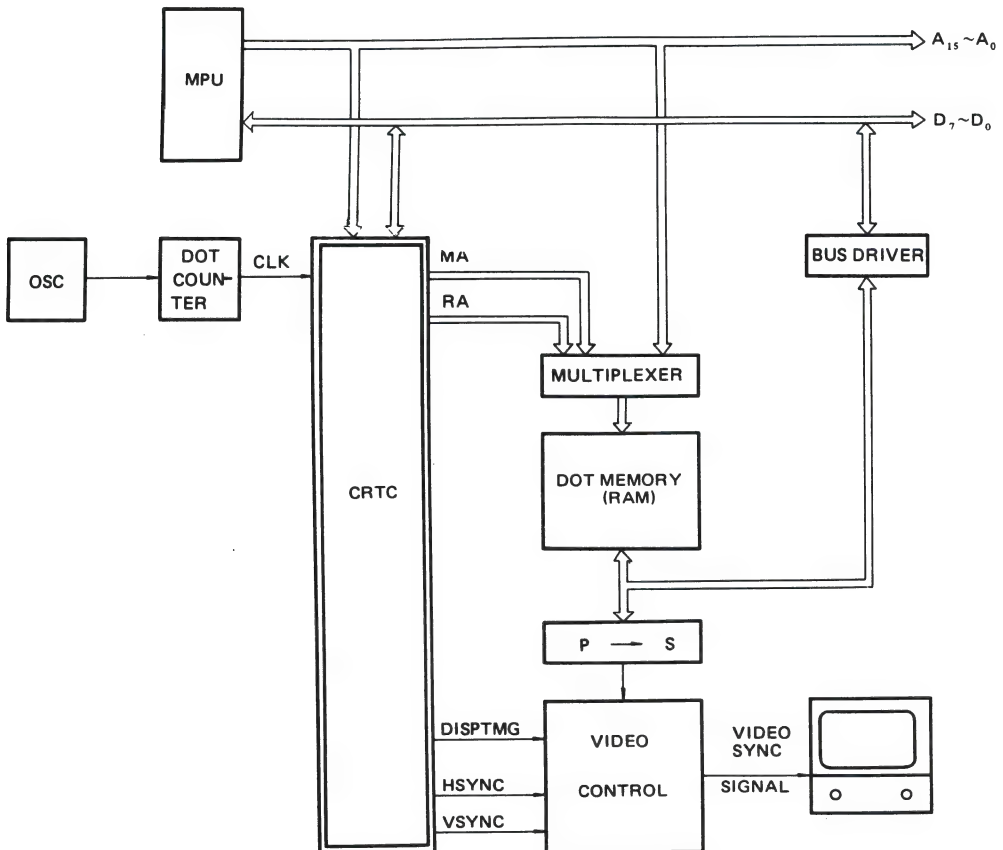


Figure 32 Monochrome Character Display

Start Address

Start address registers (R12, R13) give an offset to the address of refresh memory to read out. This enables paging and scrolling easily.

Cursor Register

Cursor registers (R14, R15) enable programming the cursor display position on the screen. As for cursor address, it is not X, Y address but linear address that is programmed.

APPLICATIONS OF THE CRTC

• Monochrome Character Display

Fig. 32 shows a system of monochrome character display. Character clock signal (CLK) is provided to the CRTC through OSC and dot counter. It is used as basic clock which drives internal control circuits. MPU is connected with the CRTC by standard bus and controls the CRTC initialization and read/write of internal registers.

Refresh memory is composed of RAM which has capacity of one frame at least and the data to be displayed is coded and stored. The data to refresh memory is changed through MPU bus, while refresh memory is read out successively by the CRTC to display a static pattern on the screen. Refresh memory is accessed by both MPU and

the CRTC, so it needs to change its address selectively by multiplexer. The CRTC has 14 MA (Memory Address output), but in fact some of them that are needed are used according to capacity of refresh memory.

Code output of refresh memory is provided to character generator. Character generator generates a dot pattern of a specified raster of a specified character in parallel according to code output from refresh memory and RA (Raster Address output) from the CRTC. Parallel-serial converter is normally composed of shift register to convert output of character generator into a serial dot pattern. Moreover, DISPTMG, CUDISP, HSYNC, and VSYNC are provided to video control circuit. It controls blanking for output of parallel-serial converter, mixes these signals with cursor video signal, and generates sync signals for an interface to monitor.

• Color Character Display

Fig. 33 shows a system of color character display. In this example, a 3-bit color control bit (R, G, B) is added to refresh memory in parallel with character code and provided to video control circuit. Video control circuit controls coloring as well as blanking and provides three primary color video signals (R, G, B signals) to CRT display device to display characters in seven kinds of color on the screen.

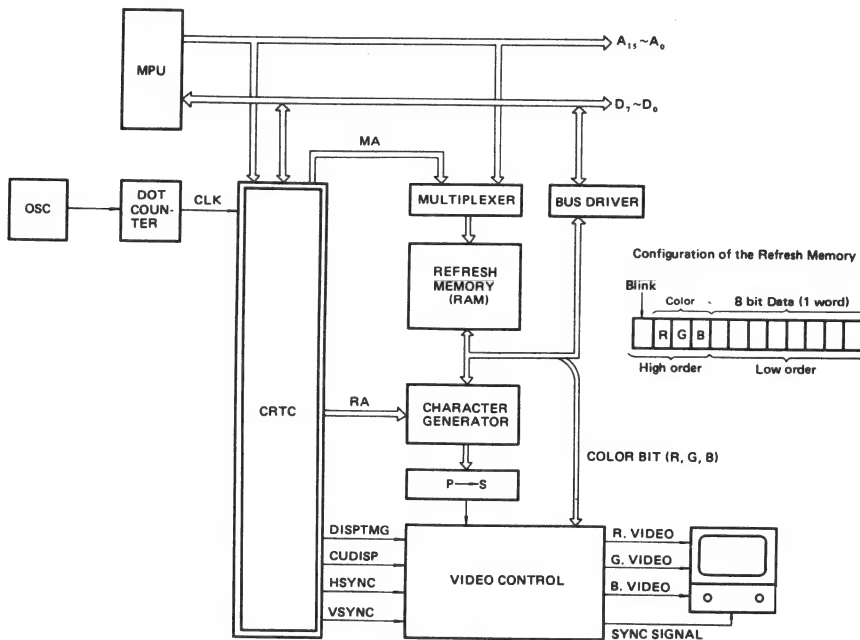


Figure 33 Color Character Display

• Color limited Graphic Display

Limited graphic display is to display simple figures as well as character display by combination of picture element which are defined in unit of one character.

As shown in Fig. 34, graphic pattern generator is set up in parallel with character generator and output of these generators are wire-ORed. Which generator is accessed

depends on coded output of refresh memory.

In this example, graphic pattern generator adopts ROM, so only the combination of picture elements which are programmed to it is used for this graphic display system. Adopting RAM instead of ROM enables dynamically writable symbols in any combination on one display by changing the contents of them.

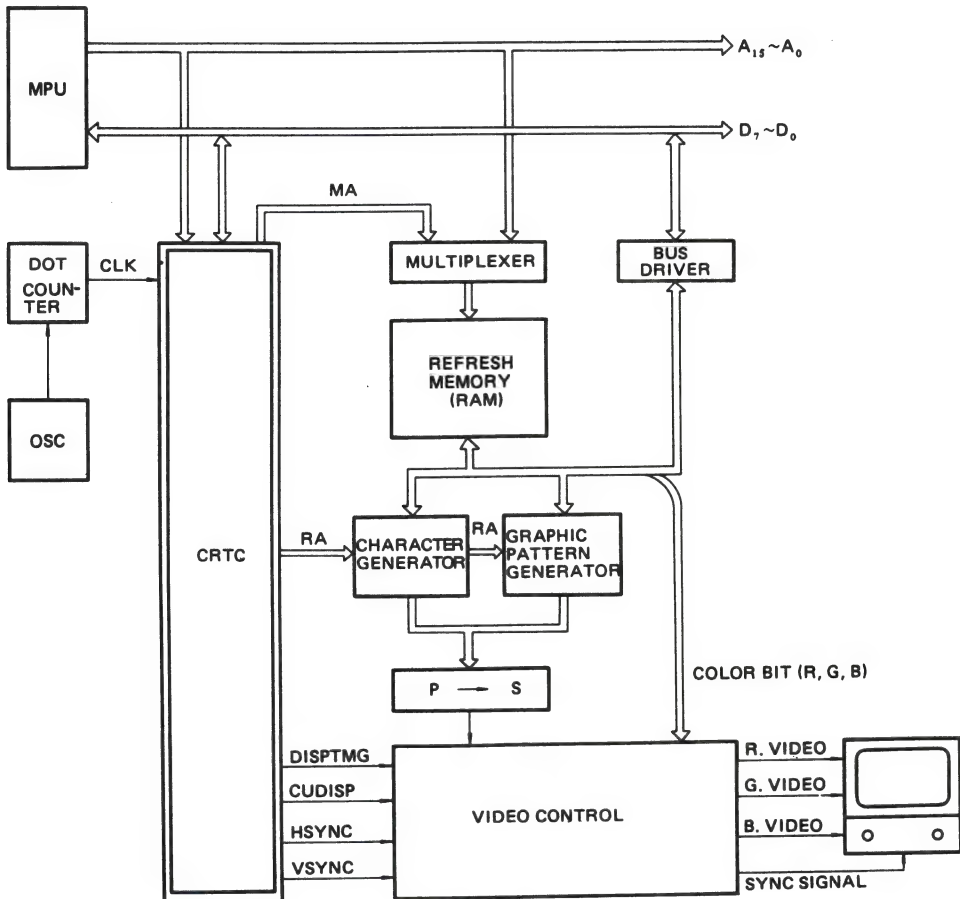


Figure 34 Color Limited Graphic Display

• Monochrome Full Graphic Display

Fig. 35 shows a system of monochrome full graphic display. While simple graphic display is figure display by combination of picture elements in unit of 1 picture elements, full graphic display is display of any figures in

unit of 1 dot. In this case, refresh memory is dot memory that stores all the dot patterns, so its output is directly provided to parallel-serial converter to be displayed. Dot memory address to refresh the screen is set up by combination of MA and RA of CRTC.

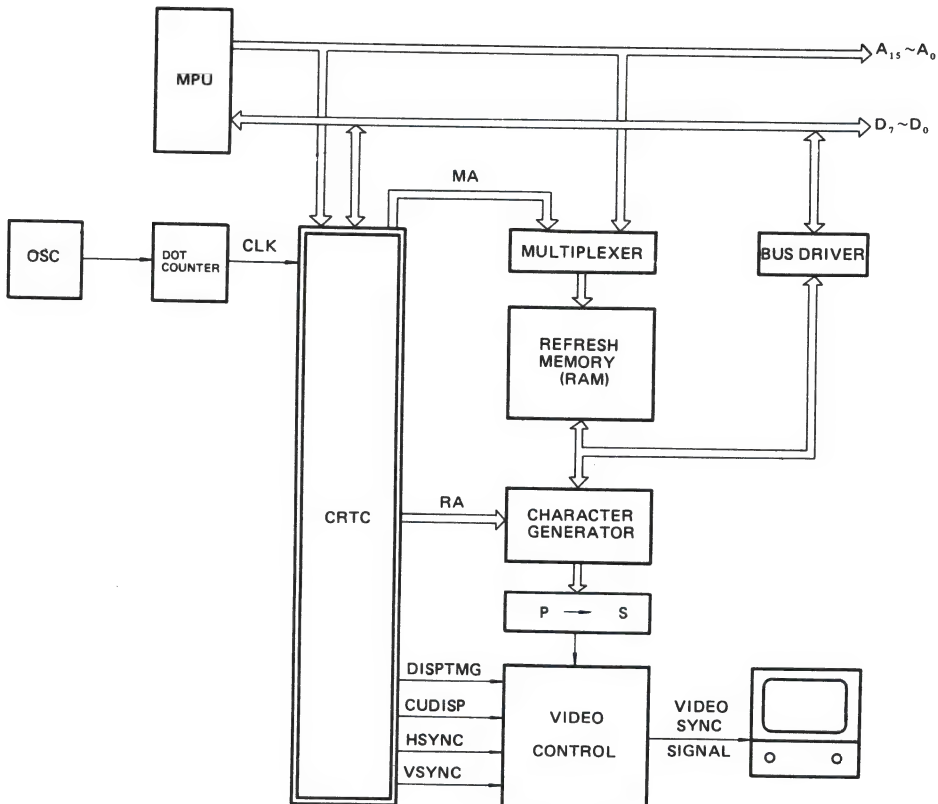


Figure 35 Monochrome Full Graphic Display

Fig. 36 shows an example of access to refresh memory by combination of MA and RA. Fig. 36 shows a refresh memory address method for full graphic display. Cor-

respondence between dot on the CRT screen and refresh memory address is shown in Fig. 37.

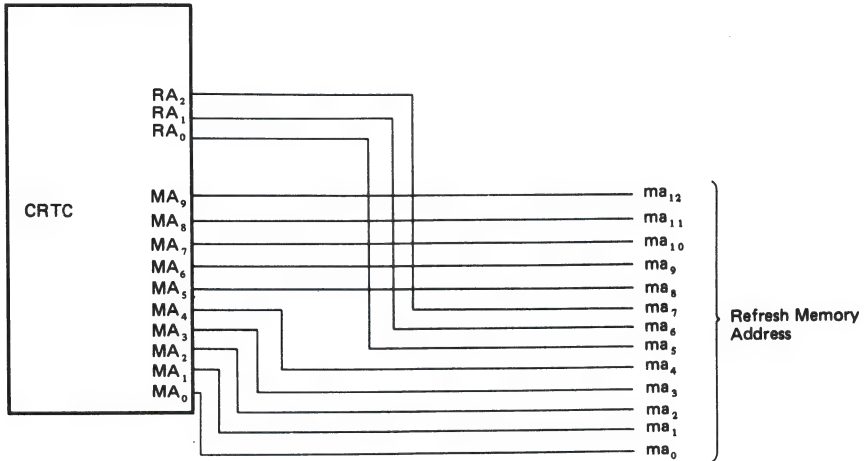


Figure 36 Refresh Memory Address Method for Full Graphic Display

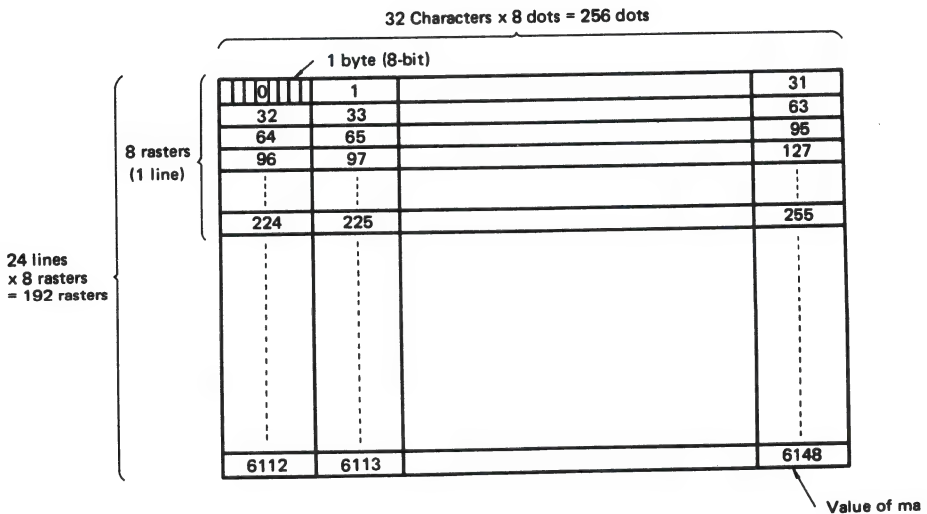


Figure 37 Memory Address and Dot Display Position on the Screen for Full Graphic Display

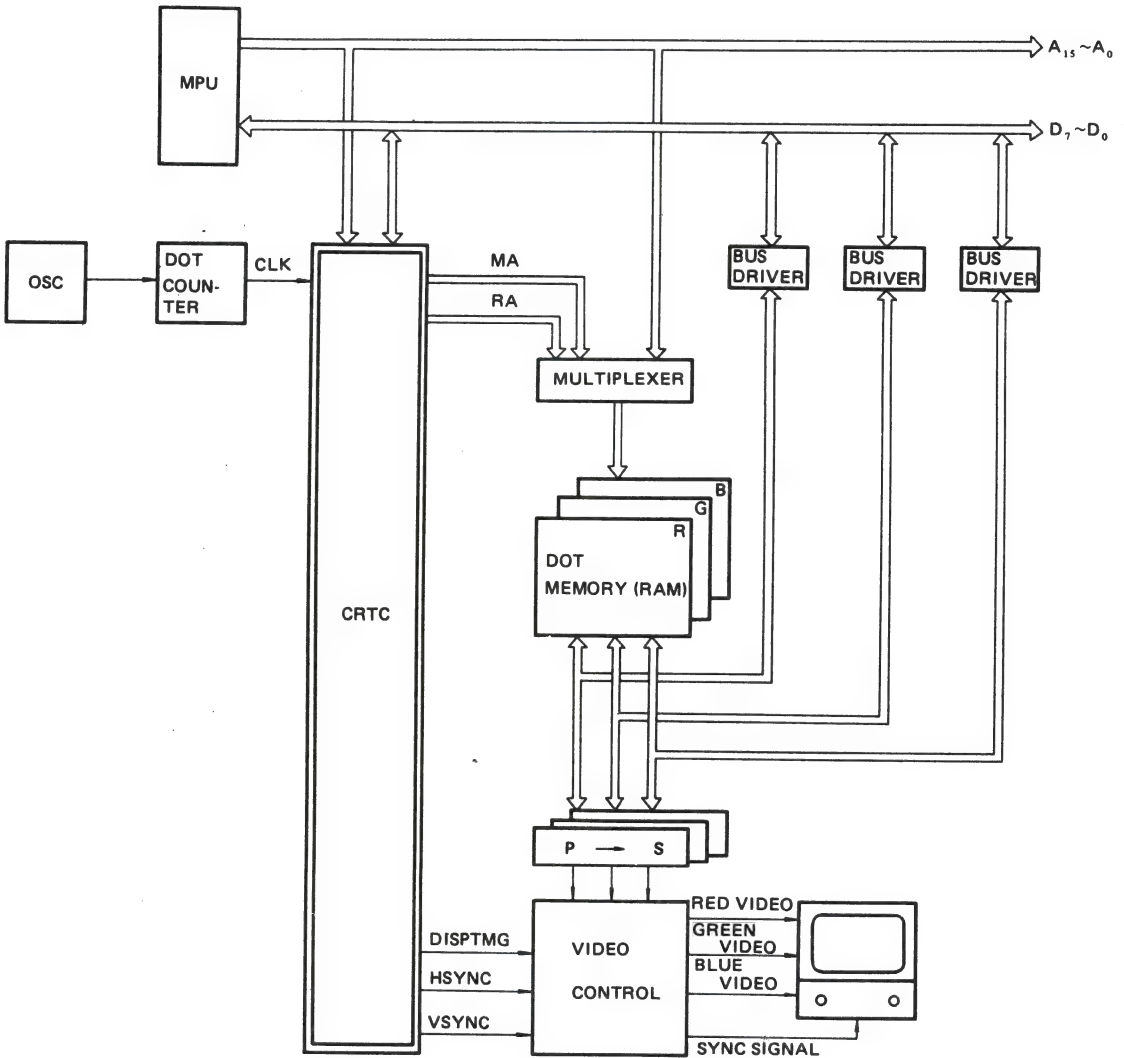


Figure 38. Color Full Graphic Display

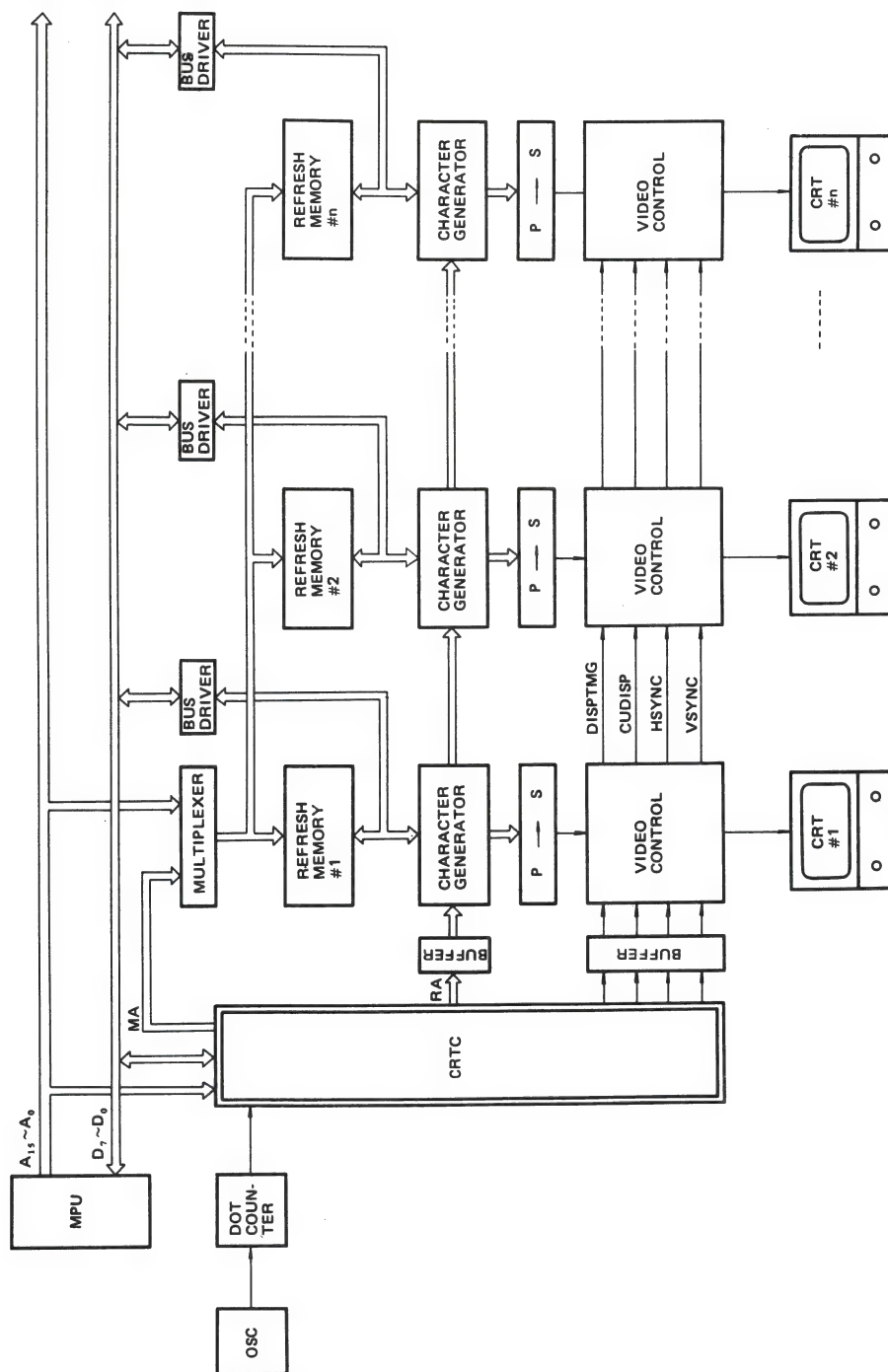


Figure 39. Cluster control by the CRTC

■ DISPLAY SEQUENCE AFTER $\overline{\text{RES}}$ RELEASE OF GM68B45S

GM68B45S starts the display operation immediately after the release of $\overline{\text{RES}}$. The operation at the first is different from the normal subsequent display operation.

[Operation at the first field after the $\overline{\text{RES}}$ release]

- (1) DISPTMG and CUDISP are not output. (They remain at "Low" level. The display is inhibited.)
- (2) The data programmed in the start address register is not used. (MA and RA start at "0".)
- (3) The sequences are shown in the following figures.

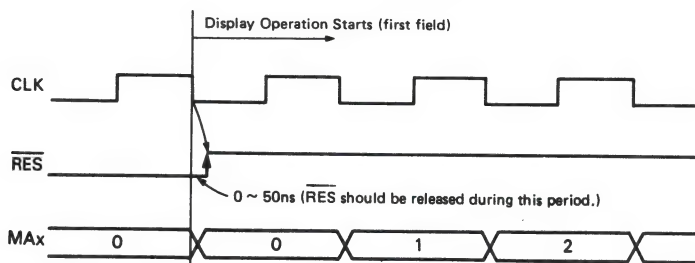


Figure 40 $\overline{\text{RES}}$ Release Sequence

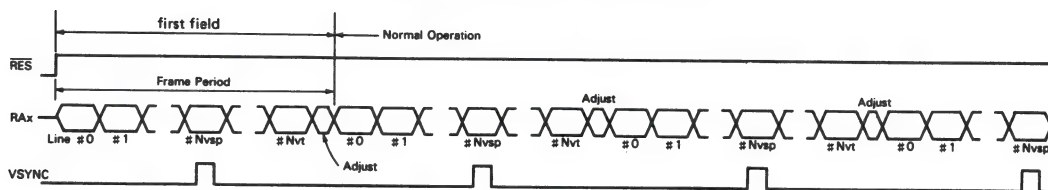


Figure 41 $\overline{\text{RES}}$ Release Sequence in The Non-interlace Mode

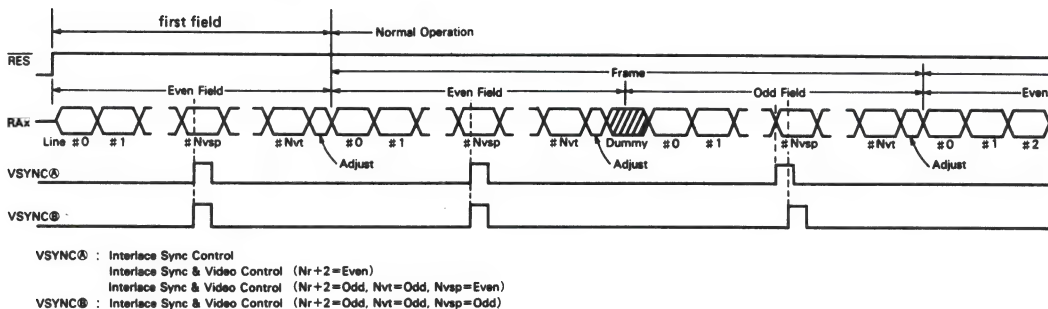


Figure 42 $\overline{\text{RES}}$ Release Sequence in The Interlace Mode (1)

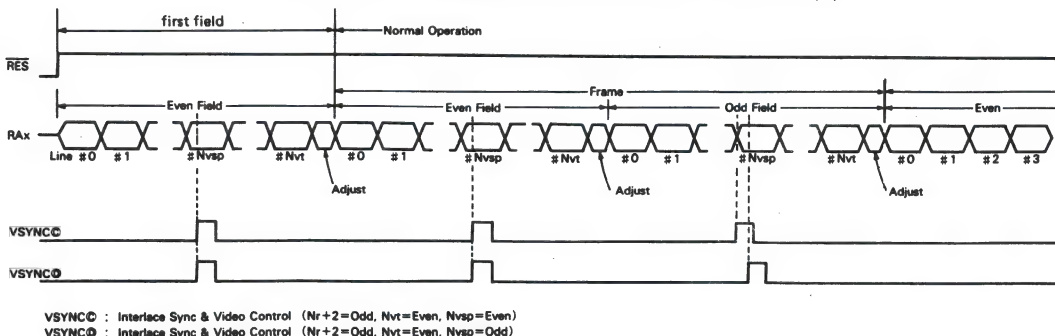


Figure 43 $\overline{\text{RES}}$ Release Sequence in The Interlace Mode (2)

■ ANOMALOUS OPERATIONS IN GM6845S CAUSED BY REWRITING REGISTERS DURING THE DISPLAY OPERATION*

Register #	Register Name	Anomalous operations caused by rewriting registers & Conditions to avoid those operations [△]	Rewriting** OK or NG
R0	Horizontal Total	The horizontal scan period is disturbed.	X
R1	Horizontal Displayed	There are some cases where the width of DISPTMG becomes shorter than the programmed value at the moment of a rewrite operation. An error operation occurs only during one raster period.	O
R2	Horizontal Sync Position	There are some cases where HSYNC is placed on the position different from the programmed value or the noise is output.	X
R3	Sync Width	When a rewrite operation is performed at a "High" level on HSYNC pulse or VSYNC pulse, there are some cases where the width pulse becomes shorter than the programmed value at the moment of a rewrite operation.	△
R4	Vertical Total	When a rewrite operation is performed during the last raster period in the line, there is a possibility that the disturbance occurs during the vertical scan period. There is no problem of a rewrite operation during raster period except this period.	△
R5	Vertical Total Adjust	When a rewrite operation is performed in the last character time of the raster period, there are some cases where the numbers of Adjust Raster, specified by program, are not added. (Only during the adjust raster period)	△
R6	Vertical Displayed	After the moment of a rewrite operation, there are some cases where the Display is inhibited. However, the display according to the programmed value is performed from the next field.	O
R7	Vertical Sync Position	There are cases where VSYNC is placed on the position different from the programmed value or the noise is output.	X
R8	Interlace & Skew	Neither scan mode bit nor skew bit is rewritten dynamically. Dynamic Rewrite into scan mode bit and skew bit is prohibited.	X
R9	Maximum Raster Address	The internal operation will be disordered by a rewrite operation.	X
R10	Cursor Star Raster	When a rewrite operation is performed in the last character time of the raster period, there are some cases where the litter occurs on the cursor raster or the cursorn is not displayed correctly. There is also a possibility that the blink rate becomes temporally shorter than usual.	△
R11	Cursor End Raster	When a rewrite operation is performed in the last character time of the raster period, there are some cases where the litter occurs on the cursor raster or the cursor is not displayed correctly. Moreover, there are also some cases where the blink rate becomes temporally shorter than normal operation.	△
R12	Start Address (H)	R12 and R13 are used in the last raster period of the field. A rewrite be performed except during this period. However, when R12 and R13 are rewritten in each field separately, the display operatio, whose start address is determined temporally by programming sequence, will be performed. A rewrite operation should be performed during the horizontal/vertical display period.	O
R13	Start Address (L)		O
R14	Cursor (H)	When a rewrite operation is performed during the display period, there are some cases where the cursor is temporally displayed at the address different from the programmed value. A rewrite operation should be performed during the horizontal/vertical retrace period. Also, when R14 and R15 are rewritten in each field separately, the cursor is displayed temporally at the temporal address determined by programming sequence.	O
R15	Cursor (L)		O

* means temporary abnormal operations in rewriting the internal register during the display operation. Normally, after a rewrite operation the LSI performs the specified display operation from the next field.

(The operations in this table are outside our guarantee and are regarded as materials for reference.)

O A rewrite operation is possible without affecting the screen in the display so much.

** △ If conditions are satisfied, a rewrite operation is possible. If conditions are not satisfied, there are some cases where a flicker and so on occur temporally.

X When a rewrite operation is performed, there are some cases where a flicker and so on occur temporally.

GD75188

QUADRUPLE LINE DRIVERS

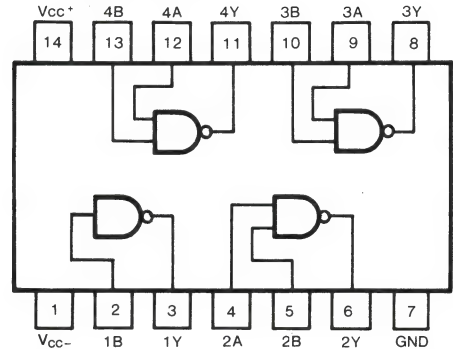
Feature

- Meets Specifications of EIA RS-232C
- Designed to be Interchangeable with SN75188
- Current Limited Output .. 10mA Typical
- Power-Off Output Impedance ... 300Ω Min
- Slew Rate Control by Load Capacitor
- Flexible Supply Voltage Range
- Input Compatible with Most TTL and DTL Circuits

Description

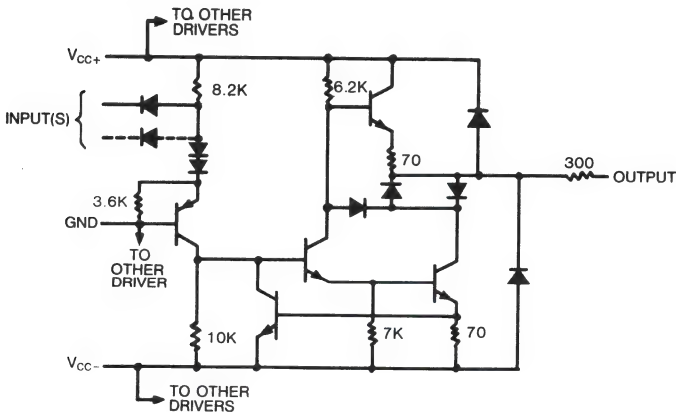
The GD75188 is a monolithic quadruple line driver designed to interface data terminal equipment with data communication equipment in conformance with the specifications of EIA standard RS-232C with a diode in series with each supply-voltage terminal as shown under typical applications. The device is characterized for operation from 0°C to 75°C

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package

Schematic (each driver)



Function Table

A	B	Y
H	H	L
L	X	H
X	L	H

Absolute Maximum Ratings

• Supply voltage	V_{CC+}	15V
• Supply voltage	V_{CC-}	-15V
• Input voltage range	V_I	-15V~+7V
• Output voltage range	V_O	-15V~+15V
• Continuous total dissipation at (or below) 25°C	P_T	1W
• Operating free-air temperature range	T_A	0~+75°C
• Storage temperature range	T_{STG}	-65~+175°C
• Lead temperature 1/16 inch from case for 60 seconds, P Package		300°C
seconds, J Package		260°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			1.9			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	$V_{IL}=0.8V$ $R_L=3k\Omega$	$V_{CC+}=9V$, $V_{CC-}=-9V$	6	7		V
			$V_{CC+}=13.2V$ $V_{CC-}=-13.2V$	9	10.5		
V_{OL}	Low-level output voltage	$V_{IH}=1.9V$ $R_L=3k\Omega$	$V_{CC+}=9V$ $V_{CC-}=-9V$		-7	-6	V
			$V_{CC+}=13.2V$ $V_{CC-}=-13.2V$		-10.5	-9	
I_{IH}	High-level input current	$V_I=5V$				10	μA
I_{IL}	Low-level input current	$V_I=0$			-1	-1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level■	$V_I=0.8V$	$V_O=0$	-6	-10	-12	mA
$I_{OS(L)}$	Short-circuit output current at low level■	$V_I=1.9V$	$V_O=0$	6	10	12	mA
r_o	Output resistance, power off	$V_{CC+}=0$ $V_O=-2V$ to 2V	$V_{CC-}=0$	300			Ω
I_{CC+}	Supply current from V_{CC+}	$V_{CC+}=9V$, No load	All inputs at 1.9V		15	20	mA
			All inputs at 0.8V		4.5	6	
		$V_{CC+}=12V$ No load	All inputs at 1.9V		19	25	
			All inputs at 0.8V		5.5	7	
		$V_{CC+}=15V$, No load, $T_A=25^\circ C$	All inputs at 1.9V			34	
			All inputs at 0.8V			12	
I_{CC-}	Supply current from V_{CC-}	$V_{CC-}=-9V$, No load	All inputs at 1.9V	-13	-17		mA
			All inputs at 0.8V		-0.015		
		$V_{CC-}=-12V$, No load	All inputs at 1.9V	-18	-23		
			All inputs at 0.8V		-0.015		
		$V_{CC-}=-15V$, No load, $T_A=25^\circ C$	All inputs at 1.9V			-34	
			All inputs at 0.8V			-2.5	
P_D	Total power dissipation	$V_{CC+}=9V$, No load	$V_{CC-}=-9V$			333	mW
		$V_{CC+}=12V$, No load	$V_{CC-}=-12V$			576	

□ All typical values are at $T_A=25^\circ C$

■ Not more than one output should be shorted at a time.

NOTE: The algebraic convention where the more positive (less negative) limit is designated as maximum is used in this data sheet for logic voltage levels only, e.g., if -6V is a maximum, the typical value is a more negative voltage.

Switching Characteristics, $V_{CC+}=9V$, $V_{CC-}=-9V$, $T_A=25^\circ C$

PARAMETER	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		220	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$R_L=3k\Omega$,	100	175	ns
t_{TLH}	Transition time, low-to-high-level output‡	See Figure 1	55	100	ns
t_{THL}	Transition time, high-to-low-level output‡	$C_L=15pF$	45	75	ns
t_{TLH}	Transition time, low-to-high-level outputs§	$R_L=3k\Omega$ to $7k\Omega$,	2.5		μs
t_{THL}	Transition time, high-to-low-level outputs§	See Figure 1	3.0		μs

‡ Measured between 10% and 90% points of output waveform.

§ Measured between +3V and -3V points on the output waveform (EIA RS-232C conditions)

Parameter Measurement Information

NOTE: A. The pulse generator has the following characteristics; $t_w = 0.5\mu s$, $PRR = 1\text{ MHz}$, $Z_0 = 50\Omega$
 B. C_i includes probe and jig capacitance.

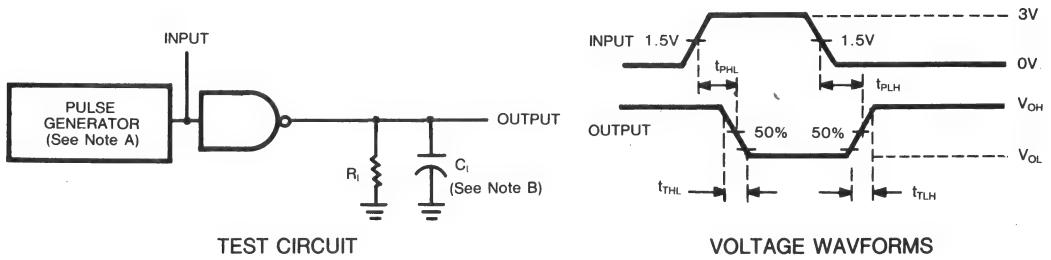


Figure 1. Propagation and Transition Times

Thermal Information

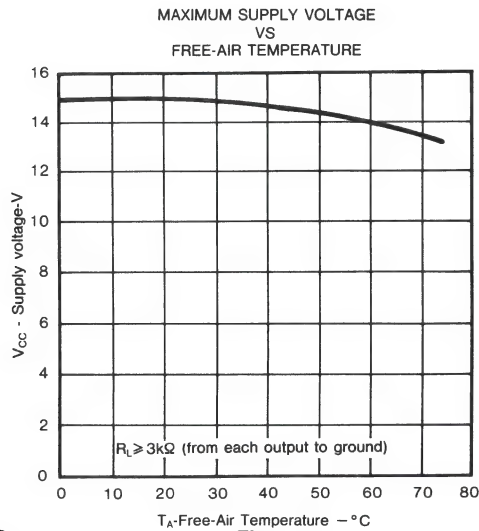


Figure 2.

Typical Application Data

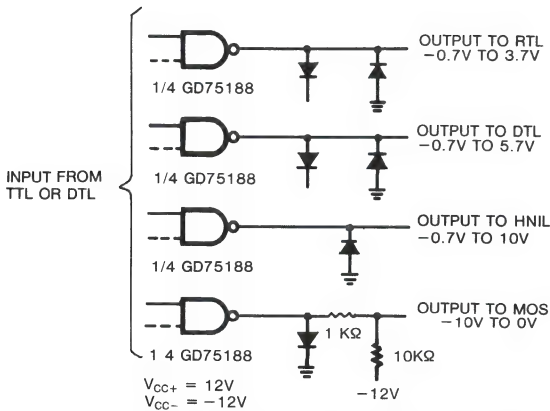


Figure 3 - Logic Translator Applications

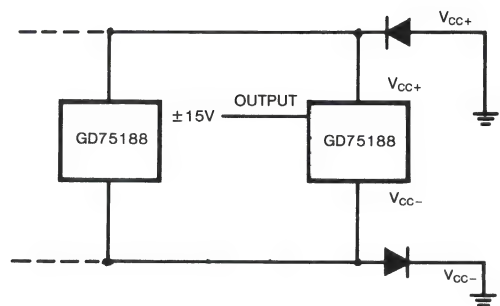


Figure 4 - Power Supply Protection to Meet Power-Off Fault Conditions of Eia Standard RS-232C

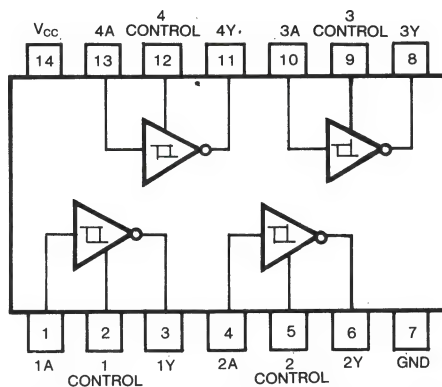
GD75189/A

QUADRUPLE LINE RECEIVERS

Feature

- Input Resistance ... $3k\Omega$ to $7k\Omega$
- Input Signal Range ... $\pm 30V$
- Fully Interchangeable with SN/75189A
- Operates from Single 5-V Supply
- Built-In Input Hysteresis (Double Thresholds)
- Response Control Provides: Input Threshold Shifting
Input Noise Filtering
- Satisfies Requirements of EIA RS-232-C

Pin Configuration

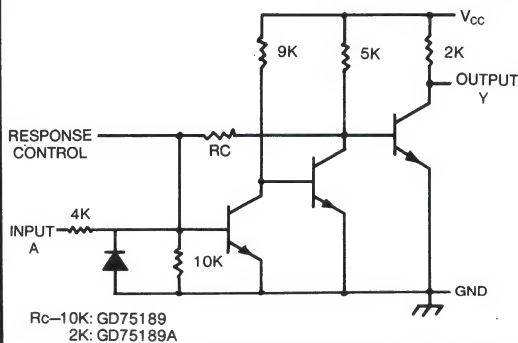


Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Description

The GD75189/A is monolithic quadruple line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA standard RS-232C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage can be connected between this terminal and ground to shift the input threshold voltage levels. An external capacitor can be connected from this terminal to ground to provide input noise filtering.

Schematics (each gate)



Absolute Maximum Ratings

• Supply voltage	V_{CC}	10V
• Input voltage	V_I	$\pm 30V$
• Output current	V_O	20 mA
• Continuous total dissipation at (or below) 25°C	P_T	1 W
• Operating free-air temperature range	T_A	0~ 175 °C
• Storage temperature range	T_{STG}	-65~+175°C
• Lead temperature 1/16 inch from case for 60 seconds, J Package		300 °C
• Lead temperature 1/16 inch from case for 10 seconds, P Package		260 °C

Electrical Characteristics over recommended operating free-air temperature range (): GD75189A

SYM BOL	PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage	1		1(1.75)	(1.9)	1.5(2.25)	V
V_{T-}	Negative-going threshold voltage	1		0.75	0.97	1.25	V
V_{OH}	High-level output voltage	1	$V_I=0.75V, I_{OH}=-0.5mA$	2.6	4	5	V
			Input open, $I_{OH}=-0.5mA$	2.6	4	5	
V_{OL}	Low-level output voltage	1	$V_I=3V, I_{OL}=10mA$	0.2	0.45		V
I_{IH}	High-level input current	2	$V_I=25V$	3.6		8.3	mA
			$V_I=3V$	0.43			
I_{IL}	Low-level input current	2	$V_I=-25V$	-3.6		-8.3	mA
			$V_I=-3V$	-0.43			
I_{OS}	Short-circuit output current	3		-3			mA
I_{CC}	Supply current	2	$V_I=5V$, Outputs open	20		26	mA

† All characteristics are measured with the response control terminal open.

‡ All typical values are at $V_{CC}=5V, T_A=25^{\circ}C$

Switching Characteristics, $V_{CC}=5V, T_A=25^{\circ}C$

SYM BOL	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	4	$C_L=15pF, R_L=3.9k\Omega$	25	85		ns
t_{PHL}	Propagation delay time, high-to-low-level output		$C_L=15pF, R_L=390\Omega$	25	50		
t_{TLH}	Transition time, low-to-high-level output		$C_L=15pF, R_L=3.9k\Omega$	120	175		ns
t_{THL}	Transition time, high-to-low-level output		$C_L=15pF, R_L=390\Omega$	10	20		

Parameter Measurement Information

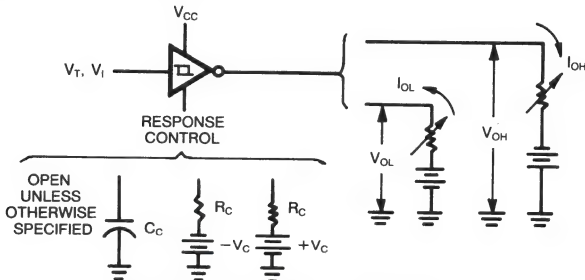


Figure 1 — $V_{T+}, V_{T-}, V_{OH}, V_{OL}$

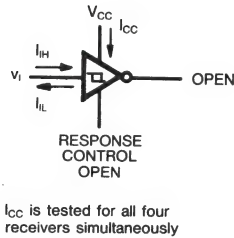


Figure 2 — I_{iH}, I_{iL}, I_{CC}

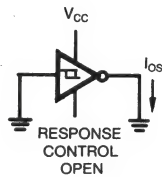
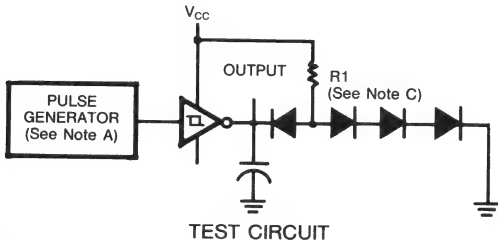
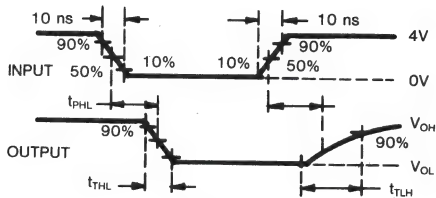


Figure 3 — I_{OS}



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 4 - Switching Times

- NOTES: A. The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega, t_w = 500ns$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent

Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Typical Characteristics

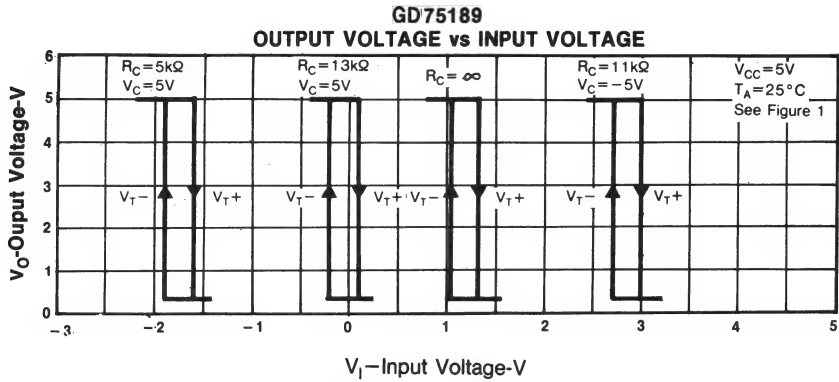


FIGURE 5

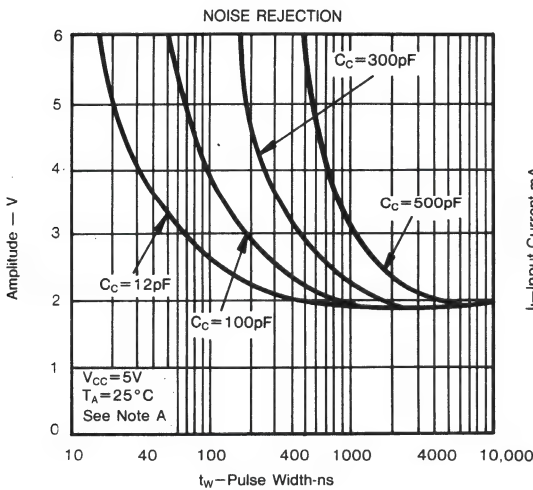
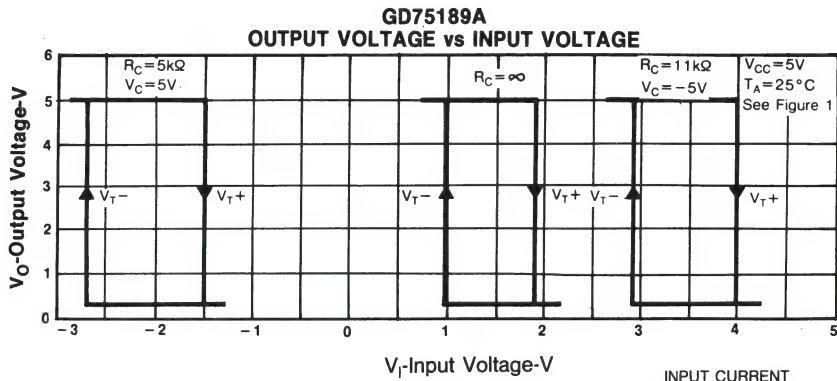


Figure 6

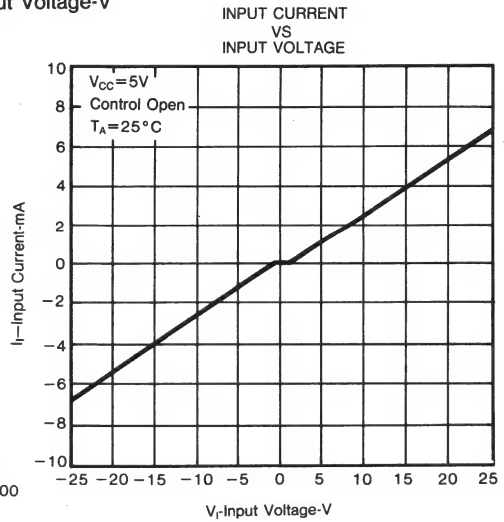


Figure 7

NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from zero volts, will not cause a change of the output level.

GD26LS29

QUAD THREE-STATE SINGLE ENDED RS-423 LINE DRIVER

Feature

- Four single ended line drivers in one package for maximum package density
- Output short-circuit protection
- Individual rise time control for each output
- 50 Ω transmission line drive capability
- High capacitive load drive capability
- Low I_{CC} and I_{EE} power consumption (26mW/driver typ.)
- Meets all requirements of RS-423
- Three-state outputs for bus oriented systems
- Outputs do not clamp line with power off or in hi-impedance state over entire transmission line voltage range of RS-423
- Low-current PNP inputs compatible with TTL, MOS and CMOS
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- 100% reliability assurance screening to MIL-STD-883 requirements

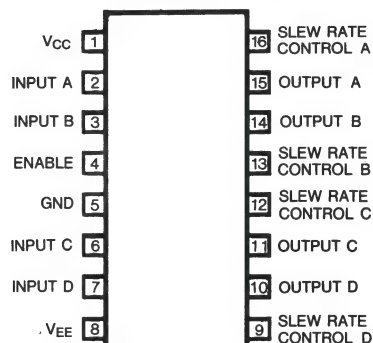
Functional Description

The GD26LS29 is a quad single ended line driver, designed for digital data transmission. The GD26LS29 meets all the requirements of EIA Standard RS-423 and Federal STD 1030. It features four buffered outputs with high source and sink current, and output short circuit protection.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

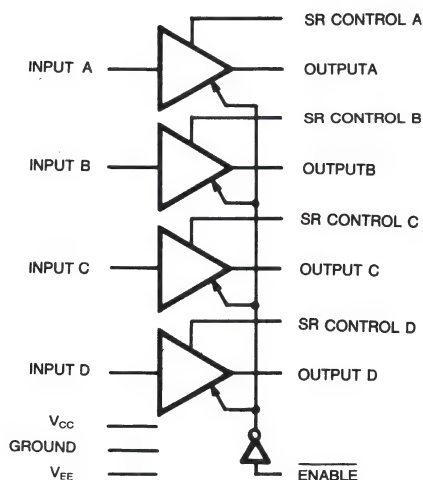
The GD26LS29 has three-state outputs for bus oriented systems. The outputs in the hi-impedance state will not clamp the line over the transmission line voltage of RS-423. A typical full duplex system would use the GD26LS29 line driver and up to twelve GD26LS32 line receivers or an GD26LS32 line receiver and up to thirty-two GD26LS29 line drivers with only one enabled at a time and all others in the three-state mode.

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package

Logic Diagram



ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Supply Voltage	
V+	7.0V
V-	-7.0V
Power Dissipation	600mW
Input Voltage	-05 to +15.0V
Output Voltage (Power Off)	±15V
Lead Soldering Temperature (10 seconds)	300°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O \bar{V}_O	Output voltage	$R_L = \infty$ $V_{IN} = 2.4V$	4.0	4.4	6.0	Volts
		$V_{IN} = 0.4V$	-4.0	-4.4	-6.0	Volts
V_T \bar{V}_T	Output Voltage	$R_L = 450\Omega$ $V_{IN} = 2.4V$	3.6	4.1		Volts
		$V_{IN} = 0.4V$	-3.6	-4.1		Volts
$ V_T - \bar{V}_T $	Output Unbalance	$ V_{CC} = V_{EE} $, $R_L = 450\Omega$		0.02	0.4	Volts
I_{X+} I_{X-}	Output Leakage Power Off	$V_{CC} = V_{EE} = 0V$ $V_O = 10V$		2.0	100	μA
		$V_O = -10V$		-2.0	-100	μA
I_{S+} I_{S-}	Output Short Circuit Current	$V_O = 0V$ $V_{IN} = 2.4V$		-70	-150	mA
		$V_{IN} = 0.4V$		60	150	mA
I_{Slew}	Slew Control Current	$V_{SLEW} = V_{EE} + 0.9V$		±110		μA
I_{CC}	Positive Supply Current	$V_{IN} = 2.4V$, $R_L = \infty$		18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$		-10	-22	mA
I_O	Off State (High Impedance) Output Current	$V_{CC} = MAX.$ $V_O = 10V$		2.0	100	μA
		$V_O = -10V$		-2.0	-100	μA
V_{IH}	High Level Input Voltage		2.0			Volts
V_{IL}	Low Level Input Voltage				0.8	Volts
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$		1.0	40	μA
		$V_{IN} \leq 15V$		10	100	μA
I_{IL}	Low Level Input Current	$I_{IN} = -12mA$			-1.5	mA

AC CHARACTERISTICS $V_{CC} = 5.0V$, $V_{EE} = -50V$, $T_A = 25^\circ C$

PAR-AMETERS	DESCRIPTION	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
Sr+	Positive Slew Rate	$R_L = 450\Omega$, $C_L = 500pF$, Fig. 1 $C_C = 50pF$		3.0		μs
		$C_C = 0pF$		120	300	ns
Sr-	Negative Slew Rate	$R_L = 450\Omega$, $C_L = 500pF$, Fig. 1 $C_C = 50pF$		3.0		μs
		$C_C = 0pF$		120	300	ns
Src	Slew Rate Coefficient	$R_L = 450\Omega$, $C_L = 500pF$, Fig. 1		0.06		$\mu s/pF$
t_{LZ} t_{HZ} t_{ZL} t_{ZH}	Output Enable to Output	$R_L = 450\Omega$, $C_L = 5.0pF$, $C_C = 0pF$		180	300	ns
				250	350	
		$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$		250	350	
				180	300	

- Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, $25^\circ C$ ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

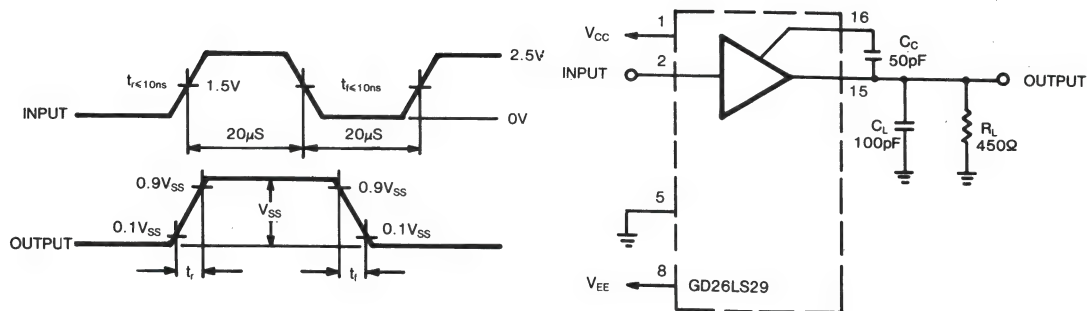


Figure 1. Rise Time Control.

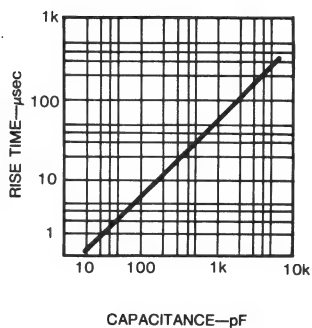


Figure 2. Slew Rate (Rise or Fall Time) Versus External Capacitor

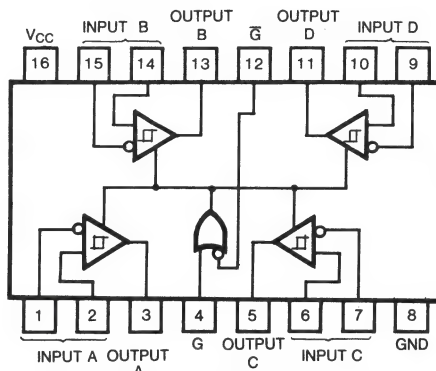
GD26LS33A

QUAD DIFFERENTIAL LINE RECEIVERS

Feature

- GD26LS33AC has $\pm 15\text{-V}$ Common-Mode Range with $\pm 500\text{ mV}$ Sensitivity
- Input Hysteresis ... 50 mV Typical
- Operates From a Single 5-V Supply
- Low-Power Schottky Circuitry
- 3-State Outputs
- Complementary Output Enable Inputs
- Input Impedance ... $12\text{ k}\Omega$ Min

Pin Configuration



Suffix-Blank: Plastic Dual In Line Package
 Suffix-J : Ceramic Dual In Line Package

Description

GD26LS33A is quadruple line receiver for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. Three-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

Function Table (Each Receiver)

DIFFERENTIAL INPUT	ENABLES G \bar{G}		OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	H	X	L
	X	L	L
X	L	H	Z

H = high level, L = low level, X = irrelevant
 Z = high impedance (off), ? = indeterminate

Absolute Maximum Ratings over Operating Free-Air Temperature Range (Unless Otherwise Noted)

- Supply voltage, V_{CC} 7V
- Input voltage 5.5V
- Differential input voltage (see Note 2) $\pm 25\text{V}$
- Enable input voltage 7V
- Low-level output current 50 mA
- Continuous total dissipation at (or below) 25°C free-air temperature 1W
- Operating free-air temperature range 0°C to 70°C
- Storage temperature range -65°C to 150°C
- Lead temperature $1/16$ inch (1.6 mm) from case for 60 seconds: J package 300°C
- Lead temperature $1/6$ inch (1.6 mm) from case for 10 seconds: package 260°C

NOTES: 1. All voltage values, except differential voltage, are with respect to the network ground terminal.
 2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IC}	Common mode input voltage		± 15	V
I_{OH}	High-level output current		-440	μA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	$^{\circ}C$

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP *1	MAX	UNIT
V_{TH}	Differential input high-threshold voltage	$V_{OH}=2.7\text{ V}$ $I_{OH}=-440\text{ }\mu A$		0.5		V
V_{TL}	Differential input low-threshold voltage	$V_{OL}=0.45\text{ V}$, $I_{OL}=8\text{ mA}$	-0.5			V
$V_{T+}-V_{T-}$	Hysteresis *3			50		mV
V_{IH}	High-level enable input voltage		2			V
V_{IL}	Low-level enable input voltage				0.8	V
V_{IK}	Enable input clamp voltage	$V_{CC}=4.75\text{ V}$ $I_I=-18\text{ mA}$			-1.5	V
V_{OH}	Low-level output voltage	$V_{CC}=4.75\text{ V}$, $V_{ID}=1\text{ V}$ $V_{I(G)}=0.8\text{ V}$, $I_{OH}=-440$	2.7	3.5		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75$, $I_{ID}=-1\text{ V}$ $V_{I(G)}=0.8\text{ V}$			0.4	V
					0.45	
I_{OZ}	Off-state (high-impedance-state) output current	$V_{CC}=5.25\text{ V}$, $V_O=2.4\text{ V}$ $V_O=0.4\text{ V}$			20	μA
					-20	
I_I	Line input current	$V_I=15\text{ V}$, Other input at -10V to 15V			1.2	mA
		$V_I=-15\text{ V}$, Other input at -15V to 10V			-1.7	
$I_{I(EN)}$	Enable input current	$V_I=5.5\text{ V}$			100	μA
I_{IH}	High-level enable current	$V_I=2.7\text{ V}$			20	μA
I_{IL}	Low-level enable current	$V_I=0.4\text{ V}$			-0.36	mA
R_{IN}	Input resistance	$V_{IC}=-15\text{ V}$ to 15 V One input to AC ground	12	15		k Ω
I_{OS}	Short-circuit output current *4	$V_{CC}=5.25\text{ V}$	-15		-85	mA
I_{CC}	Supply current	$V_{CC}=5.25\text{ V}$ Data inputs at 0 V All outputs disabled		52	70	mA

*1 All typical values are at $V_{CC}=5\text{ V}$, $T_A=25^{\circ}C$, and $V_{IC}=0$

*2 The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

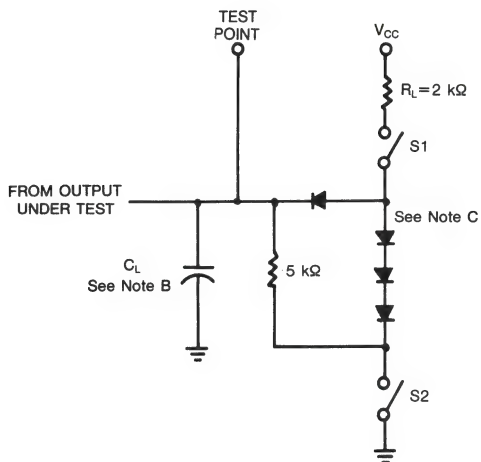
*3 Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} and the negative-going input threshold voltage, V_{T-} .

*4 Not more than one output should be shorted at a time.

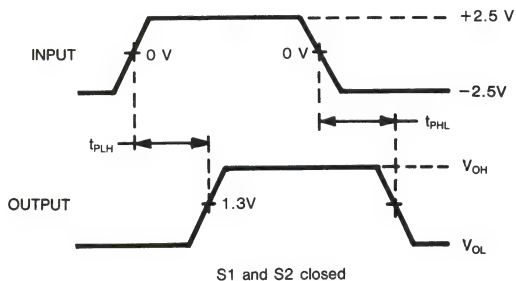
Switching Characteristics, $V_{CC}=5\text{ V}$, $T_A=25^{\circ}C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L=15\text{ pF}$ See Figure 1	20	35		ns
t_{PHL}	Propagation delay time, high-to-low-level output		22	35		ns
t_{PZH}	Output enable time to high level	$C_L=15\text{ pF}$ See Figure 2	17	22		ns
t_{PZL}	Output enable time to low level		20	25		ns
t_{PHZ}	Output disable time from high level	$C_L=5\text{ pF}$ See Figure 1	21	30		ns
t_{PLZ}	Output disable time from low level		30	40		ns

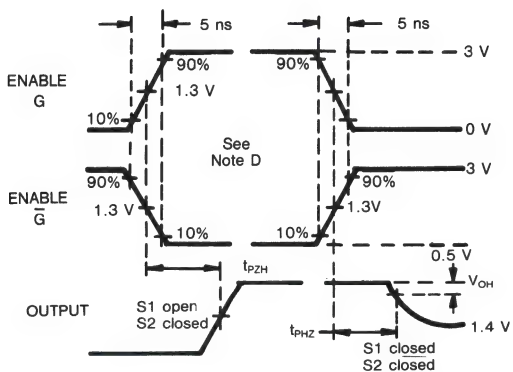
Parameter Measurement Information



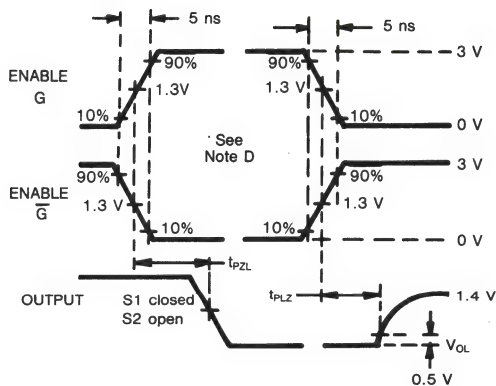
TEST CIRCUIT



VOLTAGE WAVEFORMS for t_{PLH} , t_{PHL}

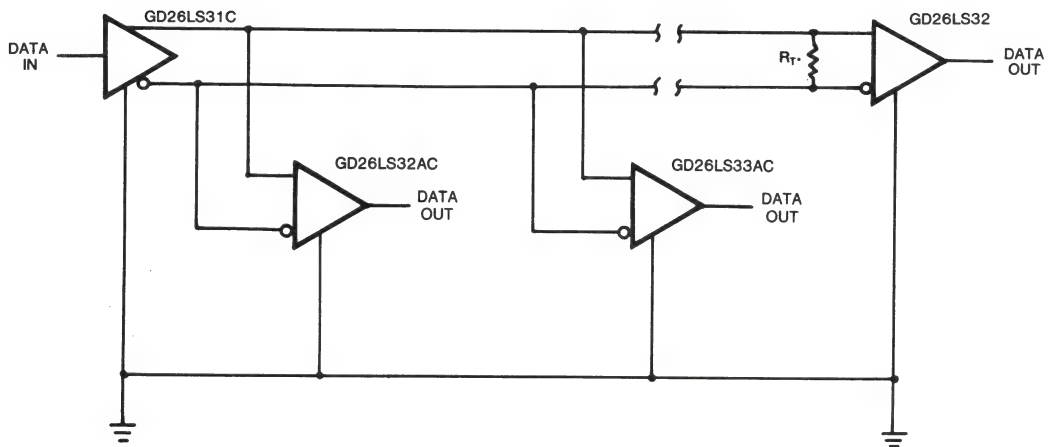


VOLTAGE WAVEFORMS FOR t_{PHZ} , t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ} , t_{PZL}

- NOTES: A. The pulse generator has the following characteristics:
 $Z_{out}=50\ \Omega$ PRR=1 MHz, $t_w=0.5\ \mu s$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.
 D. Enable G is tested with G high, G is tested with G low.

Application Example

* R_T equals the characteristic impedance of the line.

DATA SHEET INDEX

QUALITY ASSURANCE MANUAL

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